Star Test Topology for Testing Printed Circuits Boards

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Abstract— primarily, testing printed circuit boards was manual and based on the board structure, was also limited by the chip complexity. Also, it requires expensive testers and fixtures [1].

The performance of testers depends basically on the device properties. To enhance tester performance, the efforts should be focused on improving testing speed through decreasing the interconnections between the tester and the device under test [2]. The complexity of the interconnections between the device under test (DUT) and the tester became one of the major showstoppers in evaluating the health of DUT [3]. To surpass these constraints, we introduce a new test methodology based on star test topology (STT) for connecting multiple devices. Such topology provides a means of arbitrarily observing test results and source test stimulus. The model requires minimal on chip/board resources (pins/nets). Also, it is not limited by the chip function or complexity. The new methodology involves developing one shared test access port (TAP) over the entire PCB and a re-design of the on-chip DFT circuitry.

Keywords— Start test topology, STT, integrated circuit testing, bidirectional data line, higher functionality, test access port.

1. Introduction

The traditional testing methods is based on the board structure, also its limited by superfine chip packages, double-sided boards, conformal coating, multi-chip modules (MCMs), and chip complexity. Also, it requires expensive testers and fixtures. In such tests, chip functions can be ignored for shorts testing and must be considered for continuity tests [5].

The performance of testers depends basically on the device properties. To enhance tester performance, the efforts should be focused on improving testing speed through decreasing the interconnections between the tester and the device under test. The complexity of the interconnections between the DUT and the tester became one of the major showstoppers in evaluating the health of DUT [6].

Embedding memory and microcontroller units inside the testers also causes many disadvantages. It increases cost, size, and complexity of the tester. On the other hand, decreasing memory size leads to a proportional decrease in the number of devices that can be diagnosed by the tester. Versatile and multi-faceted testers can be manufactured, but the cost will be more expensive. The rapid growth in the complexity of circuits

requires a parallel and continuous development in tester microcontrollers, creating a difficult challenge [7].

To surpass these constraints, we introduce a new test methodology based on JTAG and IEEE 1149.1 Std. The new methodology involves developing one shared test access port (TAP) over the entire PCB and a re-design of the on-chip DFT circuitry. Such improvements will lead to a significant reduction in the complexity of testing nets, resources, and pins connections [8].

The new methodology uses star test topology for connecting multiple devices; such topology provides a means of arbitrarily observing test results and source test stimulus. The model requires minimal on chip/board resources (pins/nets). Also, it is not limited by the chip function or complexity [9]. Moreover, test access is not limited by the physical factors of the board and the test generation is highly automated.

In the new methodology, only one bidirectional data line is utilized in order to carry data between the TAP and each device under test. Therefore, one test access pin is required for each DUT. The new architecture will definitely help in reducing any resultant yield loss due to the proven contact problems [10, 11].

Many features and advantages are achieved by using the new methodology. One such feature is the considerable cost reduction due to utilizing only one TAP to interface all on-board devices, and also due to the high simplification in boundary scan circuits. Further advantage is that each DUT is diagnosed separately without any correlation with other DUTs. Moreover, unlike the IEEE 1149.1 Std, there is no need to embed instructions, identifications, or bypass units inside integrated circuits [12].

2. STT Architicture

As previously mentioned, the new methodology uses STT to connect all the peripherals. Each DUT is connected to the central test access port TAP using point-to-point connections. The TAP acts as a hub and the DUTs are considered as clients. The connection does not necessarily have to resemble a star in order to be classified as a star topology, but all of the DUTs access pins must be connected to one shared TAP. All traffic that traverses the testing

network has to pass through this TAP. It selects the targeted DUT to be tested. It also forwards the test pattern and returns the corresponding test data output (TDO) pattern. To select a different DUT, the computer transmits a test reset signal (TRST) followed by a new data packet. The star topology is an easier topology to design and implement.

The most important advantage of STT is that it responds immediately to any node failure. Only one DUT will be affected if an error occurs, while the entire circuit remains running. Because of this, diagnosing a single device for an error or defect is supposed to be easy.

In STT, the computer broadcasts test-data input (TDI) packets to several DUTs via TAP, and the computer can easily identify any failed DUT. Because of its simplicity in testability, managing the STT using connected DUTs is considered a trivially simple. Moreover, by STT, failures can be located easily by a logical analysis and, as a result, it can be simply diagnosed.

The new system architecture is illustrated in Figure 1; it has TAP acting as main hub and the DUTs represent the nodes. Each DUT exploits only one pin to interface the TAP. Therefore, test signals are directly transferred from TAP to the DUT without passing through other devices. To prevent drive conflicts among the DUTs, the TAP controller handles a direct addressing method.

When a data packet is received by the TAP input line, the port reads the address information in the packet header to determine its ultimate destination. Then, using serial to parallel shift registers and de-multiplexer circuits, it forwards the test packet to the next DUT on its journey; therefore, TAP performs the "data traffic control" function on the circuit.

Each DUT has its own test hub TH. It is the circuit that interfaces multiple inputs and outputs of the DUT and makes them act as a single network segment. The serial signal that is introduced at the input of the TH appears at the parallel outputs of the TH. It is specialized hardware that forwards data packets between TAP and DUT inputs and vice versa.

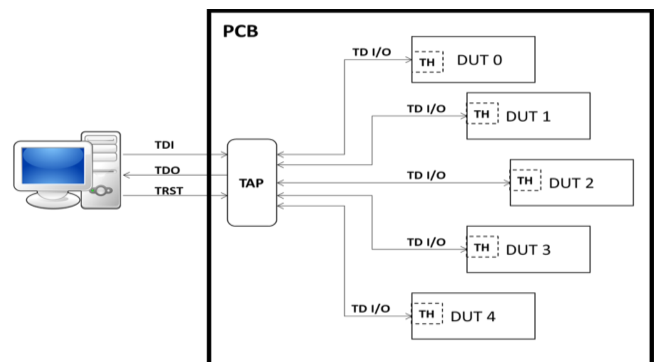

Figure 1: STT Architicture

3. STT Simulation

The circuit is designed and simulated before starting hardware building. We used the National Instruments (NI) Multisim simulation and circuit design software version 12.0.1. It is sophisticated software that gives advanced design and analysis features in order to optimize efficiency, shorten time and reduce design errors toward prototype. Intuitive Multisim tools result in saved (PCB) iterations and significant savings in design costs.

In order to simulate transmitting test patterns by the computer, we used the “Word Generator” instrument that is available in the software. It can send digital words (bit patterns) into digital circuits. The instrument is depicted in Figure 1.

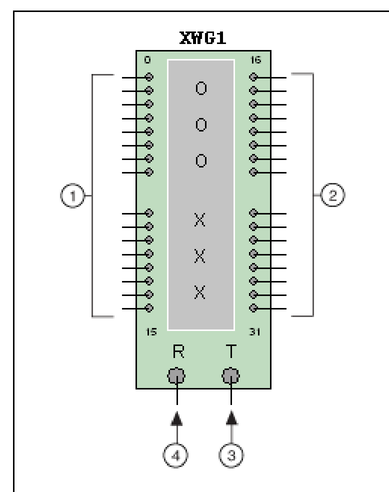

Figure 1: Word generator instrument in Multisim software

The output pins (1) which appear on the left side of the instrument are the last sixteen bits in the 32-bit word, while the output pins (2) on the right side of the instrument are the first sixteen bits in the 32-bit word. Label “T” refers to the external trigger (T) terminal 3, label “R” is assigned for the data-ready terminal (4).

The word generator settings can be entered by double clicking on the instrument face. Figure 1 shows the settings screen for the word generator instrument. As seen clearly in the figure, the output terminals (1) correspond to those on the icon. The buffer (2) generates pre-defined patterns or saves digital patterns.

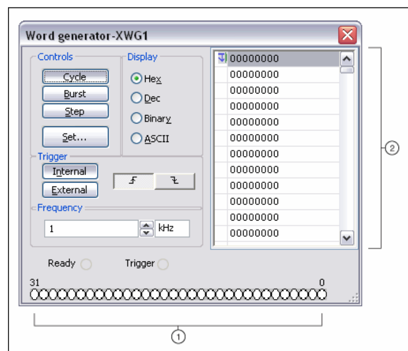

Figure 2: Word generator settings screen

The circuit output signals are captured using the Logic Analyzer instrument. It can display up to 16 digital signals in a circuit. This instrument offers an improved timing analysis and rapid data acquisition of logic states to help perform troubleshooting and design very large systems. Figure 3 shows the icon of the logic analyzer instrument. Section 1 indicates the input terminals, section 2 is the external clock terminal, section 3 is the clock qualifier terminal, and section 4 is the trigger qualifier terminal.

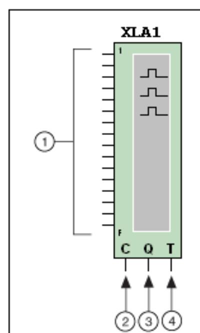

Figure 3: Multisim Logic Analyzer icon

4. Capturing and Transmitting Response Patterns

The TDO transmitter circuit carries out capturing the response signals of the IC under test and broadcasting it in a serial manner. It includes three main units: loading control unit, parallel to serial shift register, and counter unit, as illustrated in Figure . The startup signal generated by the TDI driver unit returns to play an important role in activating this unit; it stimulates the loading control unit to load the shift register and also it switches on the capturing counter circuit. The capturing period is determined by the capturing counter running time. At the end of the counting period, a reset signal is generated by the counter unit to stop running the loading control unit.

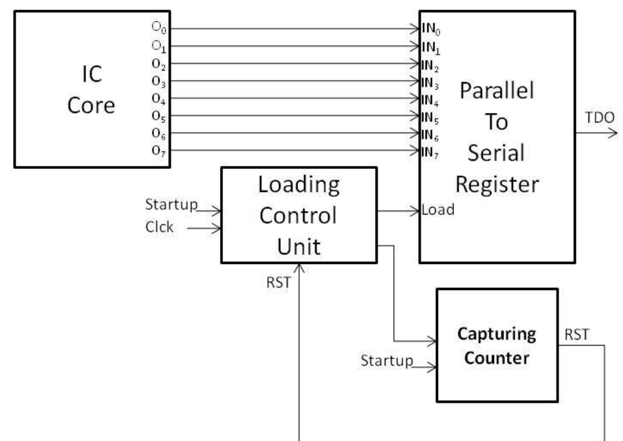

Figure 5: TDO transmitter block diagram

The circuit diagram shown in Figure 4 represents a TDO transmitter for a four-output IC. The loading control unit is formed of a D flip flop (74HC74D). It possesses three inputs: startup, clock, and reset. At the moment the startup signal turns to high, the D flip flop generates a load signal to the shift register and the counter starts running. When the counter finishes counting, it sends a reset signal to the D flip flop causing unload for the shift register.

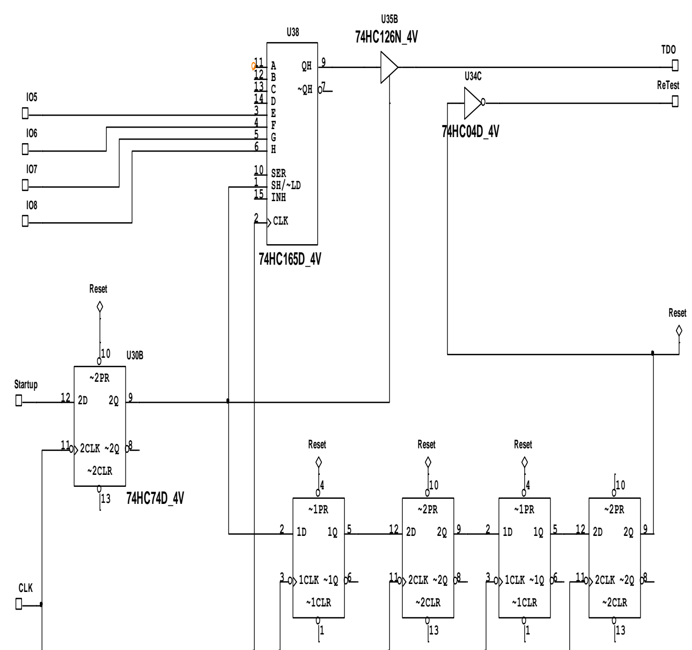

Figure 46: TDO transmitter circuit diagram

Since we utilize only one IN/OUT pin for testing, the TDO should be shifted out serially, bit by bit. For this reason we used a NXP-74HC165N shift register to perform parallel to serial shifting. The 74HC165 is a high-speed Si-gate CMOS device that complies with joint electron device engineering

council (JEDEC) standard 7A. It is pin-compatible with a low-power Schottky TTL (LSTTL).

The 74HC165 are 8-bit, parallel-load registers with complementary serial outputs. The parallel input data (D_0–D_7) will be loaded asynchronously into the register if the parallel load ($\overline{PL}$) input is 0. Otherwise, data penetrates the register serially bit by bit at the date serial (DS) input and shift once to the right (Q0→Q1→Q2, etc.) with each rising edge clock pulse if and only if the ($\overline{PL}$) input is 1. Hence, by tying the DS input to the Q7 output we allow parallel-to-serial converter expansion of the succeeding stage. One input is allowed to be used as an active LOW clock enable (CE) input since the clock input is a gated-OR structure. The assignment for the input pins CP and CE is arbitrary; it can be rearranged based on the layout convenience. For predictable operation, the rising edge (LOW→High) of the input CE can only take place while CP is High. To avoid any data shifting while $\overline{PL}$ is activated, either theca or the CE signals must be High before the rising edge of $\overline{PL}$ signal.Table 4 illustrates the functional description for the serial out shift register.

Table 41: Function table for NXP-74HC74 shift register

Operating modes	Inputs					Qn registers		Outputs	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q7}$
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$

The IC response pattern must be settled on the shift register inputs for N clock pulses where N is the number of IC outputs. The pattern will be loaded while the $\overline{PL}$input is low. When the startup signal turns to high, the $\overline{PL}$ input receives a High signal from the D flip flop and the shift register starts serializing the pattern (Figure 4 7).

This register is chosen also because of its capability to deal with excess currents that may result from defective ICs. As listed in Table 2, the register can afford an input clamping current of up to 20 mA. Moreover, it can be embedded in high-temperature industrial integrated circuits with a temperature up to 150°C.

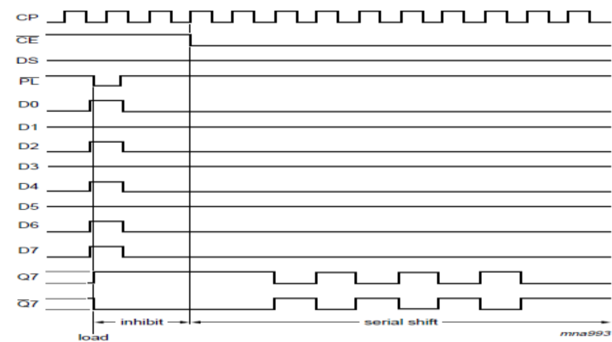

Figure 47: Timing diagram for NXP-74HC74 shift register

Table 2: Limiting values for NXP-74HC74 shift register

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−65	+150	°C

5. Conclusion

The proposed testing circuit was simulated successfully by NI Multisim software. It smoothly transmitted test patterns and received the corresponding response patterns. The circuit succeeded in testing four ICs accurately. Also, the hardware was built and ran successfully. It performed a precise testing for several ICs.

The driving Arduino source code was written, compiled, and loaded successfully. It prompts the user to enter the initial values and accordingly drives the TAP interface. All the system parts successfully integrated together to perform an advanced and sophisticated test.

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