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Power Efficient 4 Bit Flash ADC Using Cadence Tool

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Abstract - ***ADCs*** *are the essential building blocks of digital systems and are now used in a wide range of applications to enhance them and make them perform better than analog alternatives. When analog signals are converted to digital signals and then processed in real-time and mixed signal systems, flash ADC has several uses. For many applications, a high speed and low power ADC is absolutely necessary. The architecture of choice where the highest sample rate and moderate resolution are required is flash ADCs. Despite being the quickest type now available, flash ADC requires a huge number of integrated circuits to implement. Using the Cadence tool, this simulation is performed using 180nm technology. Tabulated simulation results have been documented.*

Key Words: **Flash ADC, Resistor Ladder, Comparator, Encoder; Power Dissipation**

1.INTRODUCTION

The improvement of integrated circuit technology over the past ten years has sped up the development of digital signal processors. Additionally, digital processing has the benefit of being more noise-resistant. The analog-to-digital converter functions as an interface for both analog signals and the digital signal processing system as a result. Wireless communication systems ongoing speed improvements have led to enormous demands on high-speed, low-resolution analog-to-digital converters power and speed standards.In actuality, processing, testing, and storing of digital signals are made simple. In order to process the analog signal, we convert it to a digital signal. An analog-to-digital converter could be used as the bridge to do this. Researchers are looking into new model strategies for in an ADC in an effort to boost performance while lowering power consumption. Due to the fact that flash ADC design commonly plays a major part in other forms of ADCs, it becomes progressively important in all other forms of ADCs, including pipelined and multi bit sigma delta ADCs.

Fig-1 illustrates the block diagram for an N-bit Flash ADC. A resistor ladder, a comparator arrangement, and a thermometer to binary code encoder are the three components that make up a Flash ADC. The use of a resistor ladder produces several reference voltages. The comparator array compares the incoming analog input to these created reference voltages to produce the associated thermometer code. These thermometer codes are input into the digital encoder, which turns those into the corresponding binary codes.

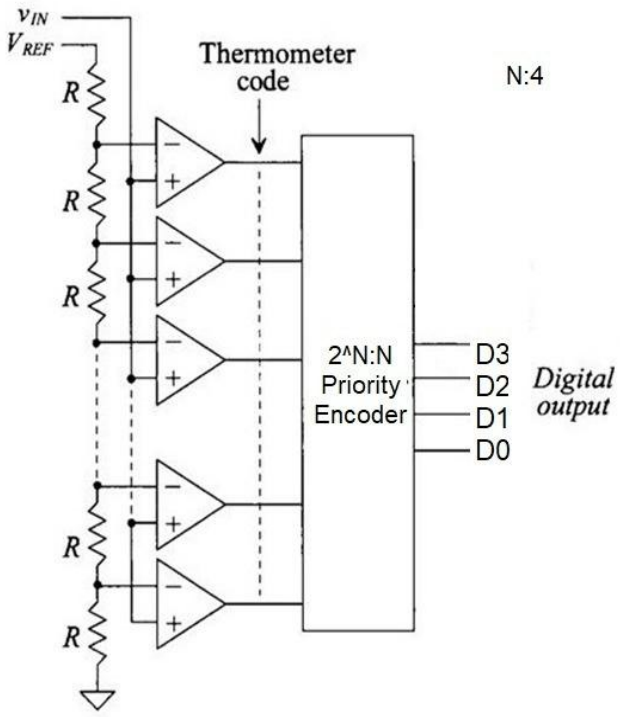

Fig - 1: Block Diagram of 4-bit Flash ADC

Of all ADC types, flash or parallel converters operate at the fastest speed. As seen in Fig. 1 They employ two resistors and one comparator for each quantization level (2-1). (a resistor string DAC). Each of the two values from the reference voltage is put into a comparator. Once the input voltage has been compared to each reference value, the comparators output generates a thermometer code.

If the voltage on the resistor string is greater than Vin or equal to Vref, the thermometer code displays all ones for each resistor level. Otherwise, it displays all zeros. The comparative data is transformed into a TV-bit digital word using a straightforward 2-1: N digital thermometer decoder circuit.

2.IMPLEMENTATION

1.1 Resistor Ladder

The fundamental objective of the resistor ladder is to supply a stable reference voltage to the comparators. The resistor ladder network, which is composed of 2N resistors, generates the reference voltage for each comparator. The reference voltage for all comparators above it, as illustrated in Fig 2, is one least significant bit (LSB) less than the reference value for the comparator immediately.

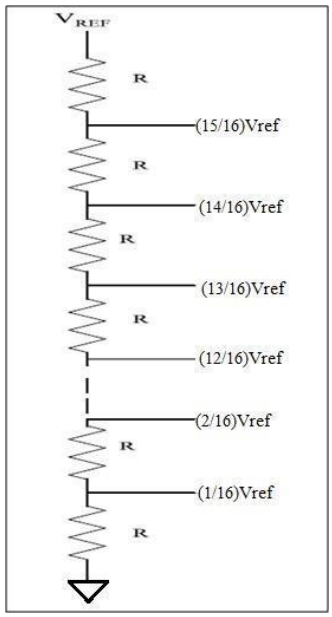

Fig – 2: Resistor Ladder

1.2 Comparator

An essential component of practically all analog-to-digital (ADC) converter types is the comparator. In the digital world of today, nothing is analog. To convert the analog data to digital data, we must therefore employ ADCs. The field of high-speed low power ADCs is currently the subject of extensive research. As technology advances, power consumption can be decreased with the use of small feature size procedures. Comparators are crucial to the development of an ADC. The crucial factors for any sort of comparator are speed, gain, power dissipation, offset, and resolution. Performance of the target application is significantly impacted by the type and architecture of the comparator. In Fig. 3, a block diagram of a comparator is displayed.

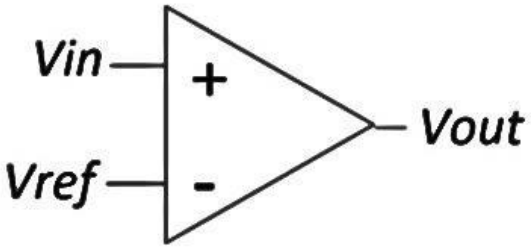

Fig – 3: Basic Block Diagram of Comparator

For Flash ADC to operate at its best, a differential comparator was chosen. Op-Amps are essentially DC-coupled, high-gain electronic voltage amplifiers with single-ended output waveforms and differential input signals. The operational amplifier (op-amp) is composed of a differential input stage driving a current mirror load and a common-source amplifier stage after that the input differential amplifier block is designed with high input impedance, high CMRR and PSRR, low noise, high gain, and low offset voltage. In the second phase of the op-amp, level shifting with increased gain and single ended to differential conversion are carried out. This design's power consumption and propagation delay are both noticeably less. The differential input signal is converted to a single-ended signal with the help of the current mirror architecture. Load also helps with common mode rejection ratio. As shown in the Fig. 4, a common source amplifier is employed to increase the first stage's gain and output swing.

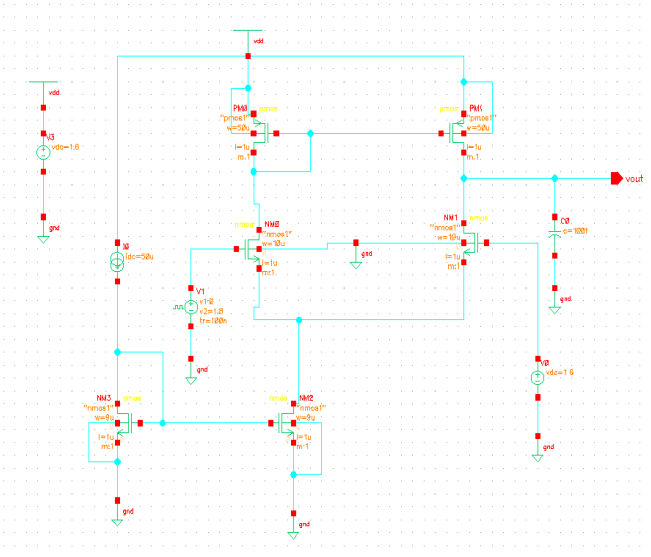

Fig – 4: Differential Comparator

1.3 Encoder

A decoder's output code usually contains more bits than its input code. Figure 5 shows the block diagram represents an encoder, which is a device whose output code has less bits

than its input code. As a result, an encoder performs the opposite role from a decoder. The provided data is compressed into a smaller form. The most popular encoders are binary encoders and priority encoders.

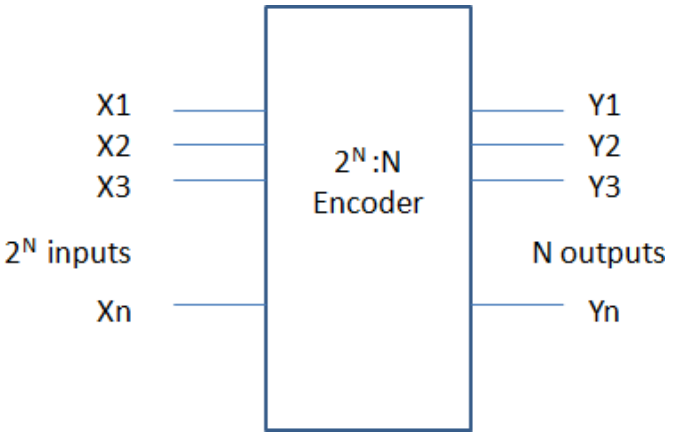

Fig – 5: Block Diagram Of Encoder

For Flash ADC to operate at its best, a differential comparator was chosen. The output of the thermometer code is transformed to a binary code at the comparator stage's output using the thermometer to a binary encoder. The unary code for the natural number n, which is either n or (n-1) ones followed by a zero, is known as the thermometer code, which is produced using the threshold inverting quantization (TIQ). The output may not be a thermometer code symbol but does contain certain anomalies. The thermometer to binary converter step may not be able to convert it to binary code since it is frequently a state machine that only takes thermometer code as inputs and may produce garbage output if given with any other input which is not thermometer code, as seen in Fig. 6.

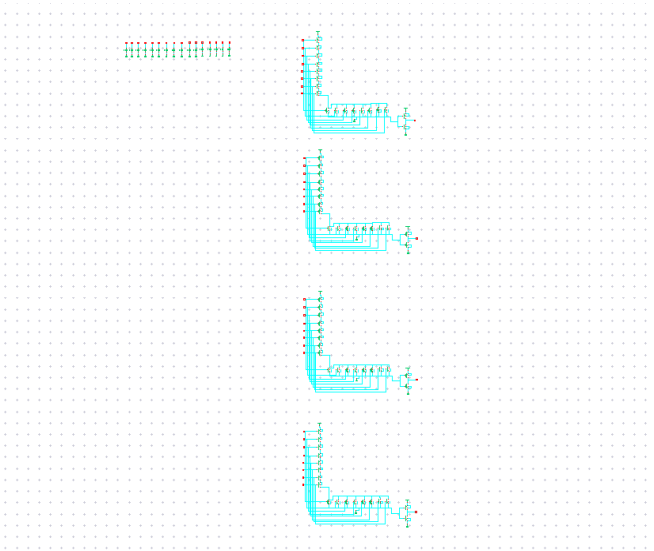

Fig – 6: OR Gate Based Encoder

1.4 Flash ADC

In the earlier concepts, an OR-based encoder and several comparators are discussed for a 4-bit flash ADC. The three major components of the flash ADC are the thermometer to binary code converter, comparators, and resistor ladder. In this scenario, a 4-bit flash ADC is created by combining the aforementioned building parts.

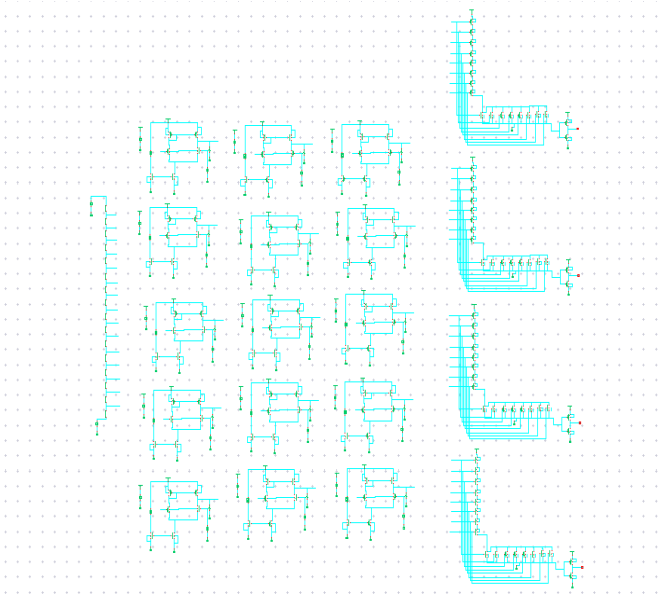

Fig – 7: Schematic of the 4 Bit Flash ADC

3.RESULT AND ANALYSIS

Using Cadence Virtuoso in 180nm technology, all of the schematics were successfully created, and they were all examined in a spectre simulator.

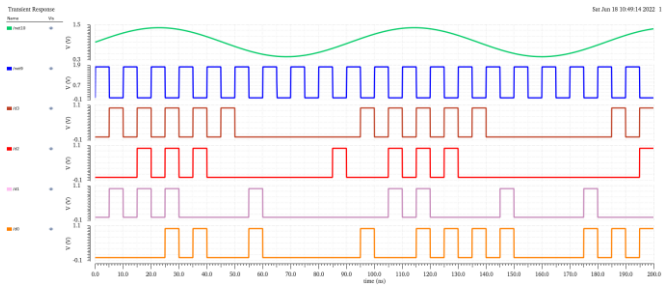

Fig – 8: Transient Analysis of the 4 bit Flash ADC

For low power applications, the suggested design provides a low-power solution with less Kickback noise. 180nm technology is used to simulate and assess this design.The findings of the simulation have been tabulated and analysed.

Table -1: Result Analysis of 4-bit Flash ADC

Result Analysis of 4-bit Flash ADC	
Parameters	**Proposed Design**
Architecture	Flash ADC
Resolution	4-bit
Technology	180 nm
Frequency	11 MHz
Power Dissipation	2.88 mW
VDD	1.8 V
Delay	12.9 ns

4.CONCLUSION

The ideal architecture for high-speed and low-power applications is thought to be the flash ADC. A variety of comparators and encoders were built and analyzed. A differential comparator is chosen from among them. Additionally, OR gate-based encoders are simple to pipeline, ensuring that they will never be the slowest component of an analog-to-digital converter architecture. The maximum inaccuracy that can be produced by this encoder is one LSB if there is any bubble in the comparator output. A 4 bit Flash ADC is constructed and its performance is evaluated by combining the resistor ladder with the comparator and encoder. The developed Flash ADC has a power dissipation of 2.88mW.

The majority of power dissipation in CMOS circuits occurs through dynamic power dissipation as opposed to static power dissipation. CMOS devices only dissipate a few nanowatts of static power. The transition activities of the circuits are the main cause of dynamic power dissipation. A higher operating frequency causes the circuits to undergo more transitional activities, which increases power loss. The circuit's switching activity may be decreased by using appropriate encoding methods. As a result, less transition activity will occur overall. As a result, the dynamic power dissipation in VLSI circuits can be efficiently decreased.

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