# Design and Development of 4-Bit Adder Programmable QCA Design using ALU Technique

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**Abstract -** *QCA as the name suggests stands for Quantum dot Cellular Automata is a domain in nano-technology employed in several digital circuits and stupendously used in electronics world. With the advancement in VLSI designs and technology, QCA design acts a powerful tool in modern day electronics in solving adder circuits. QCA cells can be utilized in many ways to study PLD design. This method basically proposes specialized architecture procedure to program devices and simulation is also done to tune QCA cells aimed for this specialized development design. This design provides an insight and idea about how adders are implemented in measuring and electronic instruments and their applications in the digital world. The performance of the respective QCA cell structures are simulated and it is tested by designer tools. It is cost – effective and relatively uses very less equipment. This mainly discusses about the area and transistor count with propagation delay. The main idea of this paper is to show how QCA cells are implemented by ALU technique with 4-bit adder circuit.*

**Keywords- QCA cells, PLD design, VLSI technique, ALU technique, RLU**

## 1. INTRODUCTION

QCA is a domain in nanotechnology used in modern sciences and proved in present era and it is sometimes inculcated and instructed in CMOS semiconductor [1]. While designing circuits, the important element is that it is arriving at the dimension which is a concern of possibility. It uses high power and leakage current. It is prominent and useful technology with minimum loopholes. A QCA cell is accounted of a couple of free electrons, probably confined in a potential [2]. It applies CMOS technology and operations of QCA are handled using ALU design. A polarized data is handled and four clocking systems are done periodically. There exists heavy work in every design of digital logic. An extensive innovative work in the field of a domain named frilled technology made it feasible for engineers and lessen the size of semiconductor. The uniqueness lies in finding an adder for 4-bit using carbon nanotubes and QCA cells based on the current CMOS based VLSI technology that can potentially increase scaling by lowering/hindering high power consumption.

The main advantage of having QCA cells is that it uses minimum power for adder circuits of 4-bits. By using Moore's law we know that the total transistors gets an increase by 50% in CMOS rising to size reduction and high power dissipation [1].In ALU design in QCA cells the literature have important features which includes working under various temperatures and the amount of energy dissipated from the circuit. This perfectly strikes the chord and momentum in the paper.

The major shortcomings lies with the QCA cells which contains four to eight quantum spots, where the position of the electrons in columbic is unidentified in 1-bit ALU circuit . This paper depicts that in advanced 4-bit adder circuits the design can be executed well by using ALU technique which performs logical as well as the arithmetic operations without any propagation time delay with ease.

## 2. FUNDAMENTALS OF QCA CELLS:

### 2.1. QCA Cells:

Basically QCA cells are also termed in emergency technologies and have the potential to build future computers through ALU. In QCA, a device which is sensitive called QCA cell is used as a fundamental unit of QCA block for growth or maturation of small number of constituent particles applied in a circuit (computing wires)[1]. We arrive at a term called quantum dot placed at a proper diagonal square cut in a linear order. A model of QCA cell is shown in fig

1(a).Polarization is a process where it is used in field of electromagnetic radiations in which the direction and magnitude are specified of a vibrating particle.

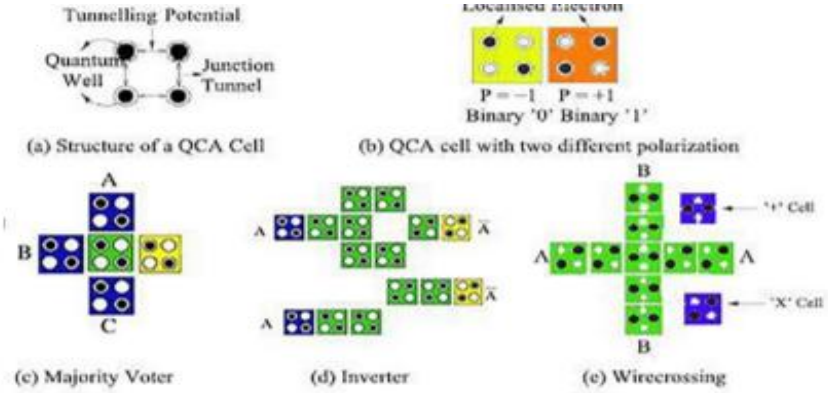



**Fig 1(a)**: a model representation of QCA cell.

### 2.2. QCA clocking:

QCA clocking is a defined as the areas where the conduction happens, in other words it can be explained as they are the conductive materials which modulate electron tunneling barriers of QCA cell in operation. The tunneling barrier has a pair of Q-dots in QCA cell where in the first stage cells where it stupendously increases. In the very first stage computation process takes place. In the second stage electrons of QCA cell are barred from entering the tunneling process. In the third stage the cells of QCA moves from higher threshold to lower threshold levels .A detailed process is shown in fig 1(b).

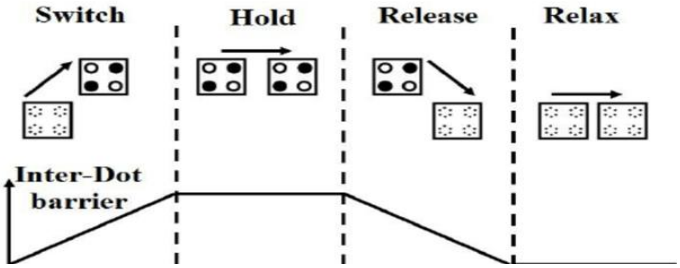



**Fig 1(b):** process of QCA

## 3. FUNCTIONALITIES OF ARITHMETIC LOGIC UNIT (ALU):

### 3.1. Reversible ALU:

It is an arithmetic circuit and an integral component of CPU in the monitor system. The number of logical calculations selected varies depending on the number of inputs and outputs according to the circuit. It is widely used in QCA cells to interpret output using arithmetic logic [2].

The implementation of ALU in CPU and few other applications have complex design and cost-effective [4].

It is basically divided into two modules reverse logic unit (RLU) and reversible arithmetic unit (RAU), ALU is flexible is implemented in logic gates.

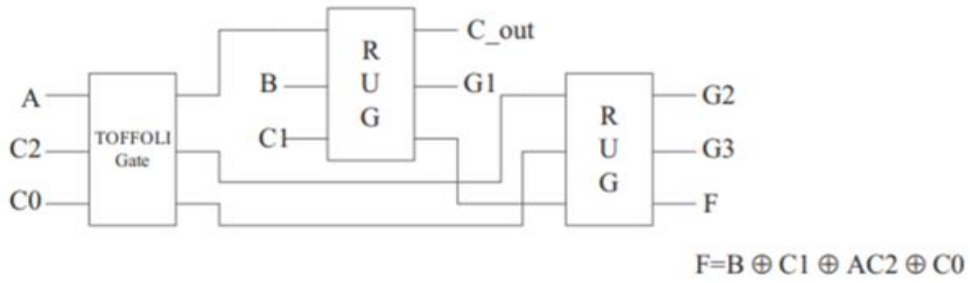



**Fig 2(a):** Circuit diagram of Reversible ALU

### 3.2. Reversible Logic Unit (RLU):

Usually 4:1 Mux is generally preferred multiplexer and it is a 1 bit logic gates and acts a CNOT gate and uses 4RM gates connected in linear fashion. This can be then advanced to 4-bit adder gates also [2].The combinations of binary numbers such as 0 and 1 are tried in varied combinations in various gates and realized through A0,A1,A2,A3 by gates such as NOR,NAND,AND,OR and EX-OR gates.

The functional description is shown below in Fig 2 (b) and QCA cells representation in 2(c).

| A0 | A1 | A2 | A3 | Operation |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | NOT |
| 0 | 0 | 1 | 0 | NAND |
| 0 | 0 | 1 | 1 | XOR |
| 0 | 1 | 0 | 0 | NOR |
| 0 | 1 | 0 | 1 | - |
| 0 | 1 | 1 | 0 | NOT |
| 1 | 0 | 0 | 1 | COPY |
| 1 | 0 | 1 | 0 | Constant |
| 1 | 0 | 1 | 1 | OR |
| 1 | 1 | 0 | 0 | XNOR |
| 1 | 1 | 0 | 1 | AND |
| 1 | 1 | 1 | 1 | COPY |

**Fig 2(b):** Functional description of RLU

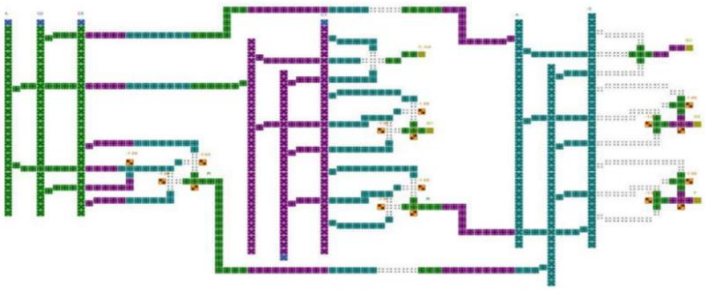


**Fig 2(c):** QCA description of RLU

### 3.3. Reverse Arithmetic Unit:

A reverse arithmetic unit being a fundamental unit of ALU does the inverse operation of ALU .It consists of a full adder which has 5 input and 2 outputs. To this contrary there are 6 garbage outputs (G0, G1, G2, G3, G4, G5).These are the fundamental functionalities of RAU [2]. It has the following inputs: M, N, O', O'', O''', O4. It clocks nearly 6 clock delays with a time delay. The fig 2(d) shows a functional description of RAU and QCA pictorial representation in 2(e).

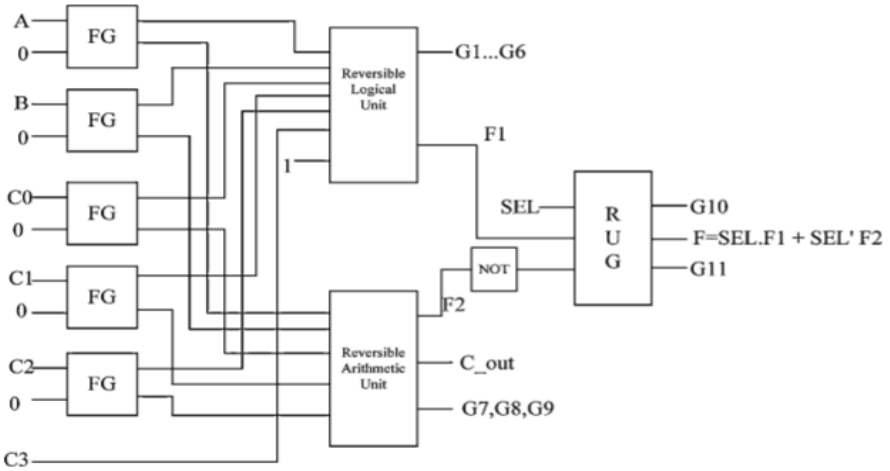



**Fig 2(d)**: Functional description of RAU using decoders

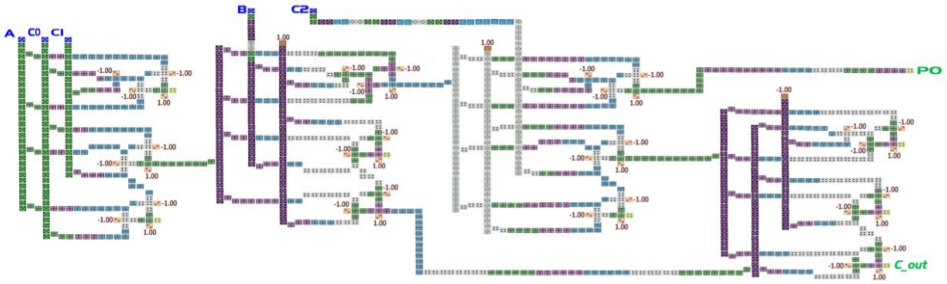



**Fig 2(e):** QCA description of RAU

### 3.4. Fault tolerance of RUG:

This process occurs during QCA manufacturing which consists of various phases that include both deposition and synthesis phase it includes additional cells and cell misalignment in reverse unit logic design.

We use Verilog library for the implementation of QCA cells, this can be converted into hardware language that majorly includes Verilog HDL definitions and elements of QCA like fan-out, fan-in, and many other applications of logic design. These QCA cells come from fault injection capability. It has a respective HDLQ Model of RUG. We assign certain variables like A, B, Y, where P=1.The fault tolerance is explained in fig 2(f).

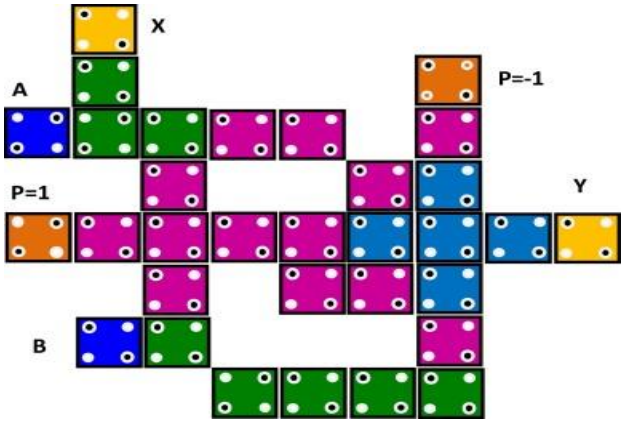



**Fig 2(f):** Fault tolerance of RUG by QCA cells

### 3.5. Design of a 4-Bit ALU design:

It is designed particularly based on the logic of cascading a four 1-bit ALU by integrating all.This consists of:

a) 4:1 Multiplexer

b) 2:1 Multiplexer to perform both arithmetic and logical operations. A single bit uses a complete full adder and one multiplexer.This is explained by having one complete full adder and three MUX(Multiplexers).

We use select lines A2,A1,A0.The proposed table is shown in fig 2(g).

| A2 | A1 | A0 | Operations |
|---|---|---|---|
| 0 | 0 | 0 | Addition |
| 0 | 0 | 1 | Subtraction |
| 0 | 1 | 0 | A<B |
| 0 | 1 | 1 | A>B |
| 1 | 0 | 0 | AND gate |
| 1 | 0 | 1 | OR gate |
| 1 | 1 | 0 | EXOR gate |
| 1 | 1 | 1 | NOT |

**Fig 2(g):** ALU operation

QCA cells plays a significant role in RAU [4]. QCA also reduces power consumption in both reversible and non- reversible circuits in adiabatic and inherent environments. In most preferences, adiabatic circuits are irreversible where technological changes are made keeping reversibility and adiabatic principles in mind.

## 4. PROPOSED METHODOLOGIES:

The proposed operation has a logical touch performed by QCA cells which is executed by a NOT gate. This demonstrates that XOR gate has a configuration rather than considering the cell method process; the result accomplishes the impact of QCA cells on each other. These XOR gates are majority inverter based .Input here are x, y, z while the output cell is' a'. It has 12 QCA cells where polarization 'e' is around '+1' which performs XOR function.

### 4.1. Full Adder Circuits:

The basic functionalities of ALU processing unit consists of both arithmetic and logical expressions in ALU is of a full adder .This consists of a Co-planar crossover which is way advanced compared to multilayer crossover that QCA cells are used 45 rotated functions are considered as not connected cells. These circuits have been designed according to the coplanar crossover. These circuits with a 1-bit adder as primary adder circuit which includes a not gate which acts as an inverter and then a majority Voter.[1] This full adder are A0,B0,CI are results where the output is both sum and carry. And input is taken from 3 input Nand gate(IC-7410). This is performed by applying ALU technique through RLU (Reversible Logic Unit).


**Fig 3(a):** QCA cells of 1-bit adder

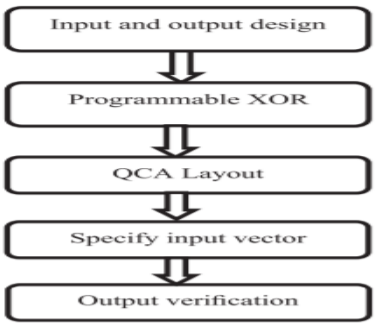



**Fig 3(b):** Flowchart representing adder process

### 4.2. Flowchart:

These following flowcharts explains about the performance made by the QCA tool kit. This flowchart in 3(b) represents 4-bit adder process and a vector input is given by a Lab View or Verilog Simulation Software [5]. Now coming to the simulation process, this process ends and output result is taken accordingly. The output comes in the form of sinusoidal waveforms.

The results are sum and carry for any circuit.

Sum= A0'B0'C0+A0B0C0'+A0B0C0+A0B0'C0'-(2)

Sum= A0 (B0C0'+B0'C0) +A0' (B0'C0+B0C0') – (3)

Sum = A0 **Θ** B0 **Θ**C0 **Θ** - (4) where **Θ= Ex-OR** function

Cout= (A0B0) + (B0C0) + (C0A0)-(5)

Equations (4) and (5) represent sum and carry of a 1-bit adder circuit. This is upgraded to 4-bit adder by using same logic using QCA cells and cascading four 1-bit adders forming a 4-bit adder.

### 4.3. 4-bit adder implementation in QCA cells:

In 4-bit Adder, the proposed Adder is arranged using QCA and PLD design using ALU technique. This can be considered for the full adder output carry and linking a chain towards the input carry of the next adder. First to prepare a 4-bit binary adder we have to have a ripple carry Si which is the sum of bits Ai and Bi. The input Carry in is connected to the next adder and propagates consequently to the end Cout. The proposed design is shown in 3(c).

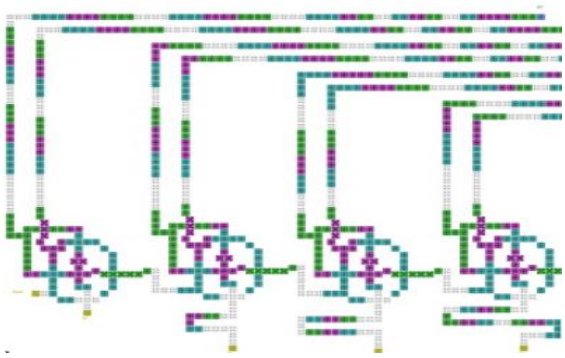


**Fig 3(c):** Proposed design of QCA cells in 4-bit adder

### 4.4. Logical and Arithmetic operations:

The designed 4-bit adder circuits which is dwelled by using QCA cells have arithmetic logic unit which does all the arithmetic operations like addition, multiplication, subtraction and division and the comparator operations too. The logical operations proposed by ALU does logical operations like AND, OR, NOT and, XOR. This 4-bit adder is composed of four ALU units connected or cascading four one bit adder.

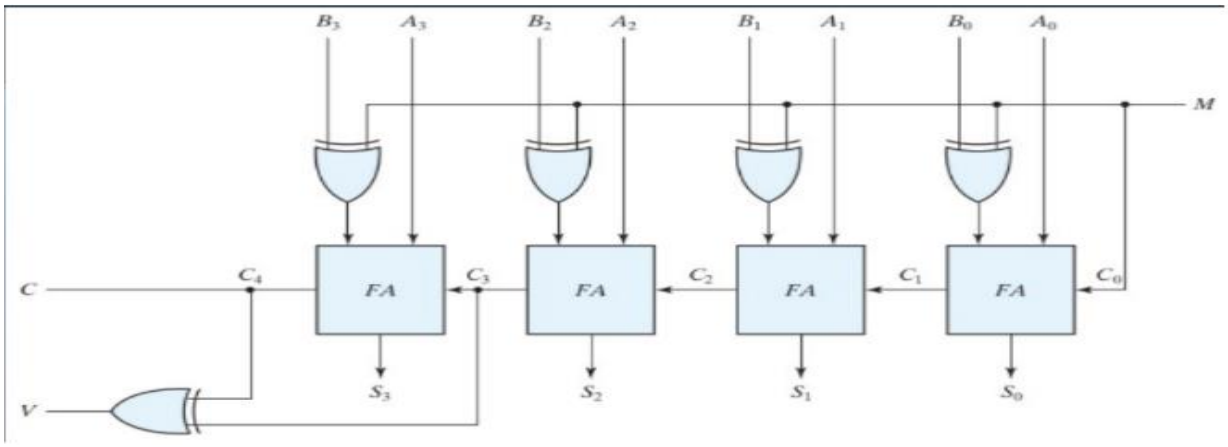



**Fig 3(d):** The schematic representation of 4-bit adders

## 5. RESULT/OUTPUT:

### A. 4-Bit Adder Simulation:

These results that are taken after simulation of the layout are shown in respective diagrams. Fig 4(a) shows the expected proposed 4-bit QCA cells whereas Fig 4(b) shows the expected input and output waveforms I of QCA cells simulations in simulation software like Lab View and Verilog simulated results.

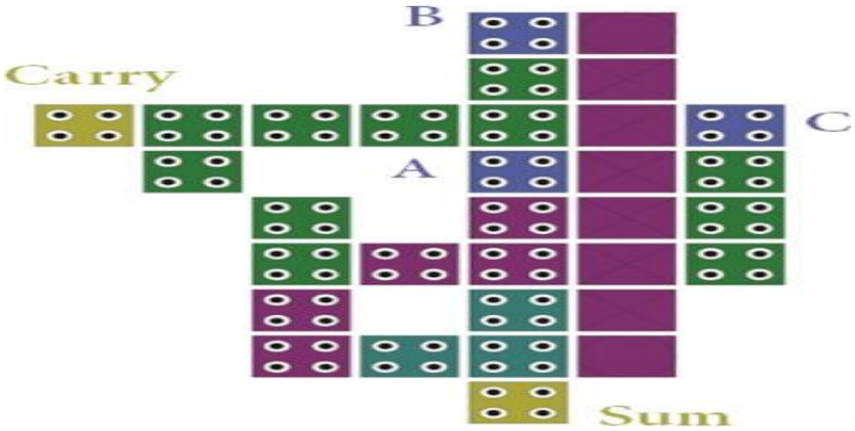
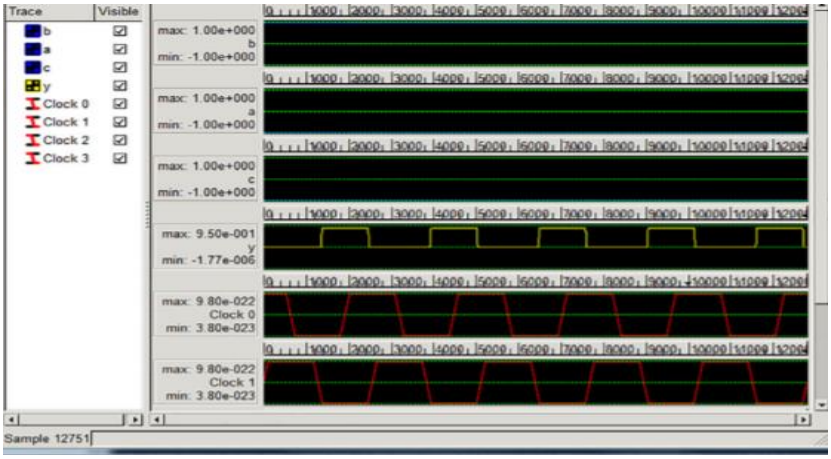



**Fig 4(a)**: expected proposed 4-bit QCA cells



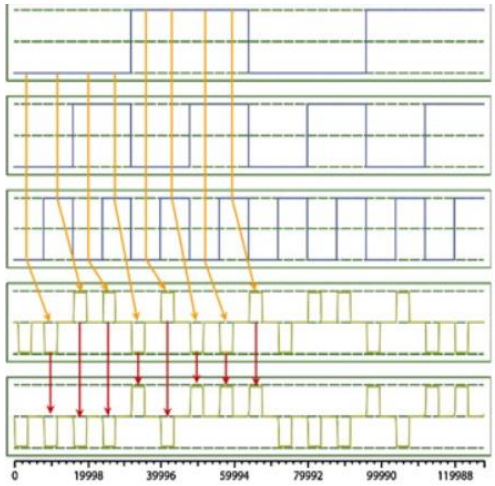



**Fig 4(b):** expected input and output waveforms done in Lab View Software and QCA Designer tool

It shows respective input and output waveforms of the particular QCA cells. Consider A, B, C as inputs and the output is considered as 'x'.The expected proposed 4-bit cell is being used by XOR design with the QCA cells. Cin acts as an enable input and Cout, n0, n1, n2, n3 acts as outputs for 4-bit adder circuits [3].These 4-bit adder circuits are called as ripple-carry adder circuit .This is a combination of all four 1-bit adder circuits integrated together.

## B. Polarization and temperature analysis:

While analyzing these circuits of 4-bit adder the presence of ALU plays an effective part. With the help of QCA cell it is important to know about this process as it is very interesting to know about the analysis of QCA cells .The main objective is to find a reversible universal gate (RUG) [2]. If we increase the temperature, the average output polarization decreases. This simulation is done practically or by other software like Lab View or QCA designer tool. Fig 4(c) shows the temperature v/s average output graph analysis. The curve is not linear and decreases upon some threshold/breakdown region.

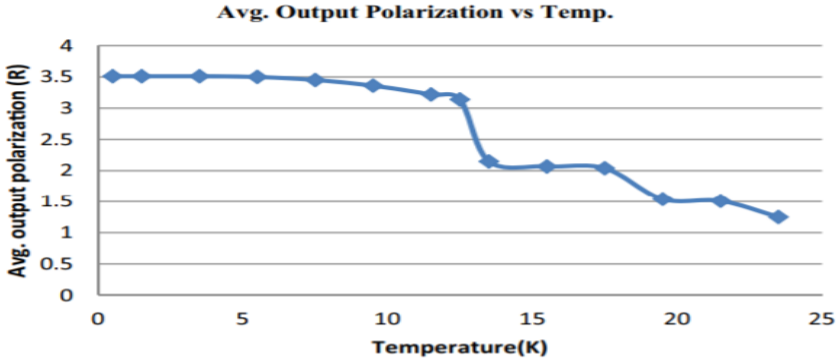



**Fig 4(c):** Temperature v/s avg.output polarization expected graph

## C. Comparison table of four bit adders:

The output or result of power dissipation and propagation delay is calculated from 4-bit adders and respectively compared with 1-bit adder ALU circuits with having two types of logic ,i.e.: CMOS and hybrid regions with the given logic .The respective comparison is shown in tabular column in fig 4(d).

| S.NO | Logic | ALU Based Design | Power dissipation | Propagation delay |
|---|---|---|---|---|
| 1 | CMOS | 4-Bit Adder | 2700nW | 54.2ns |
| 2 | Hybrid | 4-Bit Adder | 4100nW | 0.20 ns |
| 3 | CMOS | 1-Bit Adder | 73.2nW | 56.2 ns |
| 4 | Hybrid | 1-Bit Adder | 28.3nW | 0.018ns |

**Fig 4(d):** Comparison table of 4-bit ALU

## 6. FUTURE SCOPE IN THIS AREA:

Various techniques of QCA design are employed which includes 3 bit,4 bit ,5 bit binary to gray converter and gray to BCD converter are presented using ALU technique. This is useful in storing precise data and information through codes. Designing the layout circuits and simulating the proposed layout is done using QCA Designer tool. The proposed designs are done using minimum number of cells, with minimum clock delays. Some of the researches shows that the designs are area efficient and with high switching speed/velocity. The expected results are once checked by k-maps and verified by truth tables. QCA code converters logic circuits explains us detailing about the implementation. In near future these might help in minimizing error detection and leads to error free hardware units. ALU is basically used in all software applications and integration of QCA cells made integrate computer science domain with electronics domain in near future with the advancement in VLSI technique network around the globe.

## 7. CONCLUSIONS:

In the proposed work we have earlier discussed about the development of 4-Bit Adder circuits using QCA design by ALU technique which has provided a framework for advancement of 16-bit adders using VLSI technique. It had also confirmed the acceptability of the counter design of the circuit. This journal mainly speaks about various ALU techniques and how they are used to form a 4-bit adder circuit by many processes which include polarization. The circuits will hold the operation stability on hold and makes the QCA cells in ALU effective and sustainable thus being useful to majority of people around the world.

The given XOR gate carried out by QCA cells turned out to be a significant logic gate for composite QCA structure domain which further were fully utilized for complex configuration systems. The expected input and output waveforms were taken from the designer kit. The proposed methods uses very new complex values in Lab View. The proposed power and propagation delay of CMOS and normal ALU are calculated in a tabular column.

Thus, in this paper the main objectives of reversible ALU which all together had two domains name, i.e.: RLU and RAU which thoroughly justified by providing an area efficient model for 4 bit adder circuits design. This reflects the work that has more pros or advantages in the field of VLSI in the near future because of less power dissipation and efficient noise removal.

## 8. REFERENCES:

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