International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 08 Issue: 07 | July 2021 www.irjet.net p-ISSN: 2395-0072

"DESIGN AND IMPLEMENTATION OF HEALTH MONITORING SYSTEM IN ASIC FLOW USING CMOS 45 NM TECHNOLOGY"

SUSHMA K SATTIGERI[1], D.V. SRILEKHA[2], YASHASVI SURYAVAMSHI.K. S[3]

[1]Assistant Professor, Department of Electronics & Communication Engineering, Global Academy of Technology, Bengaluru, India
[2,3]Department of Electronics & Communication Engineering, Global Academy of Technology, Bengaluru, India

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ABSTRACT- *Due to the uncertain times such as this pandemic, it is important to keep trail of consumption. A certain number of people are disciplined on keeping a healthy diet whilst some of them are struggling and snacking more and not keeping up with a healthy diet. To check our body status, BMI (body mass index), BFP (Body Fat Percentage), BMD (Body Mineral Density), RMF (relative fat mass), BMR (basal metabolic rate) can be utilized as an indicator. Here we have analyzed BMI, BFP, BMD, RMF, BMR using elemental conditions like stature, weight, age, sexual inclination, abdomen circuit and so on. BMI can be used to screen for weight categories to check the health of an individual, BFP shows the fat in body, BMD exhibits minerals existing in body, RFM is viewed as obviously superior to BMI as it doesn't demonstrate about the fat mass, BMR shows the digestion pace. All the above-mentioned parameters are designed in Verilog language (RTL code) and it has been stimulated and physical design is carried out to get efficient analysis using Cadence tool*.

Key Words: 45NM, VERILOG code, Physical Design, GDS 2, floorplan, power plan, routing, Cadence, Xilinx

1.INTRODUCTION

Prior to the origination of VLSI technology, most ICs had a restricted set of functions they could perform. Electronic circuits consist of a CPU, ROM, RAM and various glue logic. VLSI allows IC designers to add these onto the chip.
Electronic fabrication units has leveled up, mostly due to the fast advances in large scale integration technologies and system design applications. With the advent of very large-scale integration (VLSI) designs, the number of applications of integrated circuits (ICs) in elevated-performance computing, controls, telecommunications, image & video processing, and consumer electronics has been evolvingg.
The present innovation in the technologies such as elevated resolution and low bit-rate video and mobile communications supplies the end-users a spectacular amount of applications, processing power.
This trend is expected to grow rapidly, with very important implications on VLSI design and systems design.

1.1 LITERATURE SURVEY

BMI is utilized as valuable occupants level proportion of overweight and weight. It is common for both men and women respectively. The BMI pointer analyses & displays the range of body weight to the square of body height of a person. As indicated by the BMI value, individuals can tell whether they are under-weight, reasonable weight or over-weight. BMI has been normalized by age and sex to characterize hunger and stoutness. BPF can be calculated using BMI. BFP of a person is the whole mass of fat cut-off by overall weight, duplicated by 100. Muscle versus fat includes necessary full & capacity body fat. RFM is approximation of weight in people that requires just calculation depending on the proportion of height and abdominal circumference estimations. Fat mass is known using two common approximation that is the height & waist circumference. BMI, RFM could be used in consistent clinical execution as an undeniable limit in assessing the body association.

1.2 METHODOLOGY

The methodology illustrates the flow of the code to be implemented. Comprehensively the flow chart is exhibited below where it explains various factors that are included in the code such as BMI, BMR, BMD, BFP, RMF, and how the formula is calculated and the code is designed.

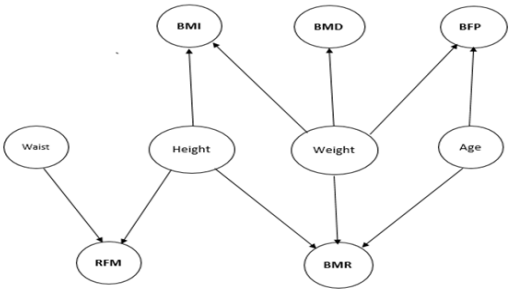


Fig1. Flow Diagram Methodology

2. RTL SCHEMATIC

Here a variable "a" is used to establish the sexual orientation, when a=0, it is assumed female or, it can be regarded as male. The set input will be taken as 8-bit in which w[7:0] will be the weight of the body measured in kilograms, h[7:0] will be the height in centimetres, [7:0]age will be the given age of the person, waist[7:0]BFP is((1.20**BMI)+ (0.23*Age) - (10.8*S)-5.4)), [7:0]RFM =(for male 64 – 20 × (tallness/abdomen circumference), for female 76 – 20 × (tallness/abdomen circumference)BMD is mapped out evidently from the weight approach of an established diagram. The final waveform of the Verilog code is obtained by using the Xilinx tool which simulates the code and gives the necessary result.

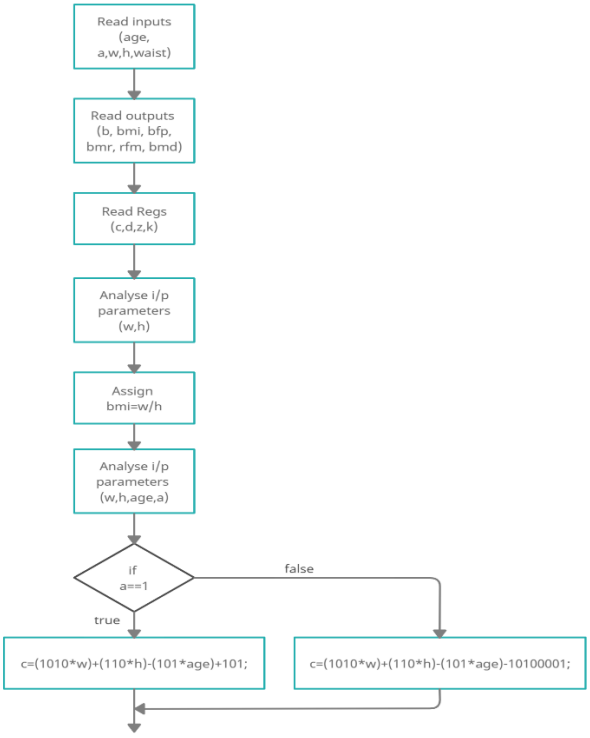


Fig 2.1 Flowchart of Verilog Code

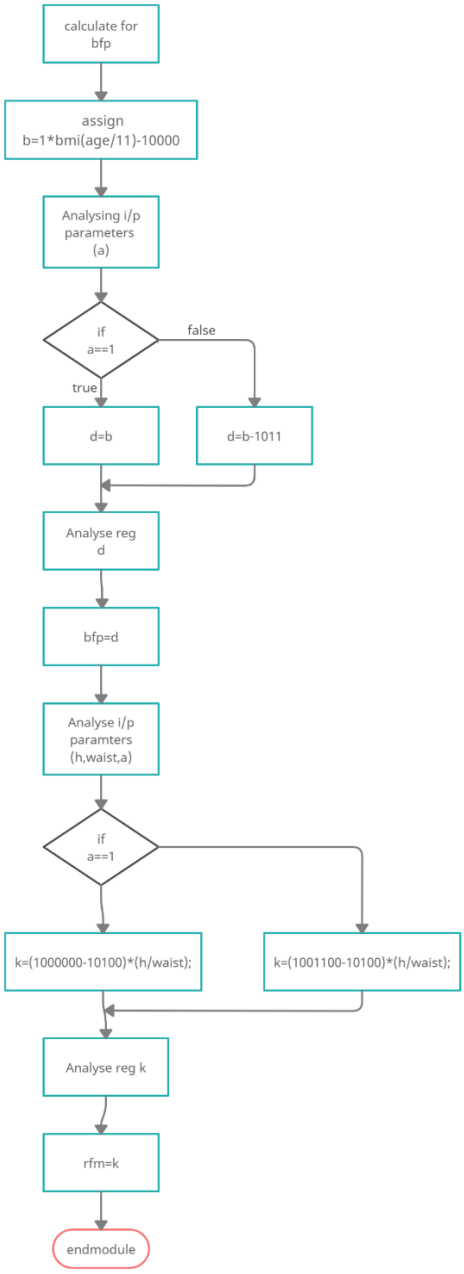
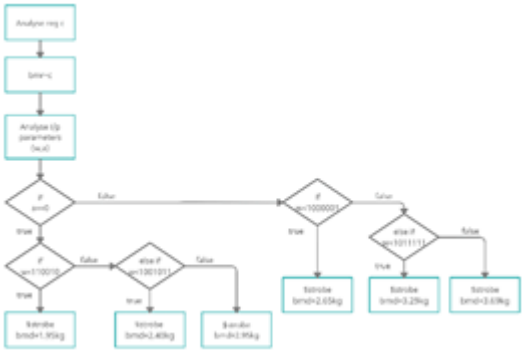


Fig 2.2 Flowchart of Verilog Code



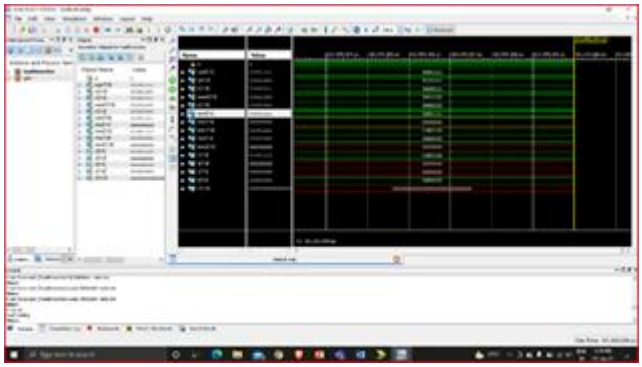


Fig 3. Simulated Waveform for The Verilog Code

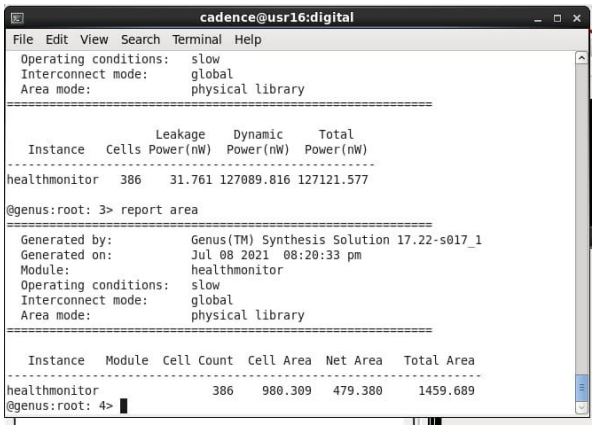


Fig 4. Area Report

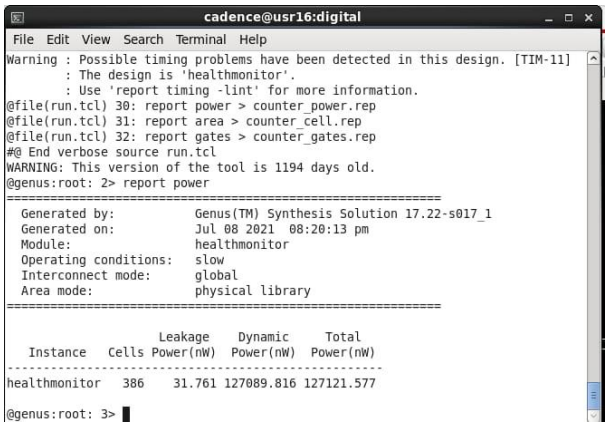


Fig 5. Power Report

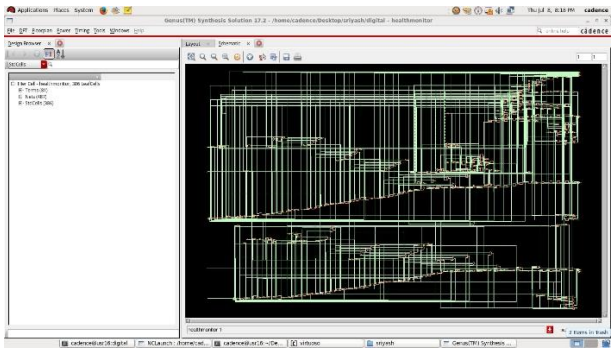


Fig 6. GUI Netlist

2.2 DESIGN OF HEALTH MOTITOR IN CADENCE PHYSICAL DESIGN FLOW

Physical design is the process of transforming a circuit explanation of the physical layout, which explains the position of cells and routes for the interconnections between the cells. The physical design contains many library & library exchange format files, Gate level netlist, synopsis design constraint file, Timing, Design rule violation. Clock design, technology files, Reports & scripts, GDS 2, CPF (Cadence Power Format) it is the power required to each gate will be defined, gates requiring same power.

In physical design, we follow series of procedures

FLOORPLAN: We estimate the die size to find the area required for the gate-level netlist to occupy. After the die size is evaluated, Pin Placement is done where input and output ports are connected with gates, later Macro Placement and Floor checkers are done.

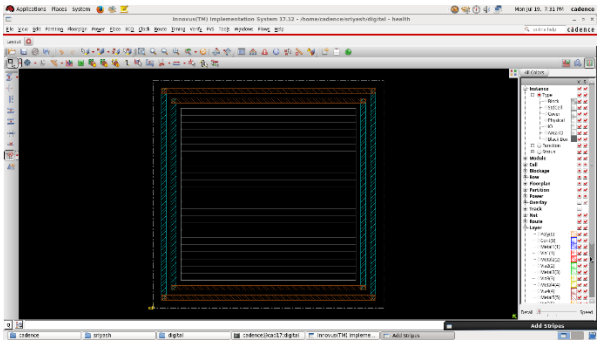


Fig 7. Floor plan

POWERPLAN: It is the phase where we provide or supply power to each gate. Here higher metals are used for power planning because the area in higher metals is more which means the resistance is less.

This includes three steps:

1) Global Net Connections: Here we declare all voltage sources required for our design that is vdd & vss.

2) Mesh/Ring generations: In mesh, the top, bottom, left & right metal will be selected which generates stripes inside. In-ring analysis generates rings around the core of vdd & vss making stripes run through the core from where macros get power from.

3) Standard cell Routing: Provides power to the standard cell between the rows in the core area.

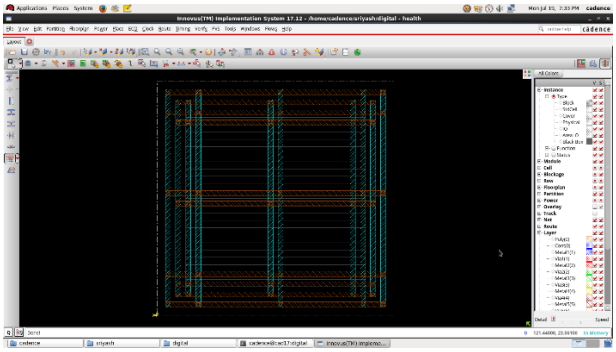


Fig 8. Power plan

PRE-PLACEMENT: It ensures that there is no functionality or connection.

PLACEMENT: It consists of three steps

a) Global Placement: It is randomly placing cells around the core area.

b) Refine Placement: It verifies area & timing consumption considers these areas, power & timing parameters, and places them accordingly in the core.

c) Placement Optimization: Reviews the refine placement status & optimizes area, power & time that it gets reduced more.

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------------------------------------------------------------
        timeDesign Summary
------------------------------------------------------------

Setup views included:
 Worst

+--------------------+---------+---------+
|     Setup mode     |   all   | default |
+--------------------+---------+---------+
|           WNS (ns):|  0.000  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |
|         All Paths:|    0    |    0    |
+--------------------+---------+---------+

+----------------+-----------------------------+------------------+
|                |             Real            |       Total      |
|    DRVs        +---------------+-------------+------------------+
|                | Nr nets(terms)| Worst Vio   | Nr nets(terms)   |
+----------------+---------------+-------------+------------------+
|   max_cap      |      0 (0)    |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)    |   0.000     |      0 (0)       |
|   max_fanout   |      0 (0)    |     0       |      0 (0)       |
|   max_length   |      0 (0)    |     0       |      0 (0)       |
+----------------+---------------+-------------+------------------+

Density: 68.466%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.25 sec
Total Real time: 0.0 sec
Total Memory Usage: 1175.597656 Mbytes
innovus 4>
```

Fig 9. Pre CTS-Timing Analysis

ROUTING: It is the stage after Clock Tree Synthesis and optimization where the exact paths for the interconnection of standard cells and macros and input pins are determined. The connections using metals and vias are created in the layout, defined by the logical connections present in the netlist.

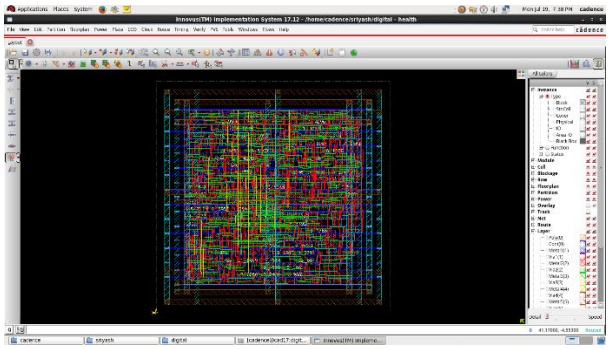

Fig 10. Routing

GDS 2: After post layout Simulation GDS 2 file will be generated.

6. CONCLUSIONS

This paper presents verification of health monitoring system in 45 NM technology using cadence tool. The frontend and backend procedure along with the performance evaluation of the Verilog code and Physical design was carried out. The performance criteria were area and power analysis were checked after routing and optimized results were obtained, after this, the process was carried up to GDS 2. It was observed that the WNS (worst negative slack) was zero which meant no violations were present and the technology used was efficient. The area and power parameters were analyzed and we got an optimized result with improved efficiency.

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