International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 08 Issue: 05 | May 2021 www.irjet.net p-ISSN: 2395-0072

Silicon Wafer Fault Detection by using Multiple Data Prediction

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Abstract - *The process monitoring and profile analysis are critical in detecting various abnormal events in semiconductor manufacturing, which consists of highly complex, interrelated, and lengthy wafer fabrication processes for yield enhancement and quality control. This study aims to develop a framework for semiconductor faults detection and classification (FDC) to monitor and analyze wafer fabrication profile data from a large number of related process variables to remove the cause of the faults and thus reduce abnormal yield loss. The purpose of this study was to develop a process management system to manage ingot fabrication and improve ingot quality. The ingot is the first manufactured material of wafers. The quality parameters were applied to evaluate the quality. Therefore, preprocessing was necessary to extract useful information from the quality data. First, statistical methods were used for data generation. The proposed framework can effectively detect abnormal wafers based on a controlled limit and the derived simple rules. The extracted information can be used to assist semiconductor faults diagnosis process recovery. The results demonstrate the practical applicability of the proposed approach.*

Key Words: **Classification, Accuracy, Artificial neural network, Artificial Intelligent, Prediction**

1.INTRODUCTION

A goal of semiconductor industries is to attain a high yield from all the wafers during the device location. Generally, to enhance the yield, uniform or systematic fault patterns serve as a guide to provide valuable feedback for engineers to identify the sources of faults. Yield loss may be attributed to many problems such as equipment malfunctions (process drift) or human mistakes. The existence of defects on the wafer may be seen as an indicator of these problems occurring, the detection of these problems accurately and early as possible becomes a crucial task. The manufacturing error by reflecting on the physical and electrical properties by wafer. Once the back end processing has been completed, wafers are subjected to a variety of electrical tests called “Parametric Tests” these tests require measuring the electrical parameters of the key devices that form the basic building blocks of all integrated circuits: resistors, capacitors, diodes, transistors, inductors, etc.

1.1 METHODOLOGIES

Based on experiments performed in this paper, a few wafer images exhibit multiple types of defects and have only a single label: this is a limitation of this dataset. From this dataset, only images with visible defects were chosen for the purpose of this paper. However, these wafer images were acquired from different lots with different image acquisition methods, so the raw images do not have a uniform definition of defects. Then, the contrast of the wafer area is enhanced before being binarized using threshold obtained via the KNN algorithm.

This operation is then followed by redefining the areas without defects as having the same grayscale value, while the defects are redefined using white pixels. The final step is to normalize the image to 256 × 256 pixels, while making sure that no white pixel is unintentionally removed by the normalization. About 75% of all the normalized images are used to train the convolution neural network, which include features extraction, features condensation, and classification.

The number of wafer images chosen for testing is 6312, and 40 images, 10 from each type of defect, were reserved for validation. The other method we investigated in this paper is the use of transfer learning on pretrained faster R-CNN models, which will be discussed later.

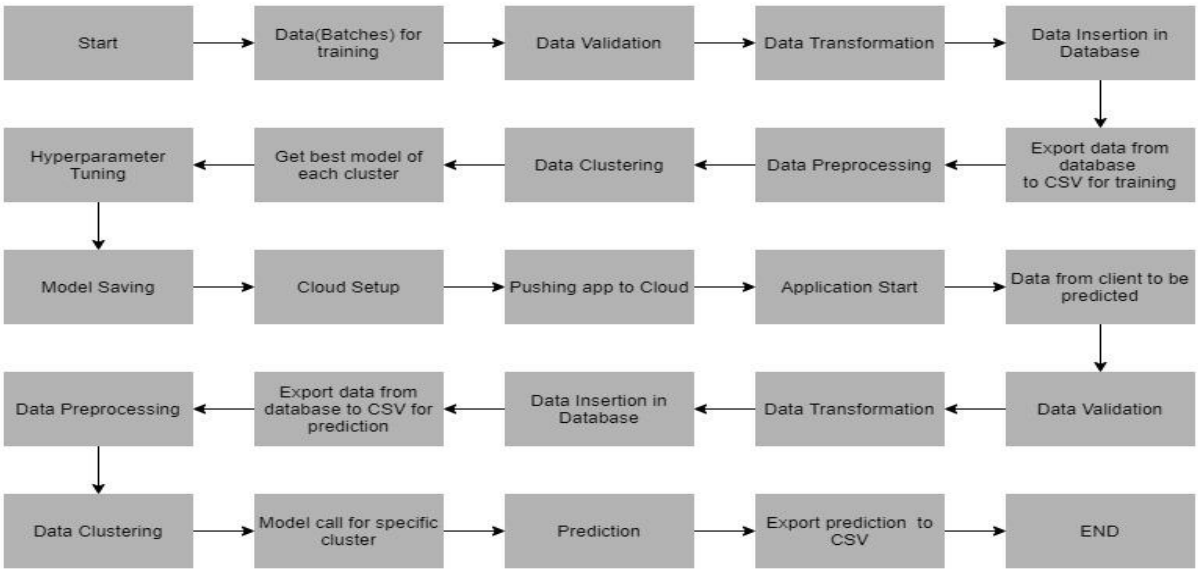

Fig: Classification Method

2. PROPOSED RESEARCH METHODOLOGY

In general, that manufacturing defects can be classified into three types: Type-A, Type-B, and Type-C.

Type-A defects are evenly random with a stable mean density. This type of defect is generated randomly, and no specific clustering phenomenon is visible, as shown in Figure 2a. The cause of this type of defect is complex and not fixed to particular patterns. It is difficult to find the cause of this type of defect. This type of yield abnormality can be reduced by improving the stability and accuracy of the process.

Type-B defects are systematic and repeatable from wafer to wafer. This type of defect has obvious clustering phenomenon, as shown in Figure 2b, c. The cause of this type of defect can usually be found by the distribution of defects on the wafer, which is used to find abnormalities in the process or machine, such as the misalignment of the mask position during photo development or excessive etching during the process, etc.

Type-C defects vary from wafer to wafer. This type of defect is the most common occurrence in semiconductor manufacturing. In this type of defect, it is very important to eliminate the causes for random defects and keep systemic defects, so that engineers can find the cause of anomalies.

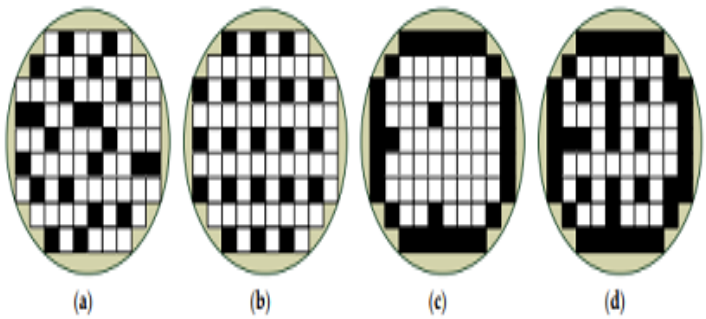

Figure 2. Wafer defects: (a) random defect, (b) repeatable defect, (c) systematic defect, and (d) combinational defect.

2.1 Comparisons and Validation

Comparisons will be made with other machine-learning-based classifiers presented in the literatures: SVM, logistic regression, random forest and weighted average (or soft voting ensemble).

The characteristics of these classifiers are:

• SVM is a well-known supervised classifier that performs by separating classes using hyper-planes, which are called support vectors.

• Logic regression is a variant extended from linear regression. The main algorithm of logistic regression is used in a binary classification algorithm to solve linearly separable problems.

• Random forest is an algorithm that integrates multiple decision trees, which is applied to the combination of various decision trees of different subsamples of the original data set.

• Unless otherwise specified, the default settings will be used for the above classifiers in the experiments. The validation will be done using 40 randomly chosen images that were not in the training or testing dataset. The result will show whether further training is required for the proposed CNN classifier.

2.2 Evaluation Measurements

The confusion matrix and the accuracy measure are used to present the classification results for ease of visualization. This measurement works the best when the number of classes is few. It presents the correct classified results along the diagonal entries in a tabular format. The incorrectly identified results are off the diagonal, and the class to which they were wrongly classified can easily be identified.

2.3 Data Description

The client will send data in multiple sets of files in batches at a given location. Data will have Wafer names and 590 columns of different sensor values for each wafer. The last column will contain the quot; Good/Bad & quot; value for each wafer. "Good/Bad" column will have two unique values +1 and -1.

& quot;+1" represents Bad wafer.

"-1" represents Good Wafer.

Except the training files, we also require & quot; schema & quot; file from the client, which contains all the relevant information about the training files such as:

The file name, Length of Date value in File Name, Length of Time value in File Name, Number of Columns, Name of the Columns, and their data type.

3. EXPERIMENT AND RESULT

In the experiments performed in this paper, 256 × 256 wafer images with defects were trained and classified into four classes, each with known causes, and compared with methods presented in previous studies: SVM, logistic regression, random forest and soft voting ensemble. Because the testing test sets are the same, the performance results can then be compared.

The result of this Paper, the use of the technology of transfer learning appears to be a feasible avenue of research in the future for wafer Fault classification.

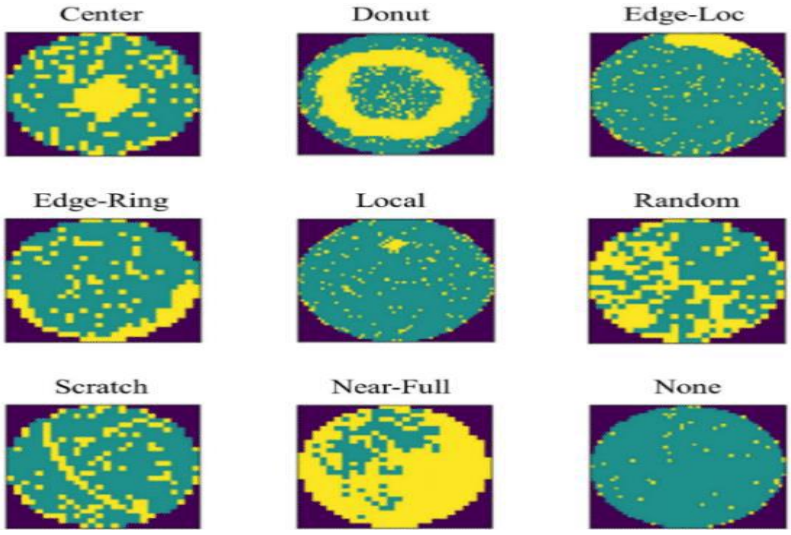

Fig: Wafer Fault Classes

The validation of the proposed CNN model was performed using 40 reserved wafer images, 10 from each defect class, and the result is shown in Table. It shows that 38 out of the 40 images were classified correctly. Two images, one in each of the center and local defects, appears to have been misclassified. A closer examination of these two misclassified images shows that they both exhibit multiple types of defect, yet only one type was labeled, as the example in Figure shows. The wafer image in Figure was labeled as a local defect, but both local and scrape-defect types can be observed. Since this study only included the four main types of defects and did not include mixed types, the two images were misclassified.

TABLE 1: EXPERIMENT VALIDATION RESULT

Fault Type	Sample Size	Accuracy
Center	10	93%
Local	10	71%
Random	10	96%
Scratch	10	77%

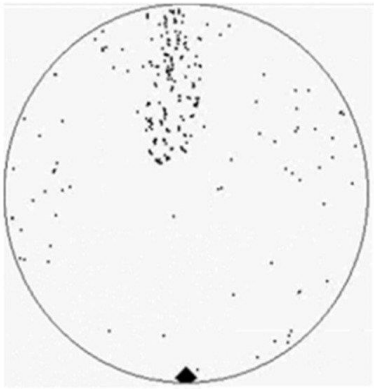

Fig: Wafer image exhibiting both scrap and local image type

3. CONCLUSIONS

The results of the experiments presented in this paper show that the use of convolution neural networks in classifying wafer images can be a feasible alternative to manual inspection and have been shown to perform well above other known machine-learning methods, such as SVM, logistic regression, random forest, and soft voting ensemble. However, the misclassification that occurred during the validation phase shows that the proposed design can be further improved. In future research, other defect types, including mixed types, should be added into the types of defects to be classified and, if possible, there should be an increase in the number of training samples used in future investigations.

ACKNOWLEDGEMENT

I would like to express my thanks of gratitude to my guide "Prof. Jayant Adhikari Sir" for their able guidance and support in completing my project. I would like to extend my gratitude to the "Prof. Priyanka Bhende Mam" and thanks to support your guidline "Dr. Narendra Chaudhari sir" & Our Principle & all professors for providing me with all the facility that was required.

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