

# High Step-Up Interleaved Boost Converter for Distributed Generation Using Renewable and Alternative Power Sources

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**Abstract** - This paper proposes a novel high step-up inter-leaved boost converter suitable for distributed generation using renewable and alternative power sources. The proposed inter-leaved boost converter not only lengthens the lifetime of the renewable power source by reducing the input-current ripple but also achieves high step-up conversion. In addition, the voltage stress of the main switches is lowered due to the lossless passive-clamp circuit. Hence, large voltage spikes across the main switches are alleviated and the efficiency is improved. Finally, a prototype circuit with an input voltage of 48 V, an output voltage of 380 V, and an output rated power of 3.5 kW are implemented and tested to demonstrate the functionality of the proposed converter. Moreover, satisfying experimental results are obtained and discussed in this paper; the measured full-load efficiency is 94.7%, and the highest measured efficiency of the proposed converter is 97.3%.

**Key Words**— High step-up conversion, interleaved boost converter, renewable and alternative power sources.

## 1. INTRODUCTION

For overcoming energy-shortage and environmental-contamination issues, renewable and alternative power sources that feature cleanliness and sustainability play an important role in the world, and have begun to be employed worldwide for environment protection [1]–[10]. The voltage levels of renewable and alternative power sources, such as photovoltaic cells and fuel cells, are generally low. Thus, high-step-up dc–dc converters have been widely utilized in such renewable energy systems in order to boost their voltage levels [11]–[15]. Fig. 1 shows a block diagram of a typical distributed generation using renewable and alternative power sources. The high step-up dc–dc converter can convert low levels of input voltage (typically 40~50V) from renewable sources into high levels of output voltages (typically 380~400V), which are then fed to a dc load or a dc–ac inverter for supplying ac

sources with an ac load. Hence, the high-step-up dc–dc converter with high efficiency is essential in such power-conversion systems.

The conventional step-up converters, such as the boost converter and flyback converter, obtain high voltage gain by adopting an extremely high duty cycle or high turns ratio of the coupled inductor. The circuit efficiency of these converters is limited due to the equivalent resistances or from the leakage inductance of windings, and high voltage spikes and stresses occur on the semiconductor devices. Adopting an extremely high duty cycle results in large conduction losses, serious diode reverse-recovery problems, and [25] electromagnetic interference issues. Because of the high voltage stresses that occur on the power devices, power switches with low  $R_{DS(ON)}$  and power diodes with low reverse-recovery time cannot be employed in this type of high-step-up converter.

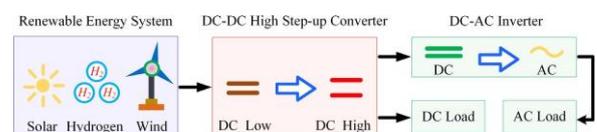


Fig. 1. Block diagram of a typical distributed generation using renewable and alternative power sources.

Some existing converters that utilize coupled inductors to achieve high-voltage conversion ratio, which recycle the leakage-inductance energy and lower the voltage stresses, have been proposed [16]–[20]. Interleaved converter with built-in transformer [21], [22] and interleaved converter with voltage multiplier module [23] or with coupled inductor [24] are another superior solution to obtain high step-up voltage gain and lower input current ripple. The coupled-inductor deals with large dc magnetizing current, so the volume

of core is larger and an air gap is required to avoid saturation of core; thus, the cost is higher and the efficiency is lower. On the other hand, the built-in transformer does not deal with large dc magnetizing current, and the voltage gain can be extended by increasing the turns ratio of the built-in transformer without an air gap; thus, the volume of core is smaller and the coupling coefficient as well as the circuit efficiency is higher. This paper proposes a novel high-step-up interleaved boost converter that not only utilizes the clamp capacitors but also integrates the secondary winding of the built-in transformer; thus, high step-up voltage gain of the presented converter and lower voltage stresses of the power devices are achieved.

The proposed interleaved boost converter with the features of high step-up conversion, high circuit efficiency, and low input-current ripple, which can lengthen the life time of the input source, is suitable for distributed generation using renewable and alternative power sources. In addition, windings of the built-in transformer can be designed to extend the step-up gain, and two diodes and two capacitors in the proposed converter act as an active clamp circuit in order to lower voltage stress on the main switches; thus, low-voltage-rated semiconductor devices (such as power MOSFETs and diodes) can be adopted in the presented converter. The key characteristics of the proposed converter are listed as follows:

- 1) lowering the input-current ripple and reducing the conduction losses result in an increased lifetime of the power sources and make the presented converter suitable for renewable and alternative energy applications;
- 2) the converter is capable of achieving high step-up gain easily;
- 3) by recycling the leakage energy, the voltage stresses of clamp diodes are alleviated and the circuit efficiency is improved;
- 4) the voltage stresses on the semiconductor components are substantially lower than the output voltage. Compared with the existing converter introduced in [21] and [22], the proposed high step-up converter decreases the power switch count and achieves similarly high circuit efficiency without soft-switching function and active clamp circuit. Moreover, the proposed converter has the features of cost-

effectiveness and relatively low input current ripple in comparison with that one presented in [23] and [24].

This paper is organized as follows. Section II describes and analyzes the proposed high step-up interleaved boost converter with built-in transformer. Section III analyzes the voltage gain, voltage stresses, and conduction losses in the presented converter. Section IV demonstrates the experimental results of a prototype circuit for supplying a 3.5-kW rated load. Finally, some conclusions are provided in Section V.

## 2. DESCRIPTION AND ANALYSIS OF THE PROPOSED HIGH-STEP-UP INTERLEAVED BOOST CONVERTER

The proposed high-step-up interleaved boost converter is shown in Fig. 2, where  $L_1$  and  $L_2$  are the energy storage inductors,  $S_1$  and  $S_2$  denote the power switches,  $C_1$  and  $C_2$  are the clamp capacitors,  $C_o$  is the output capacitor,  $D_1$  and  $D_2$  are the clamp diodes, and  $D_3$  and  $D_4$  are the rectified diodes. The built-in transformer consists of a primary winding  $N_p$ , a secondary winding  $N_{s1}$ , a third winding  $N_{s2}$ , and a leakage inductor  $L_k$ .

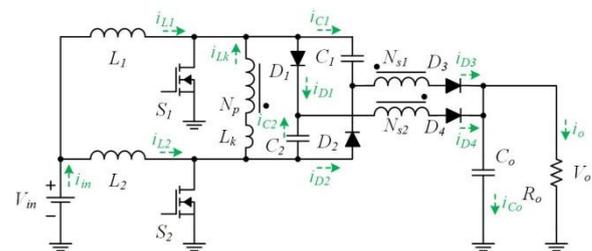


Fig. 2. Proposed high-step-up interleaved boost converter.

The gate-driving signals of the two power switches are interleaved with a 180° phase shift, and the theoretical waveform of the proposed converter operating in continuous-conduction mode (CCM) is shown in Fig.3.

Fig. 4 shows the corresponding operational modes of the equivalent circuit. There are ten main operational modes in one switching period. Due to the completely symmetrical interleaved topology, operating modes 1–5 and 6–10 are similar.

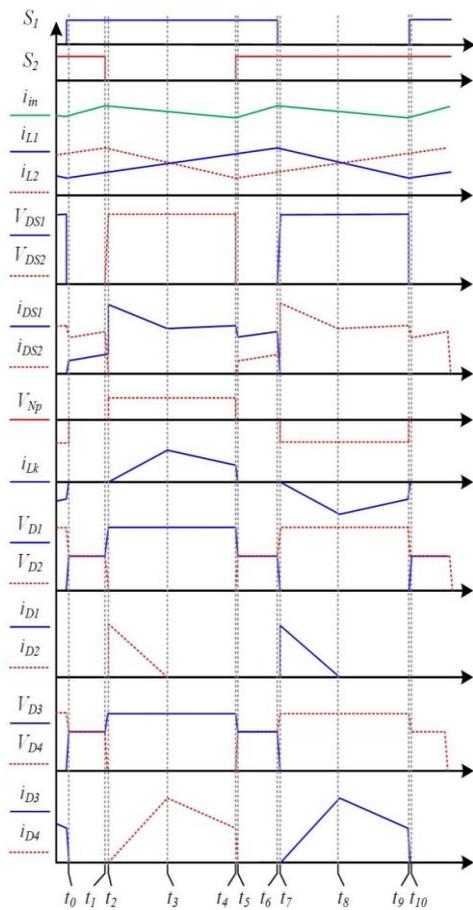
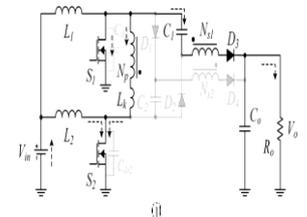
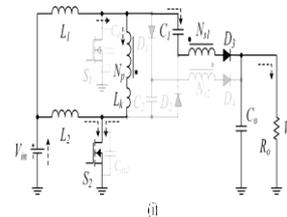
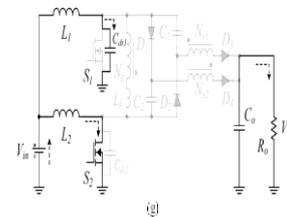
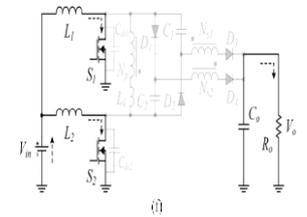
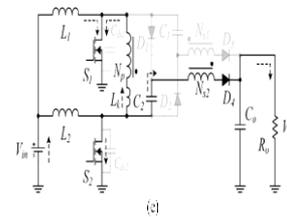
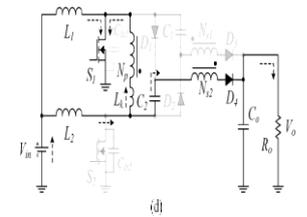
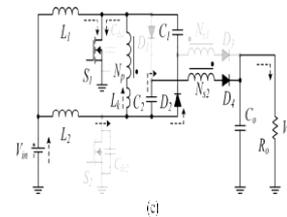
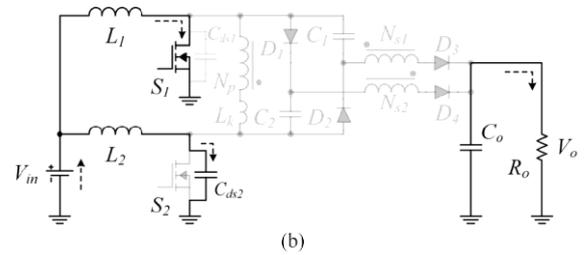
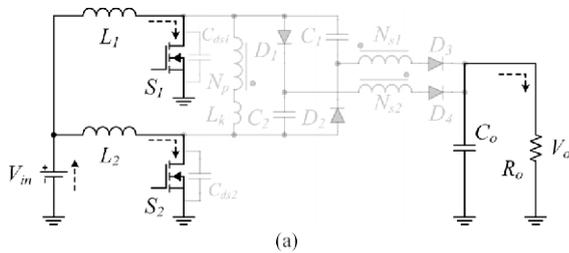


Fig. 3. Theoretical waveforms of the proposed converter operating in CCM.

In order to simplify the analysis of the proposed converter’s operating principle, only modes 1–5 are analyzed and dis- cussed. A detailed analysis of each operational mode in the proposed converter is shown in the following.



**A. Mode 1 [t<sub>0</sub>, t<sub>1</sub>]**

At t<sub>0</sub>, both power switches (S<sub>1</sub> and S<sub>2</sub>) turn ON. All the diodes (D<sub>1</sub>, D<sub>2</sub>, D<sub>2</sub>, and D<sub>4</sub>) are reverse-biased. The path of current flow is shown in Fig. 4(a). Inductors L<sub>1</sub> and L<sub>2</sub> are charged [29] by input voltage V<sub>in</sub>, and currents through inductors L<sub>1</sub> and L<sub>2</sub> linearly increase. The inductor currents i<sub>L1</sub> and i<sub>L2</sub> are, respectively, given by

$$i_{L1}(t) = I_{L1}(t_0) + \frac{V_{in}}{L_1} t \tag{1}$$

and

$$i_{L2}(t) = I_{L2}(t_0) + \frac{V_{in}}{L_2} t \tag{2}$$

where  $I_{L1}(t_0)$  and  $I_{L2}(t_0)$  are the initial values of the inductor currents.

**B. Mode 2 [ $t_1, t_2$ ]**

At  $t_1$ , power switch  $S_2$  turns OFF, and its parasitic capacitor is charged by inductor current  $i_{L2}$ . The path of current flow is shown in Fig. 4(b). The voltage of the parasitic capacitor is given by

$$V_{DS2}(t) = \frac{I_{L2}(t_1)}{C_{ds2}} t \quad (3)$$

**C. Mode 3 [ $t_2, t_3$ ]**

At  $t_2$ , power switch  $S_2$  remains OFF. The voltages of clamp diode  $D_2$  and rectified diode  $D_4$  decrease; then,  $D_2$  and  $D_4$  begin to turn ON at  $t_2$ . The path of current flow is shown in Fig. 4(c). The input voltage  $V_{in}$  and the inductor  $L_2$  provide energy to leakage inductor  $L_k$  and primary winding  $N_p$  through switch  $S_1$ , and to clamp capacitor [30]  $C_1$  through  $S_1$  and  $D_2$ . The drain-source voltage of power switch  $S_2$  is clamped by capacitor  $C_1$ . The input voltage  $V_{in}$ , inductor  $L_2$ , capacitor  $C_2$  and secondary winding  $N_{s2}$  provide energy to output capacitor  $C_o$  and to load  $R_o$  through  $D_4$ . The currents through  $L_2$ ,  $L_k$ , and  $S_1$  are, respectively, given by

$$i_{L2}(t) = i_{D2}(t) + (n+1) \cdot i_{D4}(t) \quad (4)$$

$$i_{Lk}(t) = n \cdot i_{D4}(t) \quad (5)$$

and

$$i_{DS1}(t) = i_{L1} + i_{D2}(t) + n \cdot i_{D4}(t) \quad (6)$$

**D. Mode 4 [ $t_3, t_4$ ]**

At  $t_3$ , power switch  $S_2$  is still OFF. The diode current  $i_{D2}$  decreases to zero, and the clamp capacitor voltage  $V_{C1}$  is equal to the drain-source voltage of power switch  $S_2$ . The path of current flow is shown in Fig. 4(d). [31] The rectified diode current  $i_{D4}$  is proportional to leakage-inductor current  $i_{Lk}$ . The currents through  $L_2$ ,  $L_k$ , and  $S_1$  are, respectively, given by

$$i_{L2}(t) = (n + 1) \cdot i_{D4}(t) \quad (7)$$

$$i_{Lk}(t) = n \cdot i_{D4}(t) \quad (8)$$

and

$$i_{DS1}(t) = i_{L1} + n \cdot i_{D4}(t). \quad (9)$$

**3. ANALYSIS OF VOLTAGE GAIN, VOLTAGE STRESS, AND CONDUCTION LOSSES**

To simplify the analysis of the presented converter operating in CCM, the transient characteristics of circuitry are disregarded, and small-ripple approximation issued for calculation; thus, all currents passing through the components are approximately represented by their [32]dc components. In addition, some formulated assumptions are as follows:

- 1) all components in the proposed interleaved boost con-

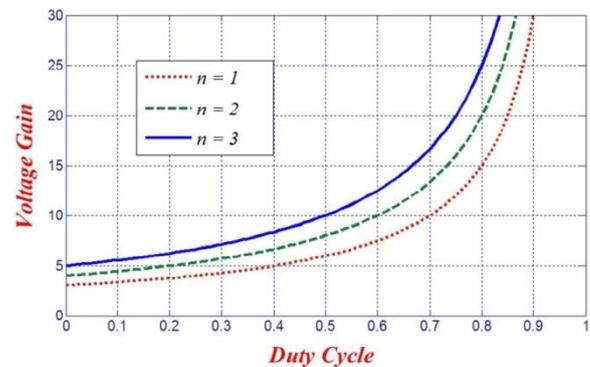


Fig.5. Voltage gain versus duty cycle in the proposed converter under different levels of turns ratio

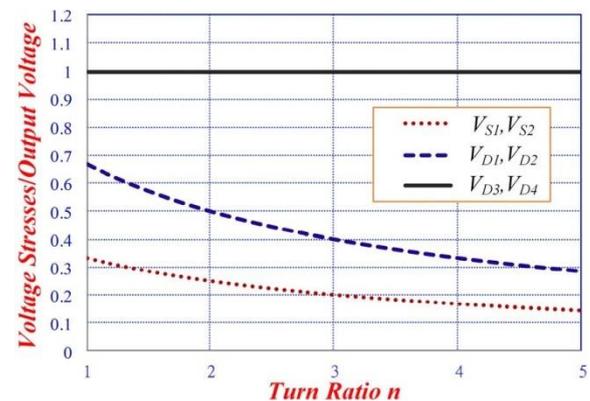


Fig. 6. Estimated voltage stresses on power switches and diodes.

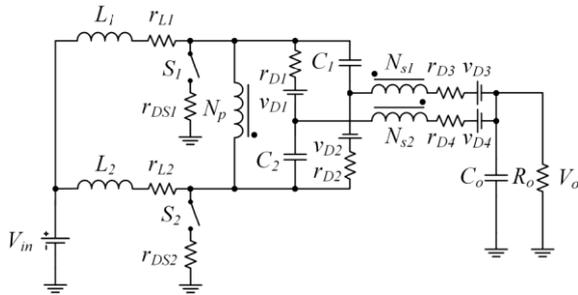


Fig. 7. Equivalent circuit for analyzing conduction losses in the proposed converter.

- 2) the coupling coefficient of the built-in transformer is unity; hence, there is no leakage inductor in either the primary or secondary side of the transformer;
- 3) Voltages on capacitors and currents through the inductors are considered to be constant due to infinitely large capacitances and inductances;
- 4) due to the symmetrically interleaving structure and operation, the symmetrical circuit components with the same characteristics and effects are defined by identical symbols, for example,  $D_1$  and  $D_2$  are defined as  $D_c$ ;  $D_3$  and  $D_4$  are defined as  $D_f$

### A. Voltage Gain

The voltage on clamp capacitors  $C_1$  and  $C_2$  can be expressed as

$$V_{C1} = V_{C2} = \frac{1}{1-D} V_o \quad (11)$$

The voltages on output capacitor  $C_o$  can be derived from

$$V_{C_o} = \frac{2+n}{1-D} V_o \quad (12)$$

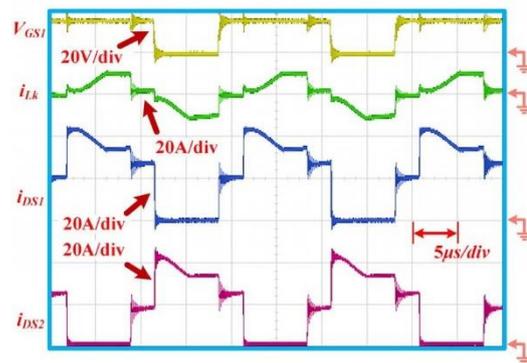
The output voltage  $V_o$  is given by

$$V_o = V_{C_o} = \frac{2+n}{1-D} V_{in} \quad (13)$$

In addition, the voltage gain of the proposed converter is described as

$$\frac{V_o}{V_{in}} = \frac{2+n}{1-D} \quad (14)$$

Equation (14) confirms that the proposed converter has a high step-up voltage gain without an extremely high duty cycle or large turns ratios for the transformer. The curve of the voltage gain related to duty cycle in the proposed converter, under different turns ratio levels for the built-in transformer, is shown in Fig. 5, where  $n$  represents  $N_s/N_p$



(c)

### B. Voltage Stress

The voltage stresses on power switches  $S_1$  and  $S_2$  are clamped, and are derived from

$$V_{DS1} = V_{DS2} = \frac{1}{1-D} V_o \quad (15)$$

The voltage stresses on diodes  $D_1$ ,  $D_2$ ,  $D_3$ , and  $D_4$  are, respectively, given by

$$V_{D1} = V_{D2} = \frac{2}{1-D} V_o \quad (16)$$

and

$$V_{D3} = V_{D4} = V_o = \frac{2+n}{1-D} V_{in} \quad (17)$$

Equations (15)–(17) confirm that the proposed converter has low voltage stresses on its semiconductor components, and hence, low-voltage-rated power devices, such as MOSFETs with low  $R_{DS(ON)}$  and Schottky diodes without reverse-recovery time, can be employed for improving circuit efficiency. With a duty cycle of 0.5, the estimated voltage stresses on power switches and diodes in relation to turns ratio  $n$  are shown in Fig. 6. As

illustrated, low voltage stress occurring on the power switches is one of the principal advantages in the proposed converter.

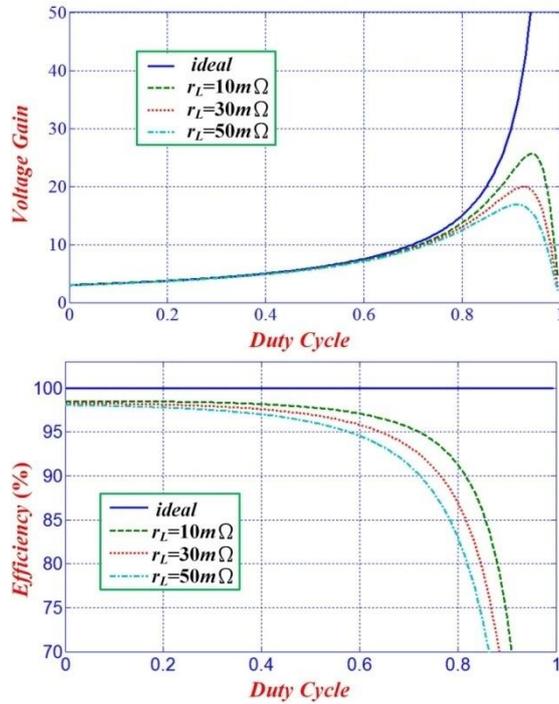
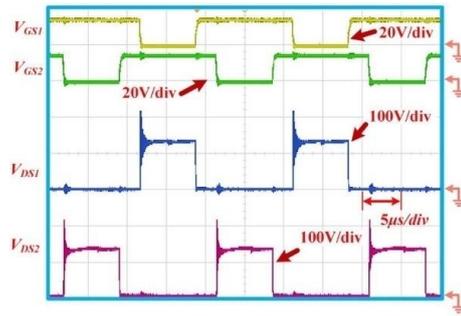
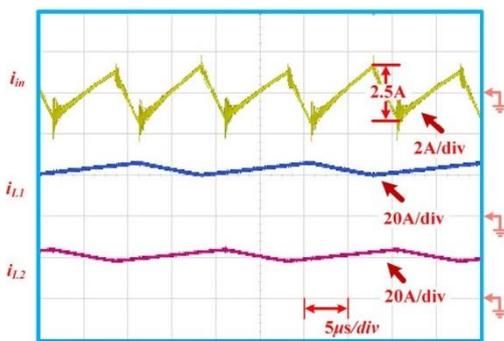
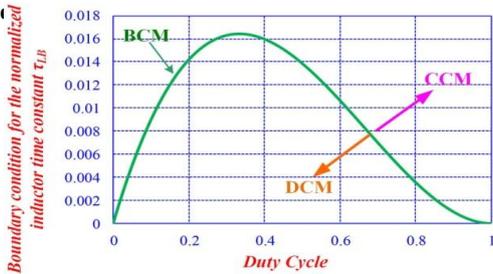
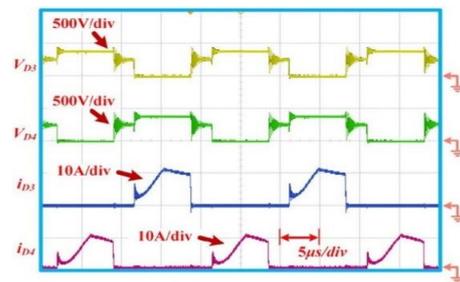


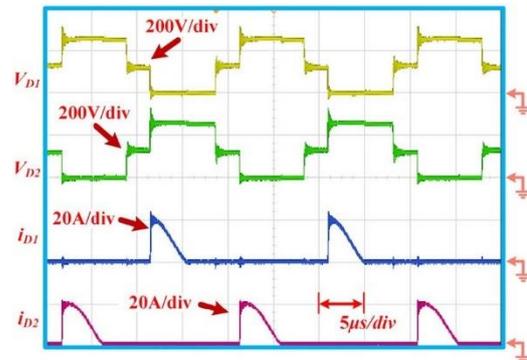
Fig. 8. Calculated voltage gain and circuit efficiency versus duty cycle at different  $r_L$  values under a full-load condition ( $R_o$  41  $\Delta$ ), inclu



(b)



(c)



(d)

### c) Conduction Losses

The equivalent circuit for analyzing conduction losses of inductors and semiconductor components in the proposed Fig. 9. Relationship between boundary condition for the normalized inductor time constant  $\tau_{LB}$  and duty cycle. converter is shown in Fig. 7, in which  $r_{L1}$  and  $r_{L2}$  are the copper resistances of the inductors,  $r_{DS1}$  and  $r_{DS2}$  denote the resistors  $R_{DS(ON)}$  of power MOSFETs,  $V_{D1}$ ,  $V_{D2}$ ,  $V_{D3}$ , and  $V_{D4}$  denote the forward-biased voltages of the diodes, and  $r_{D1}$ ,  $r_{D2}$ ,  $r_{D3}$ , and  $r_{D4}$  are the resistances of the diodes. Due to the symmetrically interleaving structure and operation, symmetrical components with the same characteristic are defined by identical symbols in (18) and (19); for

instance,  $r_{L1}$  and  $r_{L2}$  are defined as  $r_L$ ;  $r_{Dc}$  is the equivalent resistor of diodes  $D_1$  and  $D_2$ ;  $V_{Dc}$  denotes the voltage of  $V_{D1}$  and  $V_{D2}$ ;  $r_{Df}$  is the equivalent resistor of diodes  $D_3$  and  $D_4$ ;  $V_{Df}$  denotes the voltage of  $V_{D3}$  and  $V_{D4}$ . Small-ripple approximation is used to calculate conduction losses. Thus, all currents passing through the components are approximately represented by their dc components. The magnetizing currents and capacitor voltages are assumed to be constant because of the infinite values of the magnetizing inductors and capacitors. Finally, by using voltage-second balance and capacitor-charge balance theorems, the voltage conversion ratio, including the conduction losses of power devices, can be derived from The calculated voltage gain and circuit efficiency versus duty cycle at different  $r_L$  values under a full-load condition

$$V_o = \frac{+n}{1-D} \cdot \frac{VD_c + VD_f}{V_{in}} \quad \text{Voltage Stress}$$

$$R_o = \frac{2 \cdot R_{L1} + 2 \cdot R_{L2} + 2 \cdot R_{Dc} + 2 \cdot R_{Df}}{(1-D)^2} + \dots$$

Where

$$r_{L1} = (2+n)^2 \cdot r_L$$

$$r_{L2} = [(2D-1)(2+n)^2 + (1-D) \cdot (2n+3)^2] \cdot r_L$$

And

$$r_{Dc} = r_{D1} + r_{D2}$$

In addition, the circuit efficiency is expressed by

$$\eta = \frac{V_o \cdot I_o}{V_{in} \cdot I_{in}} = \frac{(1-D) \cdot (VD_c + VD_f)}{2+n} \cdot \frac{I_o}{\frac{2+n}{1-D} \cdot I_o} \cdot \frac{1}{\left[ \frac{r_{L1} + r_{L2} + r_{Dc} + r_{Df}}{R_o} + 1 \right]} \quad (19)$$

$(R_o = 41 \text{ } \blacktriangle \text{ with } V_{Dc} = V_{Df} = 0.7 \text{ V}; r_{Dc} = r_{Df} = 20 \text{ m}\blacktriangle; \dots)$

power devices, is shown in Fig. 8. As illustrated, it is easy for the proposed converter to achieve high step-up voltage conversion, and the converter is suitable for renewable energy applications.

### D. Design Consideration

In the proposed high step-up interleaved boost converter, the input current  $I_{in}$  and the ripple current  $Oi_L$  of the inductor are represented by

$$I_{in} = \frac{2+n}{1-D} \cdot I_o = \frac{2+n}{1-D} \cdot \frac{V_o}{R_o} \quad (20)$$

TABLE I

VOLTAGE/CURRENT STRESSES OF MAIN POWER DEVICES IN THE PROPOSED CONVERTER

Main Power Devices	Voltage Stress	Current Stress
Power Switches $S_1$ and $S_2$	$\frac{1}{2+n} \cdot V_o$	$\frac{(1+n+D) \cdot I_o}{2 \cdot D \cdot (1-D)}$
Power Diodes $D_1$ and $D_2$	$\frac{2}{2+n} \cdot V_o$	$\frac{I_o}{2 \cdot (2-D)}$
Power Diodes $D_3$ and $D_4$	$V_o$	$\frac{I_o}{2 \cdot (2-D)}$

TABLE II  
ELECTRICAL SPECIFICATIONS

Components	Parameters
Input Voltage $V_{in}$	48 V
Output Voltage $V_o$	380 V
Switching Frequency $f_s$	50kHz
Maximum Power $P_o$	3.5kW
Duty Ratio $D$	0.62
Main Switches $S_1$ and $S_2$	IRFP4227(200V/130A)
Diodes $D_1$ and $D_2$	MBR20200(200V/20A)
Diodes $D_3$ and $D_4$	MUR1640(400V/16A)
Capacitors $C_1$ and $C_2$	10µF
Output Capacitor $C_o$	120µF
Filter Inductors $L_1$ and $L_2$	110µF
Turn Ratio $N_s/N_p$	1:1

and

$$O_{iL} = \frac{V_{in} \cdot D}{f_s \cdot L_1} = \frac{V_{in} \cdot D}{f_s \cdot L_2} \quad (21)$$

The relationship between input current  $I_{in}$  and the ripple current  $O_{iL}$  of the inductor in boundary-conduction mode are given by

$$\frac{I_{in}}{2} = \frac{O_{iL}}{2} \quad (22)$$

Substituting (20) and (21) into (22), the boundary condition for the normalized inductor time constant which is represented by  $\tau_{LB}$ , is expressed by

$$\tau_{LB} = \frac{L_1}{R_o} \cdot f_s = \frac{L_2}{R_o} \cdot f_s = \frac{D \cdot (1 - D)^2}{(2+n)^2} \quad (23)$$

The design considerations of the proposed converter include component selection and inductor design, both of which are based on the analysis presented in Section III. In the proposed converter, the secondary windings ( $N_{s1}$  and  $N_{s2}$ ) of the built-in transformer are set as close as possible for obtaining current-sharing performance on output diodes  $D_3$  and  $D_4$ . Because the proposed converter possesses high step-up gain, the turns ratios can be set as 1 for the prototype circuit, thus reducing cost, volume, and conduction losses of the windings inside the built-in transformer.

Fig. 9 shows the relationship between the boundary condition for the normalized inductor time constant  $\tau_{LB}$  and duty cycle  $D$  under a turns ratio  $n$  of 1 according to (23), and Fig. 9 is a design guideline for selecting appropriate inductors  $L_1$  and  $L_2$  of the presented converter.

Fig. 10 shows the experimental waveforms at a load of 2 kW. Fig. 10(a) shows the interleaved pulse width modulation signals  $V_{GS1}$  and  $V_{GS2}$ , as well as the voltage stresses on the power switches. In addition, the typical value of repetitive avalanche voltage of the utilized power switch is 240 V. Although voltage spikes occur on main switches  $S_1$  and  $S_2$  (caused by the resonance of the leakage inductors in the primary side of the built-in transformer and  $C_{DS}$  of the MOSFETs), the utilized power MOSFETs are capable to sustain the voltage spikes across the switches in Fig. 10(a). Fig. 10(b) shows the ripple of input current  $i_{in}$  this means that current-sharing is achieved in the secondary windings of the built-in transformer in the presented converter. In addition, the input current  $i_{in}$  with dc part magnitude) is the sum of inductor currents  $i_{L1}$  and  $i_{L2}$ .

Fig. 10(c) shows the leakage-inductor current  $i_{Lk}$  as well as currents through power switches  $S_1$  and  $S_2$ . Fig. 10(d) shows

In addition, voltage stresses and current stresses of main power devices (including power switches and diodes) in the proposed converter are shown in Table I.

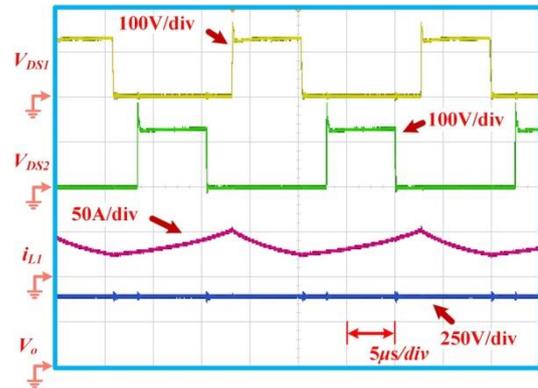


Fig.11. Measured waveforms  $V_{DS1}$ ,  $V_{DS2}$ ,  $i_{L1}$ , and  $V_o$  at a full load of 3.5kW.

#### 4. EXPERIMENTAL RESULTS

A 3.5-kW prototype circuit of the proposed high-step-up converter has been built and tested. The electrical specifications for the presented converter are shown in Table II.

The measured voltage and current waveforms of diodes  $D_1$  and  $D_2$ . The voltage stresses on diodes  $D_1$  and  $D_2$  are equal to  $V_{DS2}$  plus  $V_{C2}$  and  $V_{DS1}$  plus  $V_{C1}$ , respectively. Fig. 10(e) shows the measured voltage and current on diodes  $D_3$  and  $D_4$ , and the voltage stresses on diodes  $D_3$  and  $D_4$  are both equal to  $V_{Co}$ . The currents  $i_{D3}$  and  $i_{D4}$  decrease to zero with very light reverse-recovery losses for the diodes. The ringing effect of diode voltages, shown in Fig. 10(c)–(e), is caused by the resonance of the parasitic inductors in the circuit, the leakage inductors of the transformer in the primary and secondary sides, and the junction capacitors of the diodes. Fig. 11 shows the measured waveforms of voltages  $V_{DS1}$ ,  $V_{DS2}$ ,  $V_o$ , and current  $i_{L1}$  at a full load of 3.5 kW. Fig. 12 shows the photo

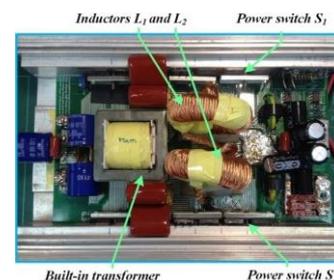


Fig. 12. Photo of the presented converter

of the presented converter, and some key components are marked. Fig. 13 shows the temperature distribution in the proposed converter at a full load of 3.5 kW by using a true infrared thermal imager (Agilent U5855A); the measured maximum and minimum temperatures are 65.4°C and 29.5°C, respectively

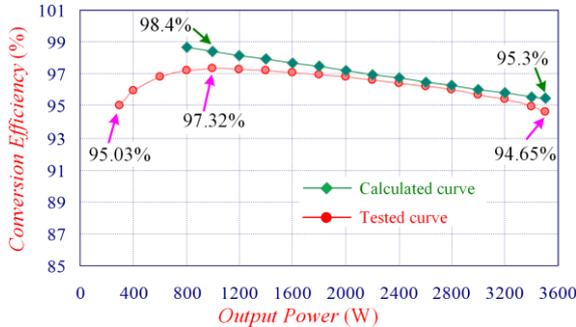


Fig. 15. Calculated and tested curve of circuit efficiency versus output power in the proposed high-step-up converter

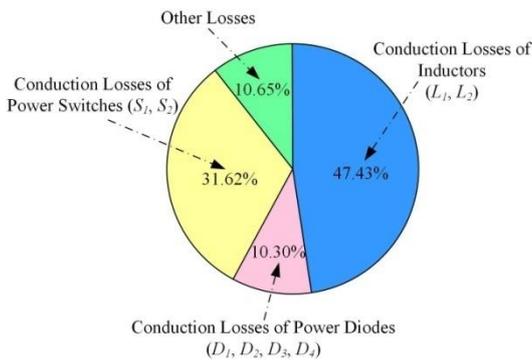
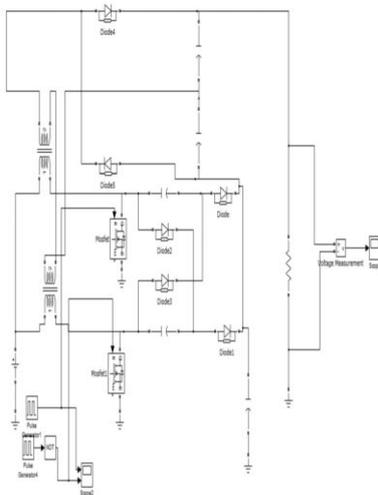


Fig. 16. Pie graph of loss breakdown in the presented converter.



analyzer (HIOKI 3390). The calculated (in CCM condition with  $V_{Dc} V_{Df} 0.7 V$ ;  $r_{Dc} r_{Df} 20 m\Omega$ ;  $r_{ds} 20 m\Omega$ ;  $r_L 30 m\Omega$ ) and tested curve of circuit efficiency versus output power in the proposed high-step-up converter are shown in Fig. 15. The measured efficiency at a full-load condition (3.5 kW) is 94.65%, which is very close to the calculated one (95.3%) at a duty cycle of 0.62. In addition, the measured efficiency at a 1-kW load (approximately one-third full-load) is about 97.32%, which is close to calculated one (98.4%) at a duty cycle of 0.62. Moreover, the measured efficiency of the light-load (300 W) is 95.03%.

Fig. 16 shows the pie graph of loss breakdown in the presented converter. The percentages of conduction losses of power switches ( $S_1$  and  $S_2$ ), power diodes ( $D_1, D_2, D_3$ , and  $D_4$ ), and inductors ( $L_1$  and  $L_2$ ) are 31.62%, 10.3%, and 47.43%, respectively. It can be seen that the dominant losses in the presented converter are the conduction losses of the power devices (including power switches, power diodes, and inductors), whose percentages are 89.35% of total losses. In addition, the percentages of other losses (including switching loss of MOSFETs, reverse recovery loss of diode, magnetic core loss, and so on) are 10.65%.

In addition, Table III shows the comparisons between the existing high step-up converters [22]–[24] and the proposed one in this paper. As shown in Table III, the proposed high step-up converter without soft-switching function has the advantages of cost-effectiveness and similar performance of the measured full-load efficiency in comparison with the converter introduced in [22]. In addition, the proposed converter has the advantages of cost-effectiveness, relatively low

TABLE III  
COMPARISONS BETWEEN THE EXISTING HIGH STEP-UP CONVERTERS [22]–[24] AND THE PROPOSED ONE

Topology	Converter in [22]	Converter in [23]	Converter in [24]	Proposed Converter
Voltage Gain	$\frac{2-2n}{1-D}$	$\frac{2+2n}{1-D}$	$n_2 + 1 + \frac{2n_2 D + 1}{1-D}$	$\frac{2+n}{1-D}$
Quantities of Power Switches	4	2	2	2
Quantities of Diodes	4	6	6	4
Quantities of Magnetic Cores	3	2	2	3
Quantities of Capacitors	3	5	5	3
Soft Switching	ZVS	No	No	No
Input Current Ripple	Very Small	Small	Small	Very Small
Converter Specifications	40V to 380V	60-90V to 400V	48V to 380V	48V to 380V
Measured Full-Load Efficiency	95.8% at 1kW	91.32% at 2kW	92.6% at 2kW	94.65% at 3.5kW

input current, and high full-load efficiency in comparison with the converters presented in [23] and [24].

### 5. CONCLUSION

This paper has proposed a high-step-up interleaved boost converter for distributed generation using renewable and alternative power sources. The analysis of operational modes, voltage gain, and stresses is provided, and a 3.5-kW prototype converter has been developed and tested. The interleaved structure inside the presented converter reduces the input-current ripple and distributes the current through each component. In addition, the lossless passive-clamp circuit recycles the leakage energy and constrains voltage spikes across power switches. Furthermore, the measured full-load efficiency is 94.7% at a rated output power of 3.5 kW, and the highest efficiency is 97.3% at an output power of 1 kW. Consequently, satisfactory experimental results have demonstrated the functionality of the proposed converter with the advantages of high step-up voltage gain, high efficiency, and suitability for renewable and alternative energy applications.

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