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Comparison of 9-level Cascaded Multilevel Inverter using Multicarrier Pulse Width Modulation Techniques

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Abstract – This manuscript presents the achieved efforts on 1-ϕ 9-level cascaded H-bridge multilevel inverter. To cheer the quality of 9-level CHBMLI output parameters primarily THD and switching losses, multicarrier level shifted technique is consider for controlling the gate pulse of 9-level CHBMLI and the complete analysis of THD for 9-level is done. This work is performed and results are validated using MATLAB/SIMULINK.

Keywords: Multilevel Inverter (MLI), Cascaded H-Bridge (CHBMLI), Multicarrier pulse width modulation technique (MCPWM).

1. Introduction

Multilevel inverter (MLI) is playing a important role in the field of medium and high voltage industries. The design of MLI is mainly depends on number of DC supplies, number of switches, voltage levels, DC link capacitors and output power quality. Most of the MLI are subdivided into three main categories flying capacitor (FC), neutral point clamped (NPC) and the cascaded H bridge (CHB). CHB MLI is very commonly used in industrial application and has a reliable structure when compare to others. CHB MLI is very beneficial with low dv/dt stress, less total harmonic distortion (THD) and less electromagnetic interference (EMI) among all of them CHB MLI is very suitable for PV array application because each panel of CHB MLI operates with separate DC voltage sources there are very large number of techniques to control the various operations MLI such as space vector pulse width modulation (SVPWM) and sinusoidal pulse with modulation (SPWM) etc and to control the output voltage of multilevel inverter; carrier based PWM is one of them. It is a so called sine triangle PWM; as a reference is sine wave and carrier is triangular wave. Level shifted method is a type of sine PWM technique and it has three types, namely: In this paper simulation of 9-level CHBMLI is done using level shifted PWM technique for single phase, and there THD is analyzed.

2. MULTILEVEL INVERTER(CHBMLI)

Fig. 2 deprived the basic layout of CHBMLI for single phase. Every splitting voltage source (V_{dc1}, V_{dc2}, V_{dc3}) associated in cascade through additional supply via a unique H-bridge circuit linked through it. Every circuit contains four switches that can create the voltage output source in positive or negative polarity; or it can be simply zero volts depending on the switching condition of the switches in the circuit [1, 2].

The level of output can be given by

$$N_{level} = 2S + 1 \qquad (1)$$

Where, *S* is the H-bridge

The voltage at every phase can be calculated by

$$V_{out} = 1V_{dc} \ (n = 1,2,3 \dots) \quad (2)$$

The number of switches used in this topology is given by the equation,

$$N_{switches} = 4S \quad (3)$$

The rewards of the CHBMLI are series H-bridges for modularized outline and wrapping. The Fig 3 demonstrates the waveform of voltage output for a 7-level CHBMLI [7, 8].

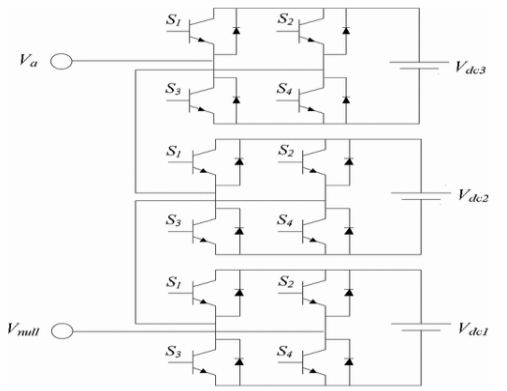

Fig 1: Topology for CHBMLI

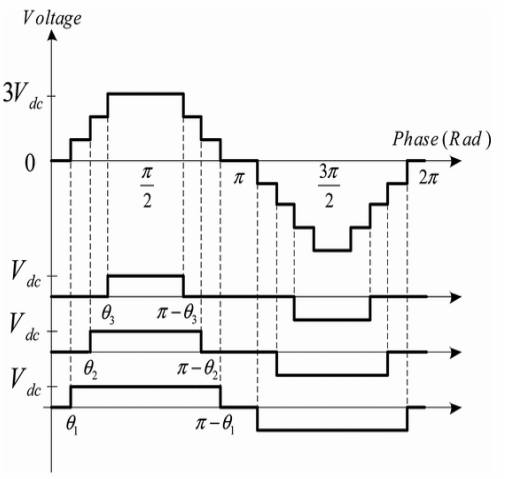

Fig 2: Typical Output Waveform for CHBMLI

3. MODULATION TECHNIQUES:

Modulation Technique is Low and High switching Frequency fort high switching frequency is considered above 1 KHz [8].

Multicarrier PWM: Multicarrier Pulse Width Modulation Technique is used in three level or more than three levels. These are classified into two types: - Level Shift, Phase Shift.

Level / Vertically Shifted PWM: Level shifted technique is the reasonable addition of sine triangle PWM for MLI, in which *n*-1 carriers are required for *n*-level inverter. They are approved in vertical shifts in constant bands defined by the levels of the inverter [8]. 3(*n*-1) carriers are requisite for 3-phases. Based on managed degrees of liberty grouping, the level shifted PWM is divided into PD, APOD and POD PWM techniques [3, 5, 6].

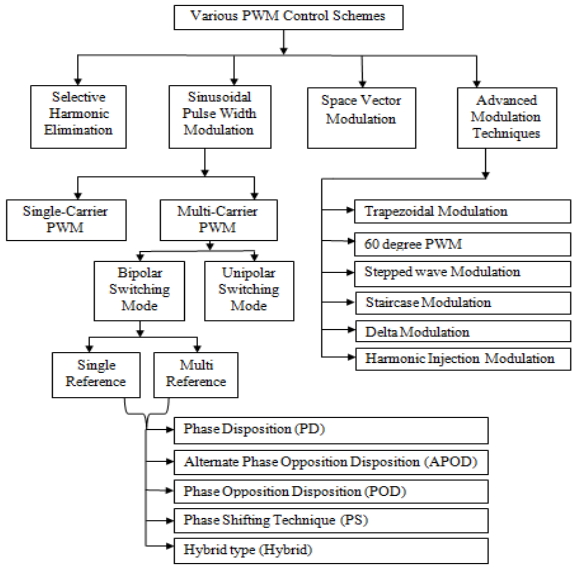

Fig 3: Types of PWM control techniques

Phase Disposition Pulse Width Modulation (PD PWM): The PDPWM with single reference is based on the evaluation of a sinusoidal reference signal with *n*-1

carriers which are vertically shifted. it can be known that the carriers that have the similar frequency f_c and amplitude A_c are in phase. The modulating signal has a frequency of f_r and an amplitude A_r.

Alternate Phase Opposition Disposition Pulse Width Modulation (APOD PWM): In APODPWM, the contiguous carriers with identical frequency and amplitude are positioned and overlapped and are phase displaced by 180° in a mode. These carriers are evaluated with single sinusoidal reference wave for the appropriate procedure of CHBMLI.

Phase Opposition Disposition Pulse Width Modulation (POD PWM): The carrier signal with similar amplitude and frequency are in phase over and under the zero reference value. However, there is 180° phase shift flanked by the ones over and under the zero reference. These carriers are overlay with single reference signal to produce the pulses for calculating the switches of MLI.

4. SIMULATION AND RESULTS:

Simulation of 9-level CHBMLI: 9-level inverter is simulated similar to that of the 7-level inverter. The difference here is the number of carrier signals. Here eight carrier signals are employed. Four of them are applied across the positive half cycle of the modulating signal [5]. Remaining four of them are applied across the negative half cycle of the modulating signal. From these signals sixteen PWM signals are generated and then given to the sixteen switches of a leg. Pulses are generated for remaining phases. Here the pulses were generated using various level shifting techniques like PDPWM, PODPWM, APODPWM.

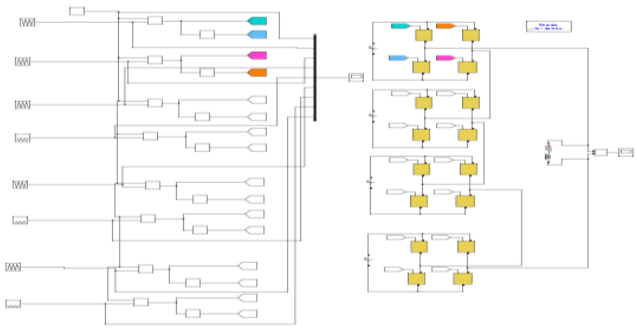

Fig. 4: Simulation for 9-level CHBMLI with PWM technique.

Table for comparisons 9-level CHBMLI on the basis of various techniques with their %THD is depicted in table 1.

Simulation Results:

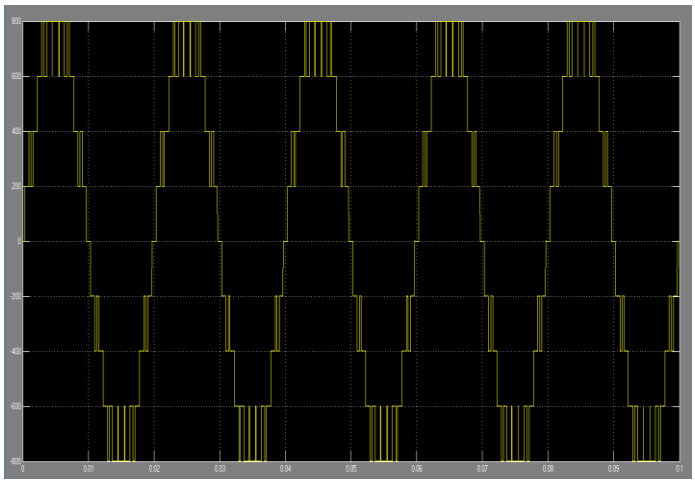

Fig. 5: Output waveform for 9-level CHBMLI.

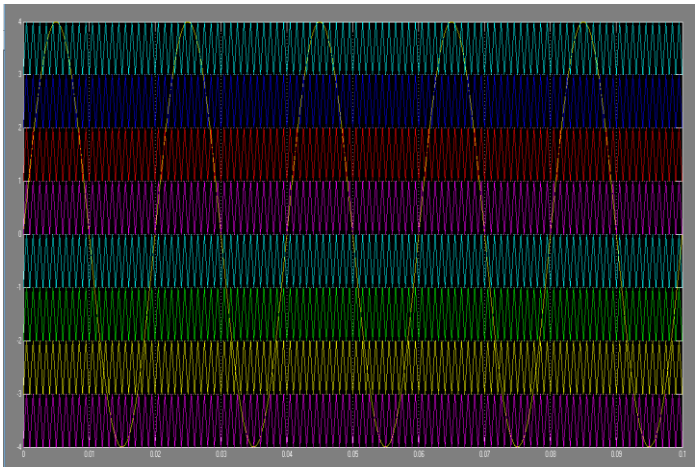

Fig. 6: Carrier arrangements for PD PWM

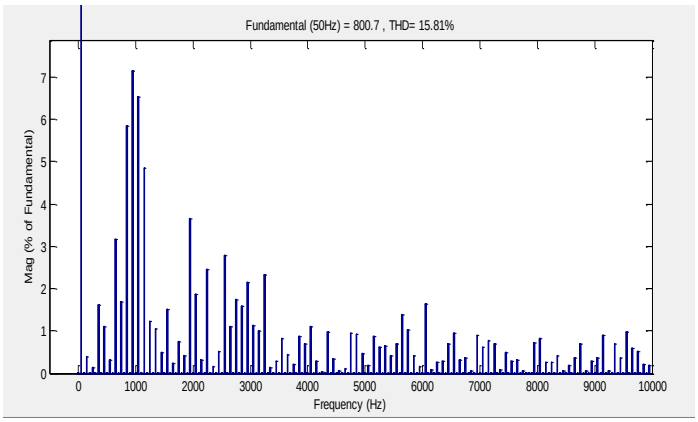

Fig.7: THD for PDPWM technique.

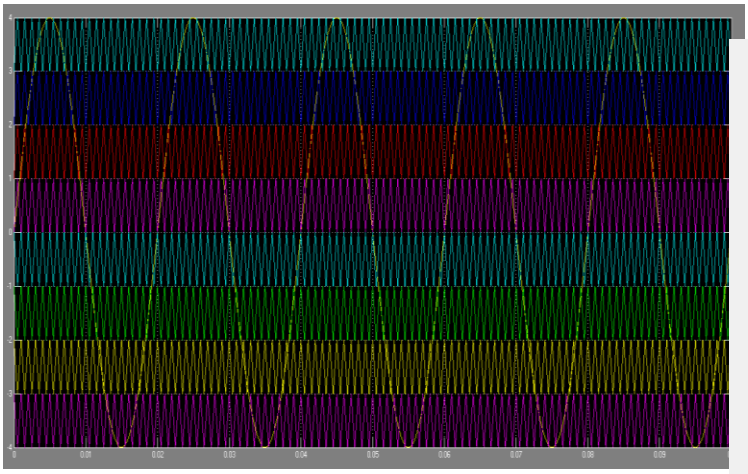

Fig. 8: Carrier arrangements for POD PWM tech.

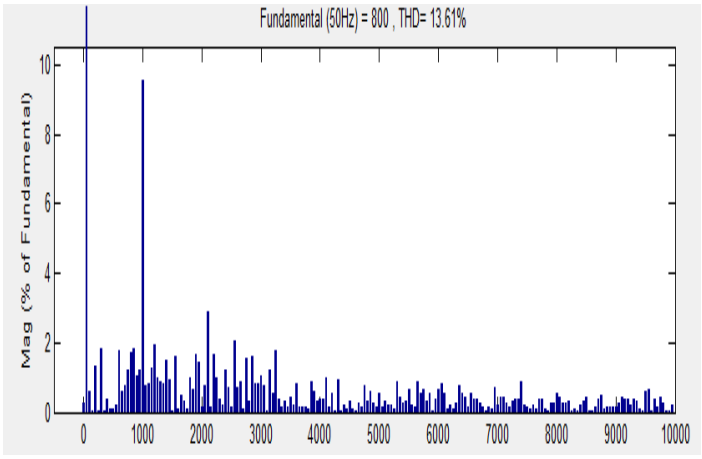

Fig. 9: THD FOR PODPWM

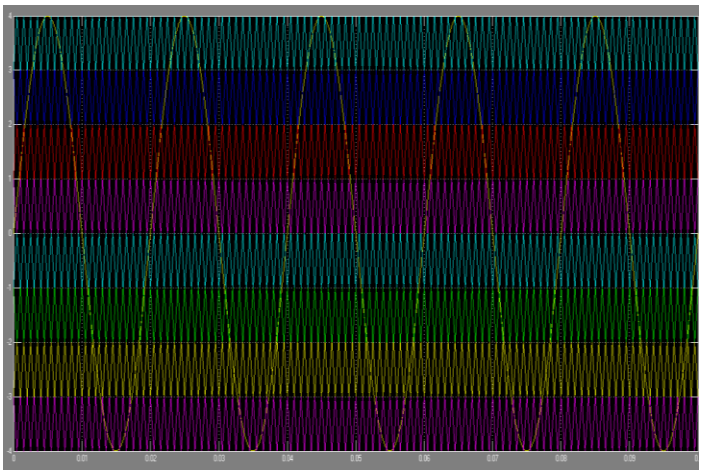

Fig. 10: Carrier arrangements for APOD PWM

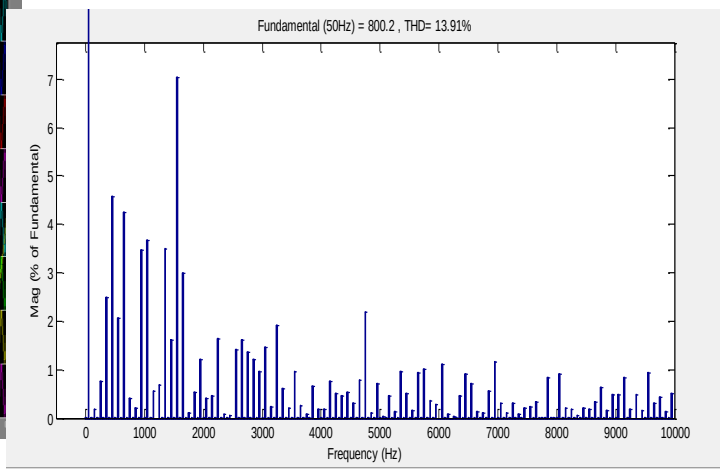

Fig. 11: THD for APODPWM tech.

Table 1 comparisons of THD of various 9-level CHBMLI on the basis of various level shifted PWM techniques.

S. No.	No. of Levels with technique	%THD
1	9-level PD PWM technique	15.81%
2	9-level POD PWM technique	13.61%
3	9-level APOD PWM technique	13.91%

5. CONCLUSION:

This paper present a single phase 9-level cascade H-Bridge multilevel inverter for DC source application. The CHB MLI copious advantages such as generation of high power, low *dv/dt* stress, minimum EMI and less THD. The projected multilevel inverter has lesser %THD without use of filter. Level shifted modulation technique is used to modulate the gate pulses of 9-level CHB-MLI and there simulation is developed in MATLAB platform. In this paper Cascade H-Bridge Topology using Phase Disposition, Phase opposition Disposition, and Alternate Phase opposition Disposition are compared. The three techniques it can conclude that the Phase opposition Disposition Topology is better among the three topologies.

6. REFERENCES

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