

# WIRELESS POWER TRANSMISSION USING NOVEL APPROACH OF ENERGY HARVESTING METHODS FOR LOW POWERED ELECTRONIC DEVICES

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**Abstract** - RF energy harvesting means to scavenge RF waves from ambient and use it to power wireless sensors and low-powered electronic devices. Renewal sources of energy like solar power can be harvested which further can be converted into a high-frequency signal by using Phase Lock Loop logic. The frequency signal is used as a source in RF energy harvesting circuit. Proposed design of energy harvesting circuit is based on cascaded Villard voltage doubler circuit. Villard circuit is a voltage multiplier which is an electrical circuit that converts AC electrical power from a lower voltage to a higher rippled D.C. voltage, typically using a network of capacitors and diodes. Proposed design consists of Schottky diodes of 2860 model and capacitors of 3.3 nF arranged in a cascaded way based on Villard voltage doubler circuit, with an RC load of resistance 100 Mega ohm and capacitance of 100  $\mu$ F output voltage is around 31.68 V at a distance of 500 M between source and receiver. source transmitting signal and receiving signal antenna are kept for 30 dB. The proposed paper presents a comparative analysis of the proposed design and other RF energy harvesting designs. In this paper, we have used MATLAB for modeling PV module for solar output. ADS (Advance Design System), 2009 version simulator is used for simulation of the proposed design and various graphs are plotted for voltage, current and power for varying distance between source and receiver and a comparative analysis is given between proposed energy harvesting circuit and previous energy harvesting circuits.

**Key words:** RF energy, voltage doubler, schottky diode, ADS, MATLAB.

## 1. INTRODUCTION

Wireless power transmission deals with transfer of electrical power from source to load without wires. From very early centuries various experiments had been carried out for showing the potential of WPT technology. First experiment regarding the wireless power transfer were carried out by NIKOLA TESLA.

Wireless power transfer technology can be categorised in two ways:

1. Near field WPT technique
2. Far field WPT technique.

### 1.1 Near field power transfer technique

Near field technique are those where coupling plays a major role in transfer of power. Coupling can be inductive between the coils or it can be capacitive between the plates which acts as electrodes. Near field technique for wireless power transfer are immensely used for charging mobile phones, electric vehicles, electric tooth brush etc.

### 1.2 Far Field Power Transfer technique

Far field technique deals with using electromagnetic radiation for wireless power transfer. power transfer can be done by using microwaves or by beaming lasers at the receiver. It can be applied for satellites which are solar powered. The above WPT technique comes under radiative methods of power transfer wirelessly.

## 2. PROPOSED METHODOLOGY

In this proposed design input is solar energy by mean of solar PV module of 83 Watt output. This power will be converted into the high-frequency mode by using PLL logic. This PLL logic actually converts solar energy signal into 2.4 GHz RF signal. In this proposed design 2.4 GHz frequency is generated but we are using a 2.4 GHz source in the simulation model which has to be simulated in the software ADS. Now from source 2.4 GHz signal is given to RF Transmitter via a wireless medium in this software we are using a line of sight antenna and the distance between transmitter and receiver is varied and output graphs are simulated for respective distances. Receiver antenna will receive transmitted RF signal and signal passes through impedance matching network. The values for lumped L & C are kept around  $1.7 \mu H$  and  $2.5 pF$  respectively. This, in turn, will maintain the same frequency on the receiver side. After that received voltage is passed from multi-stage of voltage doubler circuits which consists of frequency detector diodes. It will generate sufficient amount of voltage at the filter. The filter is a combination of RC network. Voltage regulator is used to set the voltage to the required level. After this stage, we will also involve inductive based approach which will generate required amount of power for low powered devices as shown in Fig. 4.

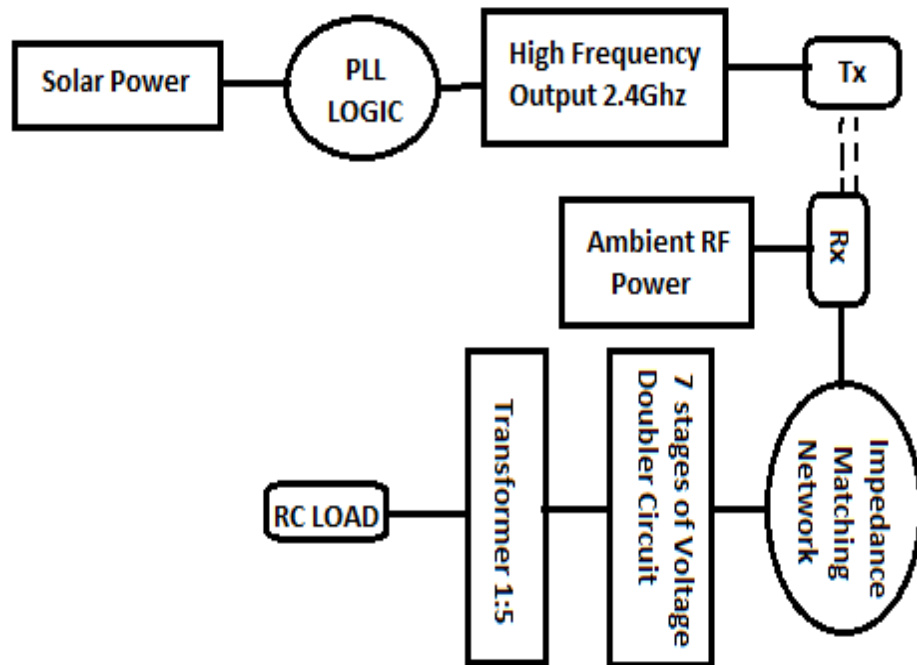


Fig -1: Proposed Wireless Power Transmission System

## 3. IMPLEMENTATION DETAILS

### 3.1 Generation of Solar Energy

To achieve 83.3 W of power with the required configuration, the single PV modules are connected. In a single module, to obtain 12 V open circuit cell voltage, 36 cells are connected in series. The analogous photovoltaic cell model can be interpreted in parallel with a diode by a current source.

### 3.2 Block Diagram

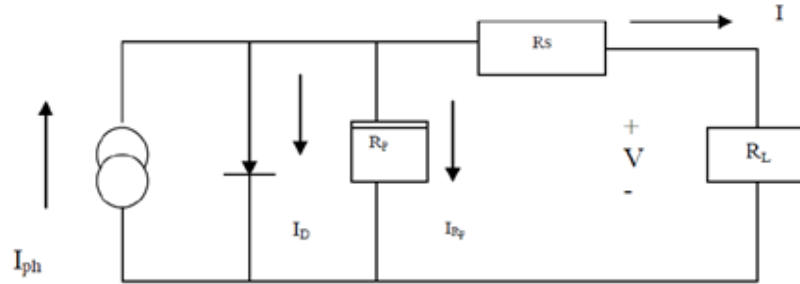


Fig -2: PV Cell model[18]

An ideal PV cell equivalent circuit can be modelled by a current source in parallel with a diode.  $R_s$  is series resistance (intrinsic) & its value is small.  $R_p$  is the equivalent shunt resistance with a very high value. Applying Kirchhoff's law to the junction where  $I_{ph}$  (current), diode, parallel resistance and series resistance are meeting, hence we get equation for the photovoltaic current  $I$ :

$$[18] \quad I = I_D - IR_p - I_{ph} \quad (1)$$

$$[18] \quad I = I_{ph} - I_0 \left[ \exp\left(\frac{V + IR_s}{V_T}\right) - 1 \right] - \left( \frac{V + IR_s}{R_p} \right) \quad (2)$$

$$I = n_{ph} I_{ph} - n_p I_{rs} \left[ \exp\left(\frac{q}{KTA} * \frac{V}{n_s}\right) - 1 \right] \quad (3)$$

$$E_G = E_G(0) - \frac{\hat{I} \pm T^2}{T + \beta} \quad (4)$$

$$I_{ph} = [I_{scr} + K_i(T - T_r)] \frac{S}{1000} \quad (5)$$

Where,  $I_{ph}$  is the current because of insolation,  $I$  is the Cell current,  $I_0$  is the Reverse saturation current,  $V$  is the Cell voltage,  $R_s$  &  $R_p$  are series & Parallel resistance respectively,  $K, T, Q$  are Boltzmann constant, temperature in Kelvin, Charge of an electron respectively. Insolation means radiation incident on the PV cells. As per simulation model in ADS software, around 83 W is generated in the enclosed MATLAB model. Two PV module is been used to generate power of 83 W.

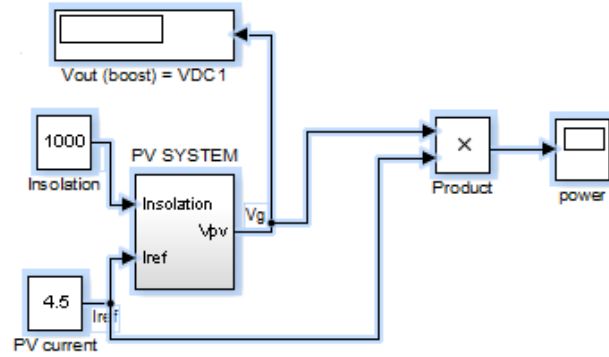


Figure-3: MATLAB Simulation Model of Solar Power Generation

### 3.3 Generation of 2400Mhz Frequency Using PLL Logic

Phase locked loop discussed below is basically a frequency synthesizer. Circuit below is an electronic and it has a VCO (voltage control oscillator), phase frequency detector. The output has phase locked in with input and it can have output which will have frequency multiple times of input frequency. Hence desired frequency can be generated.

#### 2400MHz Frequency Generation Using PLL Logic

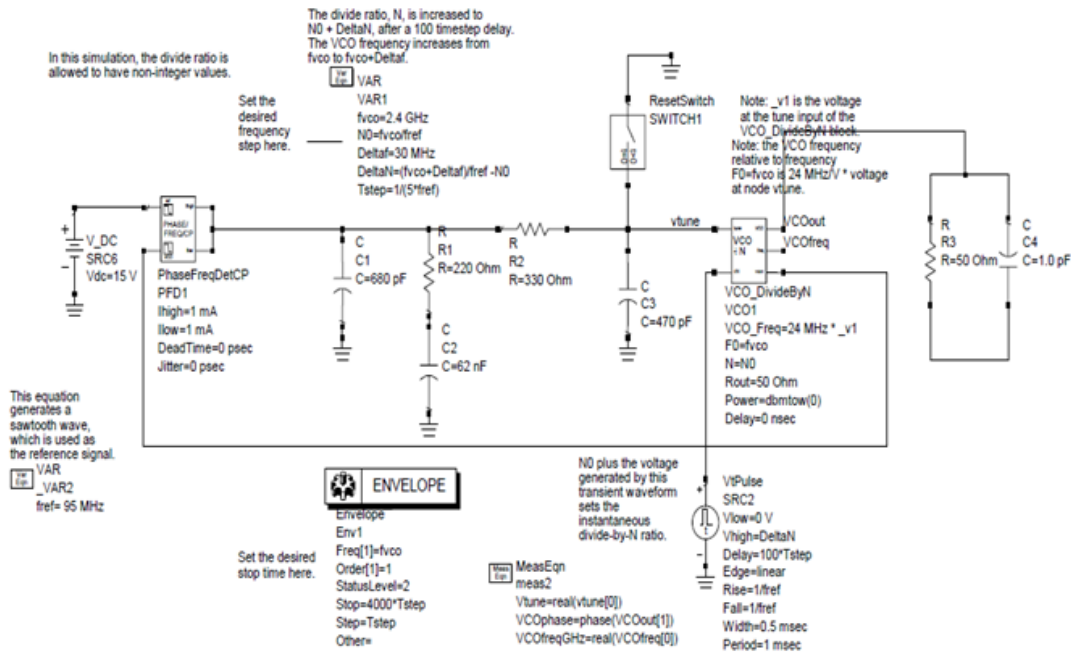


Fig -4: 2400Mhz Frequency Generation Using PLL Logic

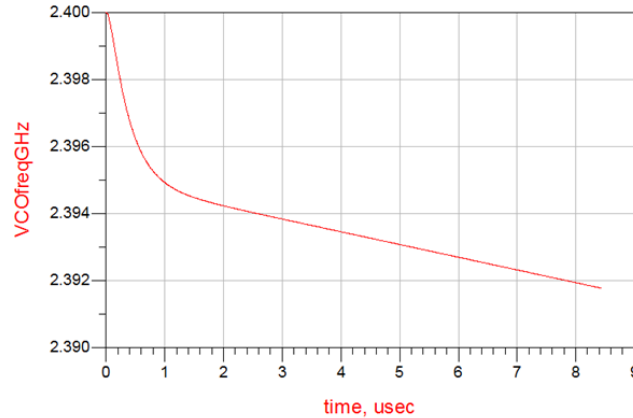


Fig -5: Output of PLL Logic

The output of PLL logic shown in Fig. 5 is a plot between output frequency and time which shows a variation in frequency. This frequency is close to around 2.4GHz which is the required transmitting frequency for the proposed design.

### 3.4 Wireless Energy Transmission using Electro-Inductive Design

According to the proposed design, the hardware system cost will be less as compared to previous existing design. In this work, the goal will be to reduce the number of voltage doublers stage & try to achieve a good distance between transmitter & receiver. Following are all simulation results which are based on Advance Design System Software. According to the proposed design, it is a combination of 6 Steps:

1. Transmission Power Section
2. Transmission & Reception Section
3. Match Network
4. Voltage Multiplier
5. Inductive Circuit
6. Load Circuit

Here for match network, we are using this particular formula:

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (7)$$

So taking the value of L=1.7nH, C=2.5pF. This is equivalent to the target frequency 2400 MHz. In this work we have also designed some previous existing approaches for comparison point of view those designs are:

1. Design and Performance Analysis of 10-Stage Voltage Doublers RF Energy Harvesting Circuit for Wireless Sensor Network [15]
2. Optimization of the Voltage Doublers Stages in an RF-DC Converter Module for Energy Harvesting [7]
3. Design Optimization and Implementation for RF Energy Harvesting Circuits [17]

#### 3.4.1 Implementation of 10-Stage Voltage Doublers RF Energy Harvesting Circuit [15]

Here according to paper [15] operating frequency is 903 MHz so value of L=10nH, C= 3.1pF. Similar in this design HSMS2852 RF Diode is used. Here total numbers of voltage multiplier stages are 10 where total 20 RF diodes are used as shown in Fig.6. Here both receiving and transmitting antenna is 30dBm.

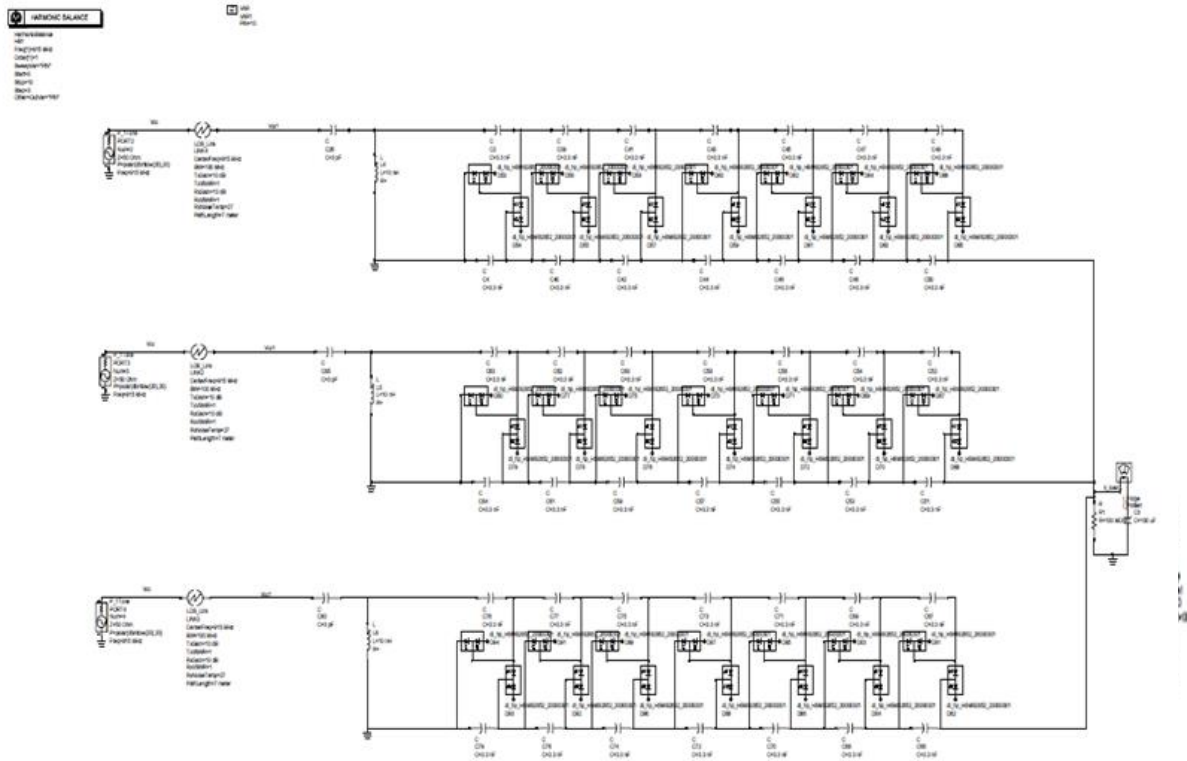


Fig -6: 10-Stage Voltage Doublers RF Energy Harvesting Circuit ref[15]

### 3.4.2 Optimization of the Voltage Doubler Stages in an RF-DC Converter Module for Energy Harvesting [7]

Here according to paper [7] operating frequency is 900 MHz so the value of  $L=1nH$ ,  $C=30pF$ . Similar in this design they are using HSMS2850 RF Diode. Here a total number of voltage multiplier stages is 7 where total 14RF diode are used as shown in Fig. 7. Here both receiving and transmitting antenna have 30dbm propagation.

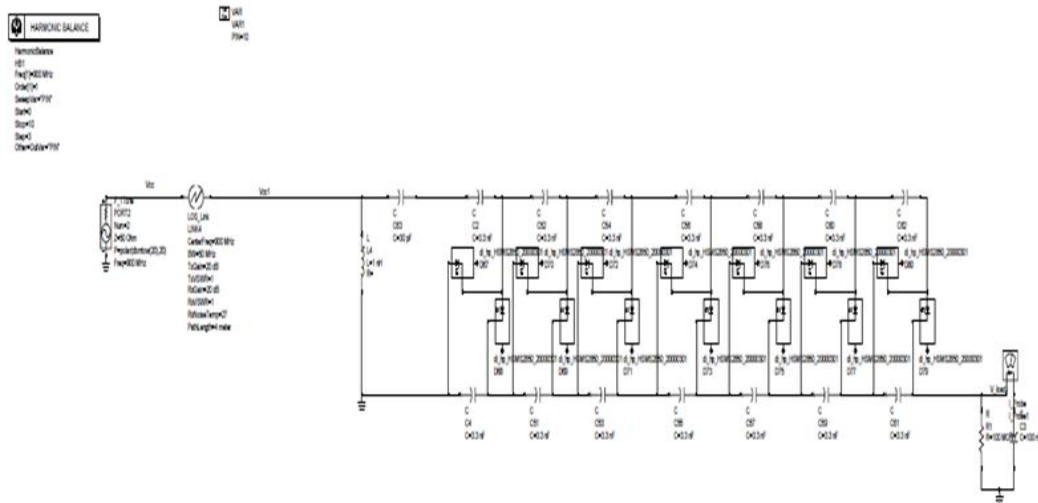


Fig-7: Optimization of the Voltage Doubler circuit 7 Stages ref [7]

### 3.4.3 Design Optimization and Implementation for RF Energy Harvesting Circuits[17]

Here according to paper [17] operating frequency is 915 MHz so the value of  $L=10\text{nH}$ ,  $C=3\text{pF}$ . Similarly, HSMS2850 RF Diode is used. Here a total number of receiver section is 3 where every section has total 7 stage voltage multiplier means total 14 RF diode are used as per Fig. 8. So total number of RF Diode are 42. Here both receiving and transmitting antenna is 30dbM.

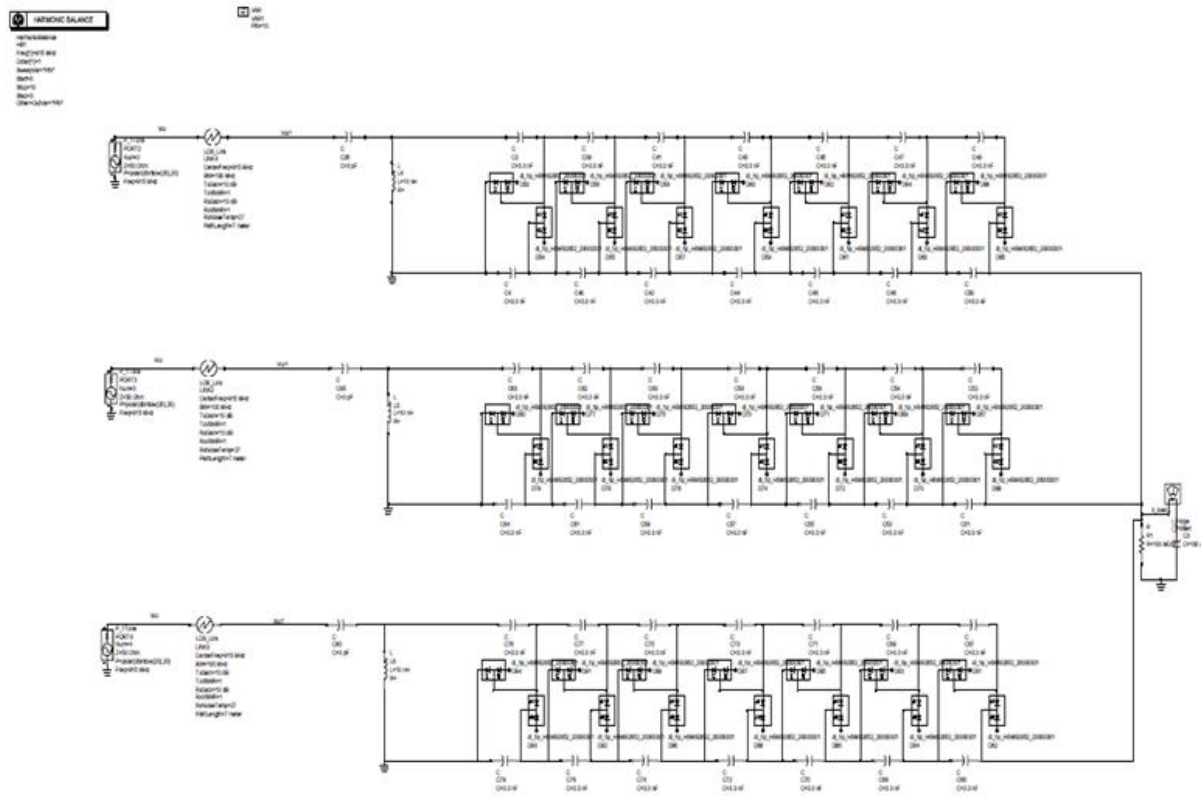


Fig - 8: Simulation Design of ref [17]

### 3.5 Proposed Design

In reference to Fig.9. Here operating frequency is 2400 MHz so the value of  $L=1.7\text{nH}$ ,  $C=2.5\text{pF}$ . Similar in this design HSMS2860 RF Diode are used. Here total numbers of voltage multiplier stages are 7 where total 14 RF diode are used. Here both receiving and transmitting antenna have 30dbM.

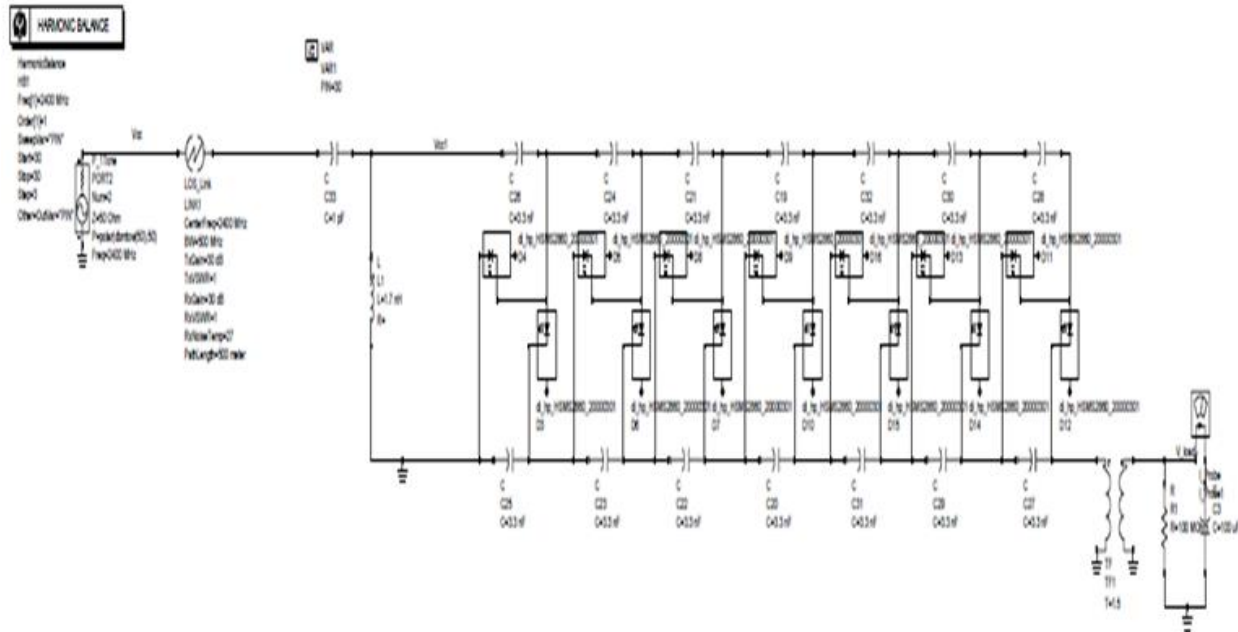


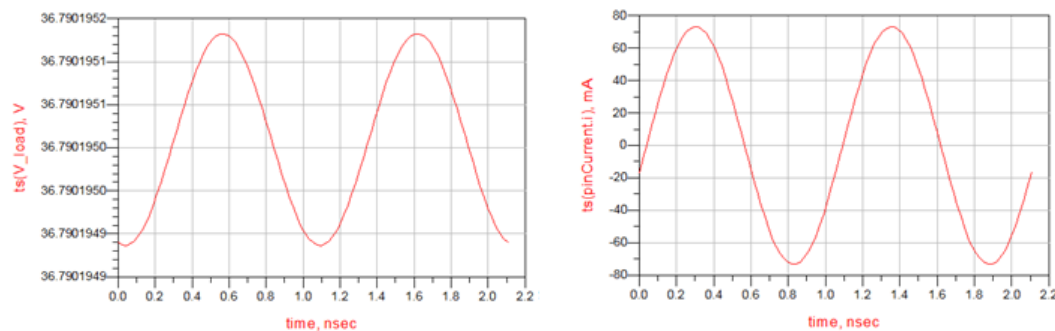
Fig -9: Proposed Simulation Design

In this **thesis** comparative analysis is presented between previous existing approaches as per reference papers [15],[7],[17] and our proposed design. A comparative study in terms of Voltage, Current, Cost,distance are also explained in detail in this chapter.

#### 4. DISTANCE BETWEEN TRANSMITTER AND RECEIVER ANTENNA IS 500 METER

##### 4.1 Output Graphs of Simulation Model for reference paper [15]

A simulation model for reference paper [15] consists of ten voltage doubler stages as shown in Fig.6. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 500 Meter. At the receiving side impedance matching is done and ten stage voltage doubler stage is made by using 20 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.9 we get output voltage across the load and current flowing through the load. The Fig. 10(a) shows Output Voltage vs Time curve having an amplitude of voltage 36.79 V and Fig.10(b) shows Output Current vs Time curve having an amplitude of current 72 mA of RC Load of ref [15] respectively.

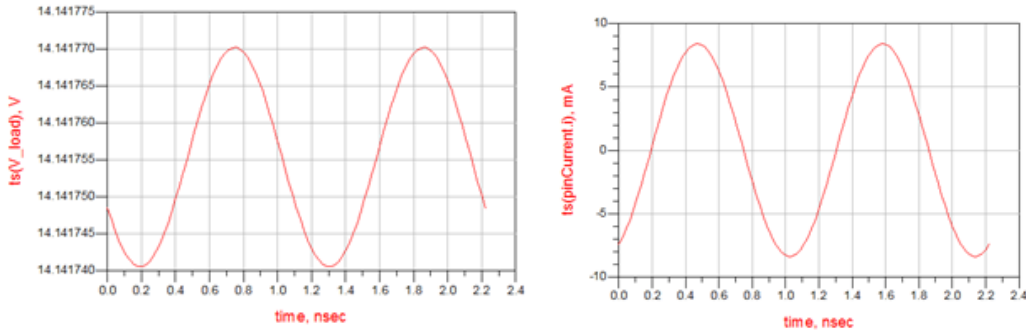


(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -10: Output Voltage vs Time curve ref [15]



### 4.2 Output Graphs of Simulation Model for reference paper [7]

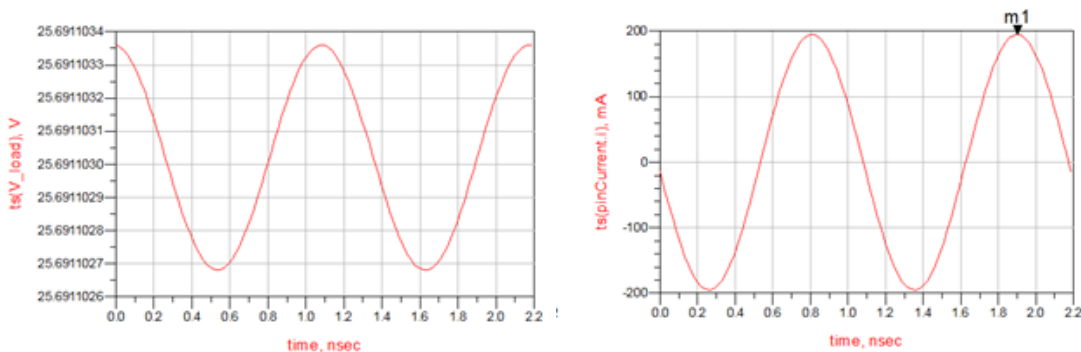
A simulation model for reference paper [7] consists of seven voltage doubler stages as shown in Fig.7. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 500 Meter. At the receiving side impedance matching is done and seven stage voltage doubler stage is made by using 14 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.7 we get output voltage across the load and current flowing through the load. The Fig. 11(a) shows Output Voltage vs Time curve having a magnitude of voltage 14.14 V and Fig.11(b) shows Output Current vs Time curve having a magnitude of current 8.1 mA of RC Load of ref [7] respectively.



(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -11: Output Voltage vs Time curve ref [7]

### 4.3 Output Graphs of Simulation Model for reference paper [17]

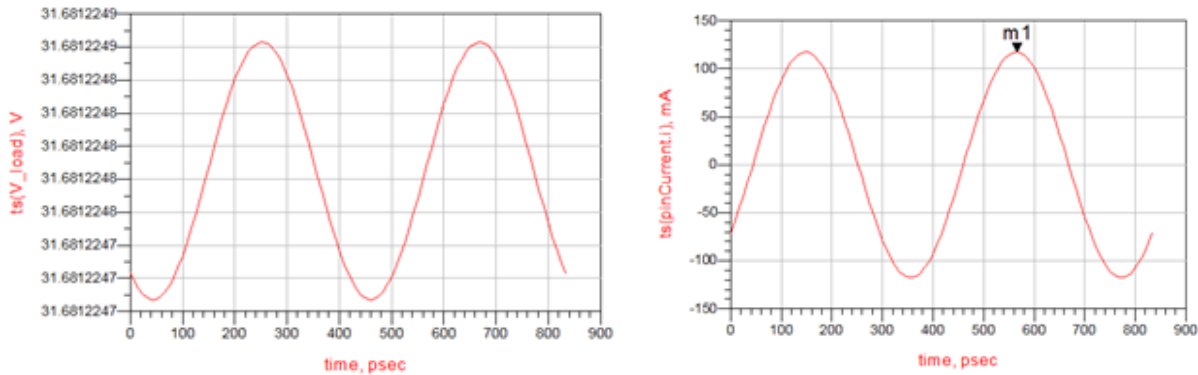
A simulation model for reference paper [17] consists of three seven voltage doubler stages as shown in Fig.8. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 500 Meter. At the receiving side impedance matching is done and three seven stage voltage doubler stage are made by using 42 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.8 we get output voltage across the load and current flowing through the load. The Fig. 12(a) shows Output Voltage vs Time curve having a magnitude of voltage 25.69 V and Fig. 25(b) shows Output Current vs Time curve having a magnitude of current 195 mA of RC Load of ref [17] respectively. The maximum current is obtained at point m1 at time=1.902 ns.



(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -12: Output Voltage vs Time curve ref [17]

#### 4.4 Output Graphs of Simulation Model of Proposed Design

The proposed simulation model with seven voltage doubler stages as shown in Fig.9. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 500 Meter. At the receiving side impedance matching is done and seven stage voltage doubler stage is made by using 14 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.9 we get output voltage across the load and current flowing through the load. The Fig. 13(a) shows Output Voltage vs Time curve having a magnitude of voltage 31.68 V and Fig. 13(b) shows Output Current vs Time curve having a magnitude of current 117 mA of RC Load of proposed model respectively. The maximum current is obtained at point m1 at time=566.7 ps.



(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -13: Output Curves of Proposed Model

#### 4.5 Comparative Voltage, Current & Power Analysis for 500m Distance

As seen from the graph of Fig. 14 there are lots of improvements in the proposed design as compared to previous existing design. According to a number of the stage, we are using only 7 stages voltage doubler circuits. In the first reference model [15] 10 stages of voltage doubler circuits are used which gives output relatively similar to that of proposed design with the only difference of 15.84% between the results. Our proposed design has less no. of frequency detector diodes which make it cost effective. In the second reference model [7] 7 stages of voltage doubler circuits are used which gives output less than 55.36% that of proposed design between the results. Our proposed design has same no. of frequency detector diodes which makes it cost effective and efficient. In the second reference model [17] 42 stages of voltage doubler circuits are used which gives output less than 18.9% that of proposed design between the results. Our proposed design has 6 times lesser no. of frequency detector diodes which makes it more cost effective and efficient. In this way, our proposed model is better than previous existing approaches.

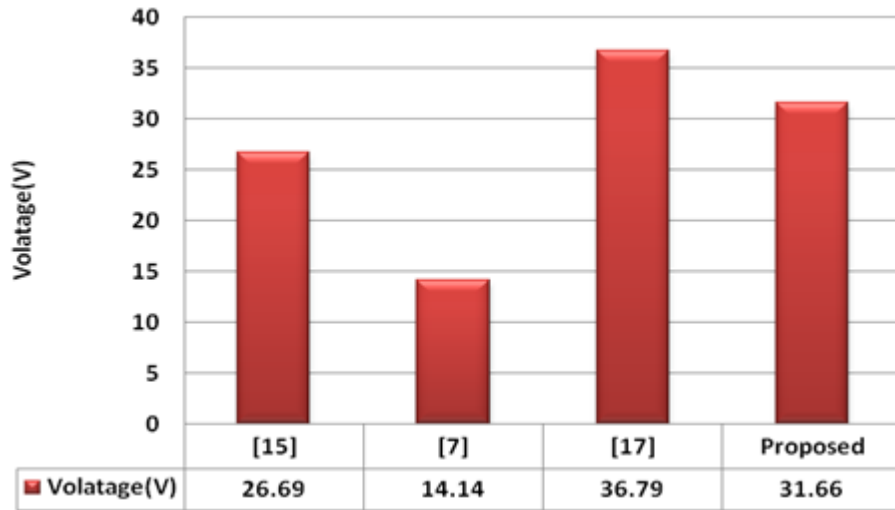


Fig -14: Comparative Voltage Analysis of all Models

As seen from the graph of Fig. 15 there are lots of improvements in the proposed design as compared to previous existing design. According to a number of the stage, we are using only 7 stages voltage doubler circuits. In the first reference model [15] 10 stages of voltage doubler circuits are used which gives output current relatively lesser to that of proposed design with the only difference of 38.46% between the results. Our proposed design has less no. of frequency detector diodes. In the second reference model [7] 7 stages of voltage doubler circuits are used which gives output less than 93% that of proposed design between the results. In the second reference model [17] 42 stages of voltage doubler circuits are used which gives output more than 66.6% that of proposed design between the results. Our proposed design has 6 times lesser no. of frequency detector diodes which makes it more cost effective and efficient. In this way, our proposed model is better than previous existing approaches.

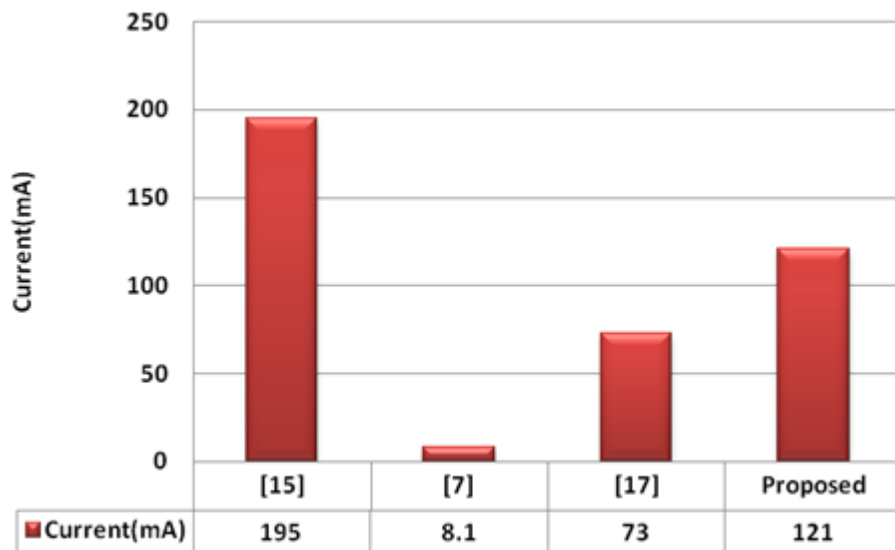


Fig -15: Comparative Current Analysis of all Models

As seen from the graph of Fig. 16 there are lots of improvements in the proposed design as compare to previous existing design. According to a number of the stage, we are using only 7 stages voltage doubler circuits. In the first reference model [15] 10 stages of voltage doubler circuits are used which gives output relatively similar to that of proposed design with the only difference of 30% between the results. Our proposed design has less no of frequency detector diodes which make it cost effective. In the second reference model [7] 7 stages of voltage doubler circuits are used which gives output less than 97% that of proposed design between the results. Our proposed design has same no of frequency detector diodes which makes it cost effective and efficient. In the second reference model [17] 42 stages of voltage doubler circuits are used which gives output more than 35% that of proposed design between the results. Our proposed design has 6 times lesser no of frequency detector diodes which makes it more cost effective and efficient. In this way, our proposed model is better than previous existing approaches.

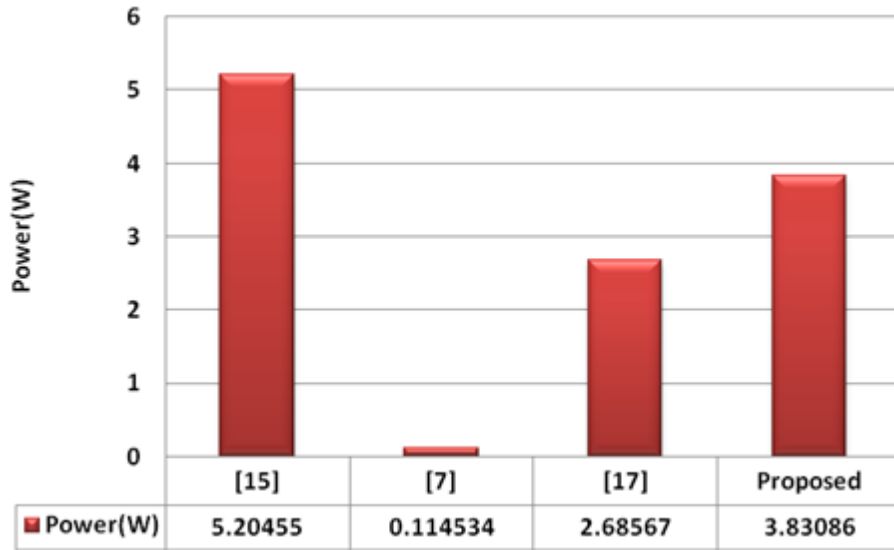
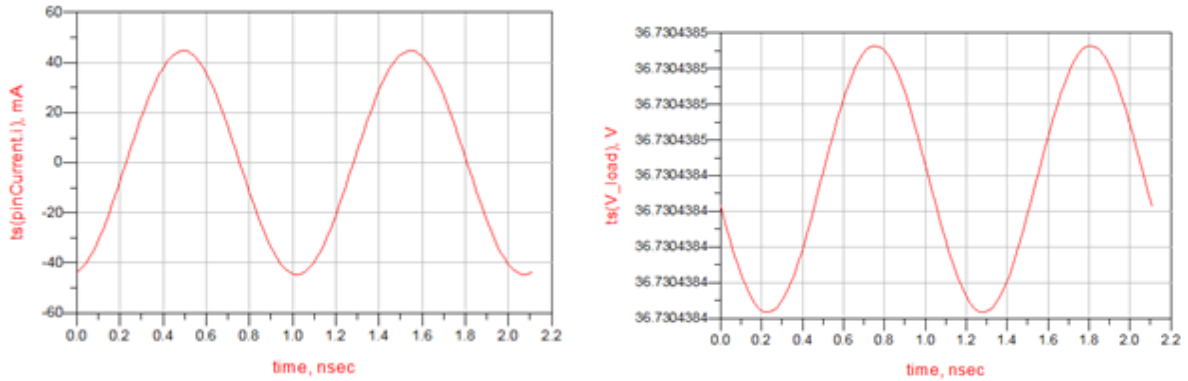


Fig -16: Comparative Power Analysis of all Models

## 5 DISTANCE BETWEEN TRANSMITTER AND RECEIVER ANTENNA IS 750 METER

### 5.1 Output Graphs of Simulation Model for reference paper [15]

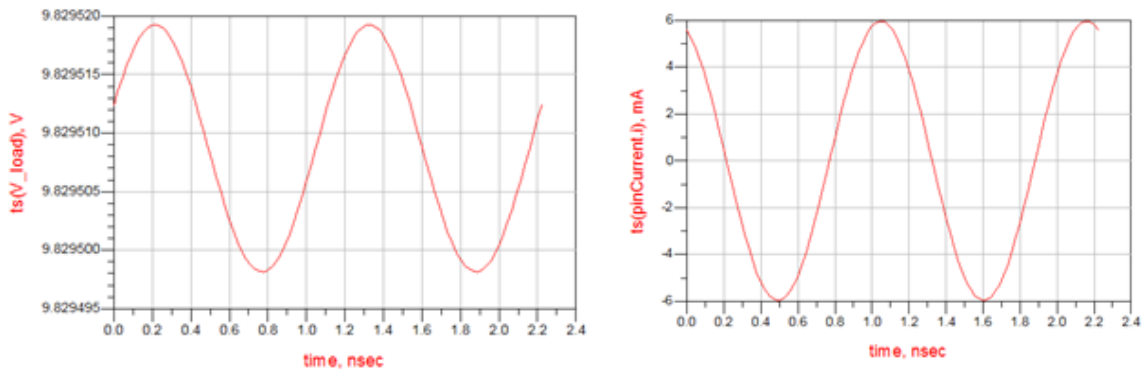
A simulation model for reference paper [15] consists of ten voltage doubler stages as shown in Fig.6. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 750 Meter. At the receiving side impedance matching is done and ten stage voltage doubler stage is made by using 20 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.6 we get output voltage across the load and current flowing through the load. The Fig. 17(a) shows Output Voltage vs Time curve having a magnitude of voltage 36.7 V and Fig. 17(b) shows Output Current vs Time curve having a magnitude of current 50 mA of RC Load of ref [15] respectively.



(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -17: Output Curves of ref [15]

### 5.2 Output Graphs of Simulation Model for reference paper [7]

A simulation model for reference paper [7] consists of seven voltage doubler stages as shown in Fig.7. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 750 Meter. At the receiving side impedance matching is done and seven stage voltage doubler stage is made by using 14 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.7 we get output voltage across the load and current flowing through the load. The Fig. 18(a) shows Output Voltage vs Time curve having an amplitude of voltage 9.82 V and Fig. 18(b) shows Output Current vs Time curve having an amplitude of current 6 mA of RC Load of ref [7] respectively.

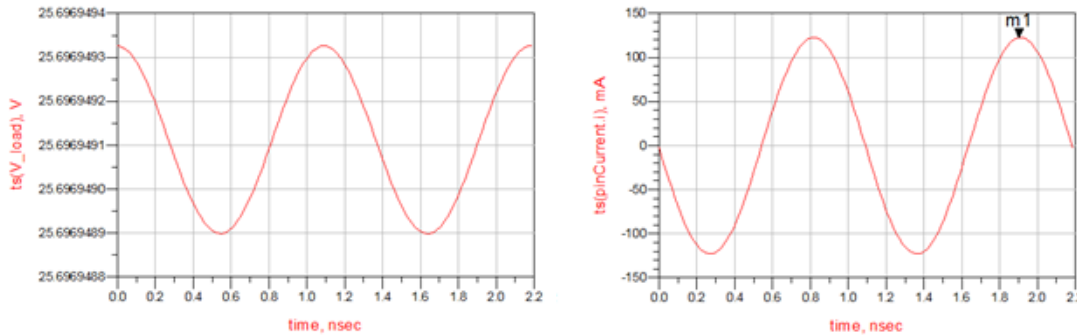


(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -18: Output Curves of ref [7]

### 5.3 Output Graphs of Simulation Model for reference paper [17]

A simulation model for reference paper [17] consists of three seven voltage doubler stages as shown in Fig.8. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 750 Meter. At the receiving side impedance matching is done and three seven stage voltage doubler stage are made by using 42 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.8 we get output voltage across the load and current flowing through the load. The Fig. 19(a) shows Output Voltage vs Time curve

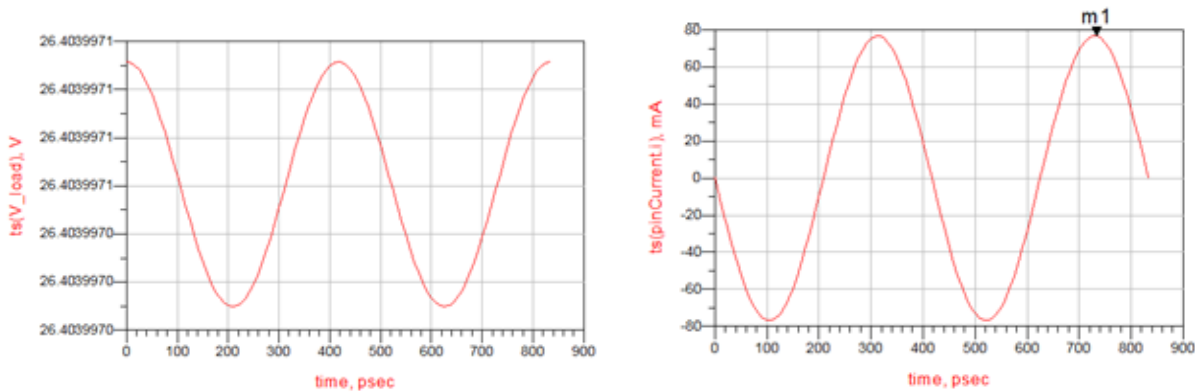
having amagnitude of voltage 25.69 V and Fig. 19(b) shows Output Current vs Time curve having amagnitude of current 123 mA of RC Load of ref [17] respectively.The maximum current is obtained at point m1 at time=1.902 ns.



(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -19: Output Curves of ref [17]

### 5.4 Output Graphs of Simulation Model of Proposed Design

The proposed simulation model with seven voltage doubler stages as shown in Fig.9. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 750 Meter. At the receiving side impedance matching is done and seven stage voltage doubler stage is made by using 14 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.9 we get output voltage across the load and current flowing through the load. The Fig. 20(a) shows Output Voltage vs Time curve having amagnitude of voltage 26.4 V and Fig. 20(b) shows Output Current vs Time curve having amagnitude of current 77 mA of RC Load of proposed model respectively. The maximum current is obtained at point m1 at time=566.7 ps.



(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -20: Output Curves of Proposed Model

### 5.5 Comparative Voltage, Current & Power Analysis for 750m Distance

As seen from the graph of Fig. 21 there are lots of improvements in the proposed design as compare to previous existing design. According to a number of the stage, we are using only 7 stages voltage doubler circuits. In the first reference model [15] 10 stages of voltage doubler circuits are used which gives output relatively similar to that of proposed design with the only difference of 39% between the results. Our proposed design has less no of frequency detector diodes which make it cost effective. In the second reference model [7] 7 stages of voltage doubler circuits are used which gives output less than 62.8% that of proposed design between the results. Our proposed design has same no of frequency detector diodes which

makes it cost effective and efficient. In the second reference model [17] 42 stages of voltage doubler circuits are used which gives output less than 2% that of proposed design between the results. Our proposed design has 6 times lesser no of frequency detector diodes which makes it more cost effective and efficient. In this way, our proposed model is better than previous existing approaches.

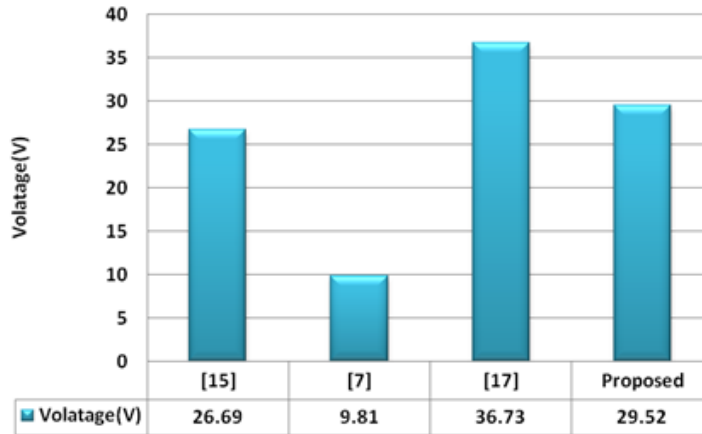


Fig -21: Comparative Voltage Analysis of all Models

As seen from the graph of Fig. 22 there are lots of improvements in the proposed design as compared to previous existing design. According to a number of stages, we are using only 7 stages voltage doubler circuits. In the first reference model [15] 10 stages of voltage doubler circuits are used which gives output current relatively lesser to that of proposed design with the only difference of 35% between the results. Our proposed design has less no of frequency detector diodes. In the second reference model [7] 7 stages of voltage doubler circuits are used which gives output less than 92.2% that of proposed design between the results. In the second reference model [17] 42 stages of voltage doubler circuits are used which gives output more than 59% that of proposed design between the results. Our proposed design has 6 times lesser no of frequency detector diodes which makes it more cost effective and efficient. In this way, our proposed model is better than previous existing approaches.

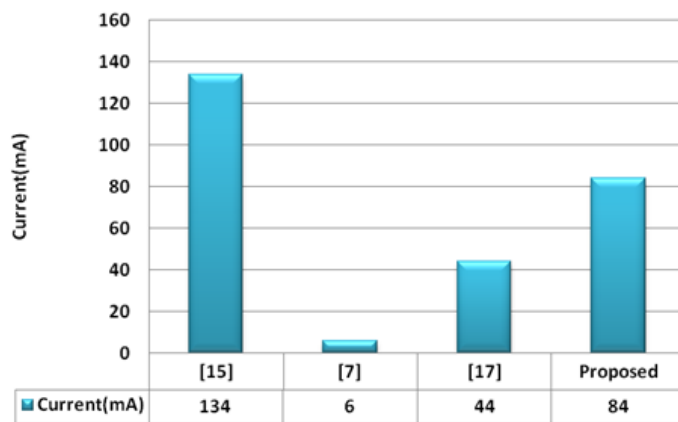


Fig -22: Comparative Current Analysis of all Models

As seen from the graph of Fig. 23 there are lots of improvements in the proposed design as compared to previous existing design. According to a number of stages, we are using only 7 stages voltage doubler circuits. In the first reference model [15] 10 stages of voltage doubler circuits are used which gives output relatively similar to that of proposed design with the only difference of 9.8% between the results. Our proposed design has less no of frequency detector diodes which make it cost effective. In the second reference model [7] 7 stages of voltage doubler circuits are used which gives output less than 96.05% that of proposed design between the results. Our proposed design has same no of frequency detector diodes which makes it cost effective and efficient. In the second reference model [17] 42 stages of voltage doubler circuits are used which gives output more than 55.17% that of proposed design between the results. Our proposed design has 6 times lesser no of frequency

detector diodes which makes it more cost effective and efficient. In this way, our proposed model is better than previous existing approaches.

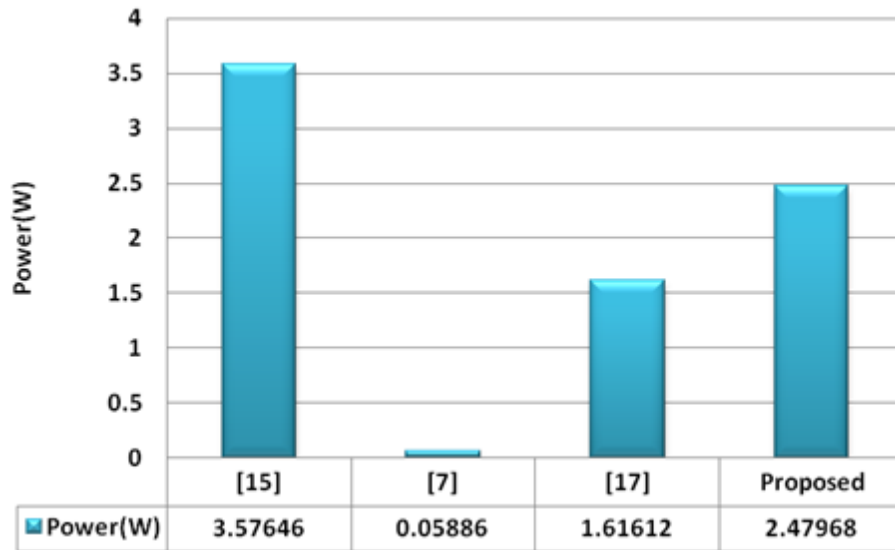


Fig -23: Comparative Power Analysis of all Models

## 6 DISTANCE BETWEEN TRANSMITTER AND RECEIVER ANTENNA IS 1000 METER

### 6.1 Output Graphs of Simulation Model for reference paper [15]

A simulation model for reference paper [15] consists of ten voltage doubler stages as shown in Fig.6. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 1000 Meter. At the receiving side impedance matching is done and ten stage voltage doubler stage is made by using 20 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.6 we get output voltage across the load and current flowing through the load. The Fig. 24(a) shows Output Voltage vs Time curve having a magnitude of voltage 36.73 V and Fig. 24(b) shows Output Current vs Time curve having a magnitude of current 36 mA of RC Load of ref [15] respectively.

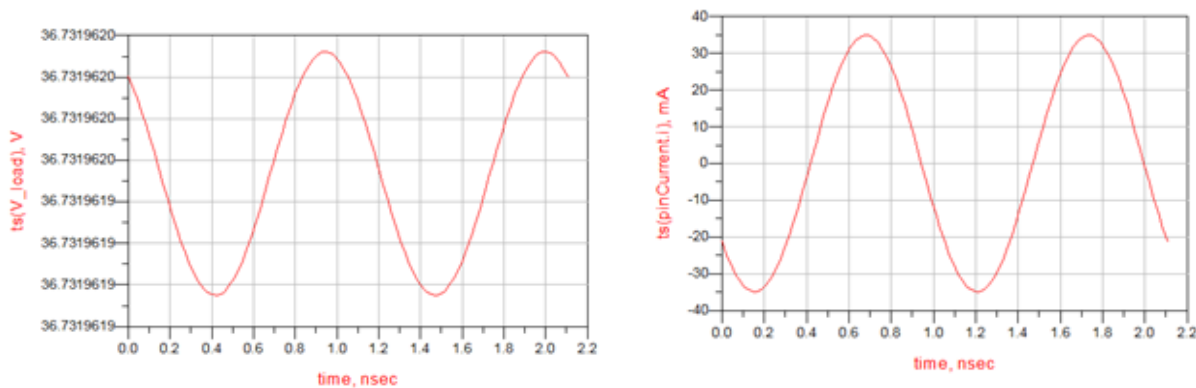
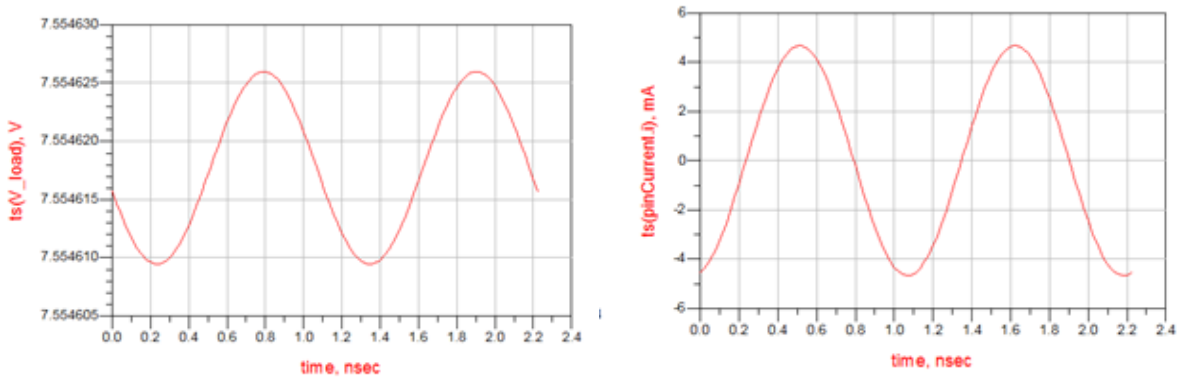


Fig -24: Output Curves of ref [15]



### 6.2 Output Graphs of Simulation Model for reference paper [7]

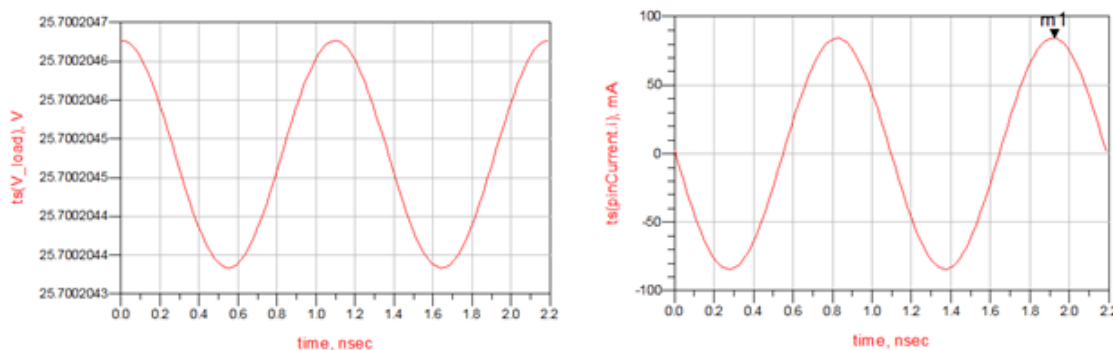
A simulation model for reference paper [7] consists of seven voltage doubler stages as shown in Fig.7. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 1000 Meter. At the receiving side impedance matching is done and seven stage voltage doubler stage is made by using 14 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.7 we get output voltage across the load and current flowing through the load. The Fig. 25(a) shows Output Voltage vs Time curve having a magnitude of voltage 7.65 V and Fig. 25(b) shows Output Current vs Time curve having a magnitude of current 4.9 mA of RC Load of ref [7] respectively.



(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -25: Output Curves of ref [7]

### 6.3 Output Graphs of Simulation Model for reference paper [17]

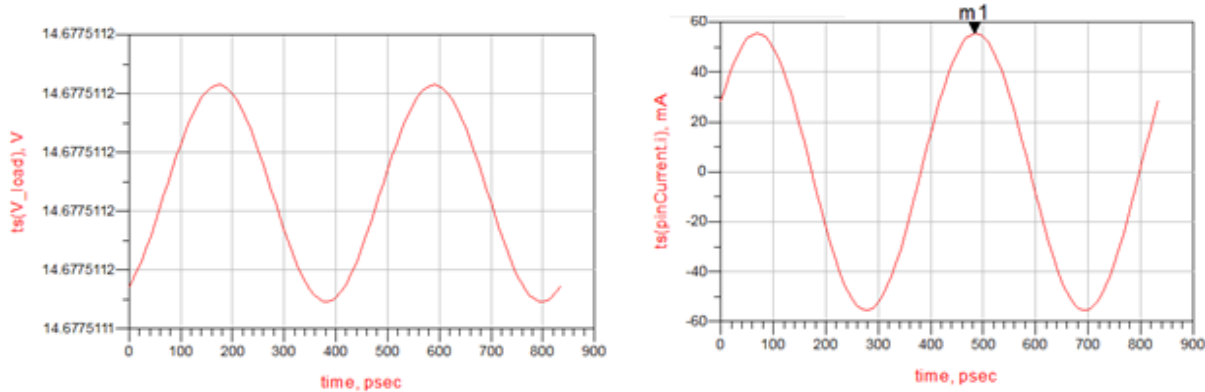
A simulation model for reference paper [17] consists of three seven voltage doubler stages as shown in Fig.8. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 1000 Meter. At the receiving side impedance matching is done and three seven stage voltage doubler stage are made by using 42 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.8 we get output voltage across the load and current flowing through the load. The Fig. 26(a) shows Output Voltage vs Time curve having a magnitude of voltage 25.7 V and Fig. 26(b) shows Output Current vs Time curve having a magnitude of current 84 mA of RC Load of ref [17] respectively. The maximum current is obtained at point m1 at time=1.923 ns.



(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -26: Output Curves of ref [17]

### 6.4 Output Graphs of Simulation Model of Proposed Design

The proposed simulation model with seven voltage doubler stages as shown in Fig.9. Advance design system is used for simulation purpose where the model is designed by using a 2.4 GHz source which is the input source available in ADS library then a line of sight antenna block with both transmitter and receiver inbuilt is connected where the length of path line is kept 1000 Meter. At the receiving side impedance matching is done and seven stage voltage doubler stage is made by using 14 HSMS 2860 frequency detector diodes. On running the simulation model of Fig.9 we get output voltage across the load and current flowing through the load. The Fig. 27(a) shows Output Voltage vs Time curve having an amplitude of voltage 14.67 V and Fig. 27(b) shows Output Current vs Time curve having an amplitude of current 56 mA of RC Load of proposed model respectively. The maximum current is obtained at point m1 at time=483.3 ps.



(a) Output Voltage vs Time curve of RC Load (b) Output Current vs Time curve of RC Load  
 Fig -27: Output Curves of Proposed Model

### 6.5 Comparative Voltage, Current & Power Analysis for 1000m Distance

As seen from the graph of Fig. 28 there are lots of improvements in the proposed design as compared to previous existing design. According to a number of stages, we are using only 7 stages voltage doubler circuits. In the first reference model [15] 10 stages of voltage doubler circuits are used which gives output relatively similar to that of proposed design with the only difference of 15% between the results. Our proposed design has less no. of frequency detector diodes which make it cost effective. In the second reference model [7] 7 stages of voltage doubler circuits are used which gives output less than 47.8% that of proposed design between the results. Our proposed design has same no. of frequency detector diodes which makes it cost effective and efficient. In the second reference model [17] 42 stages of voltage doubler circuits are used which gives output more than 75.18% that of proposed design between the results. Our proposed design has 6 times lesser no. of frequency detector diodes which makes it more cost effective and efficient. In this way, our proposed model is better than previous existing approaches.

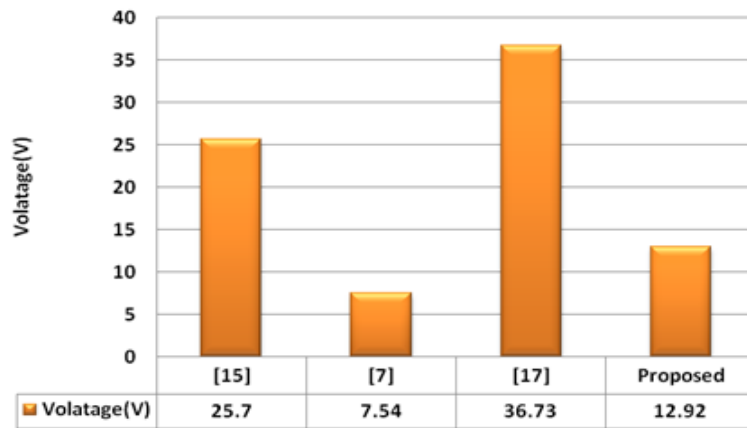


Fig -28: Comparative Voltage Analysis of all Models

As seen from the graph of Fig. 29 there are lots of improvements in the proposed design as compare to previous existing design. According to a number of thestage, we are using only 7 stages voltage doubler circuits. In the first reference model [15] 10 stages of voltage doubler circuits are used which gives output current relatively lesser to that of proposed design with theonly difference of 70% between the results. Our proposed design has less no of frequency detector diodes. In the second reference model [7] 7 stages of voltage doubler circuits are used which gives output less than 91.32% that of proposed design between the results.In the second reference model [17] 42 stages of voltage doubler circuits are used which gives output more than 28% that of proposed design between the results. Our proposed design has 6 times lesser no of frequency detector diodes which makes it more cost effective and efficient.In this way, our proposed model is better than previous existing approaches.

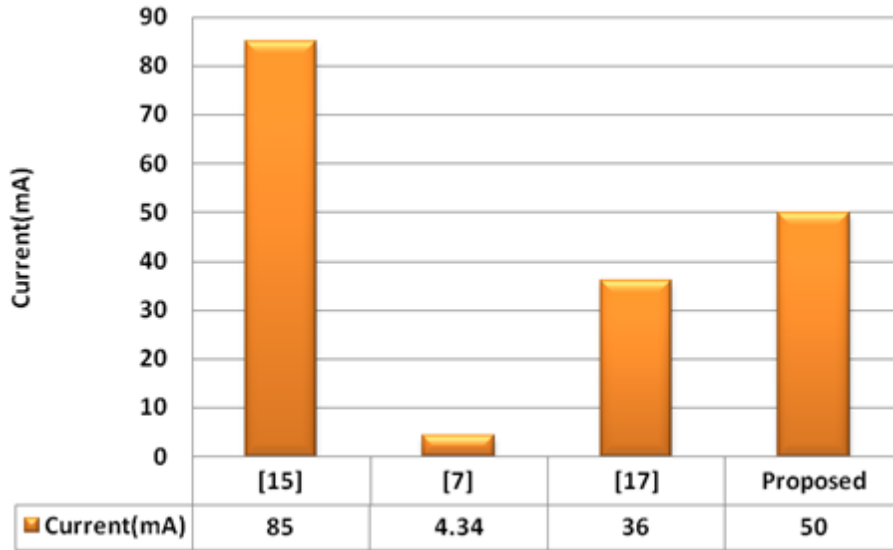


Fig -29: Comparative Current Analysis of all Models

As seen from thegraph of Fig. 30 there are lots of improvements in the proposed design as compare to previous existing design. According to a number of thestage, we are using only 7 stages voltage doubler circuits. In the first reference model [15] 10 stages of voltage doubler circuits are used which gives output relatively similar to that of proposed design with theonly difference of 62% between the results. Our proposed design has less no of frequency detector diodes which make it cost effective. In the second reference model [7] 7 stages of voltage doubler circuits are used which gives output less than 95.49% that of proposed design between the results. Our proposed design has same no of frequency detector diodes which makes it cost effective and efficient. In the second reference model [17] 42 stages of voltage doubler circuits are used which gives output more than 16.18% that of proposed design between the results. Our proposed design has 6 times lesser no of frequency detector diodes which makes it more cost effective and efficient.In this way, our proposed model is better than previous existing approaches.

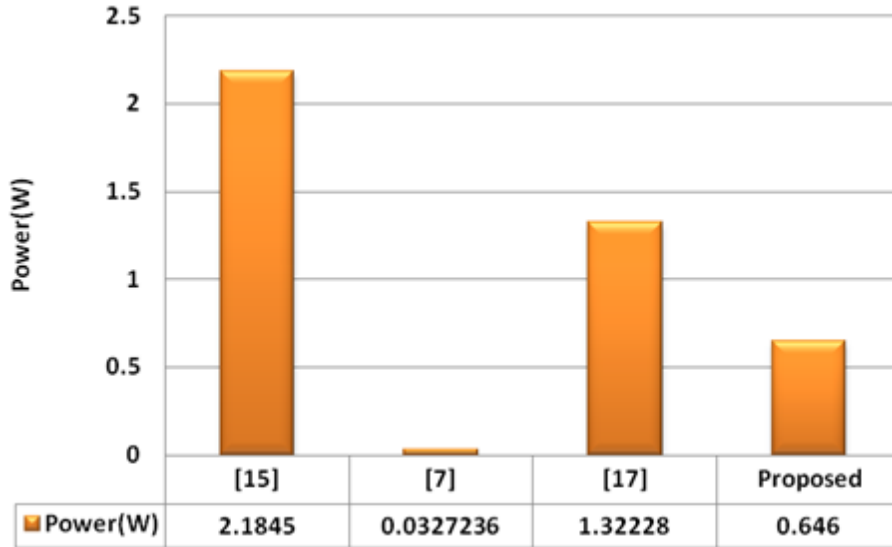


Fig -30: Comparative Power Analysis of all Models

## 7 COMPARATIVE ANALYSIS OF ALL THE APPROACHES

### 7.1 Graphical Representation of Cost Analysis

Here as seen proposed design require only 14 diode which is cost effective and its equal to [7] design but generated result is far better than [7] even generated result is very efficient as compare to previous approach design.

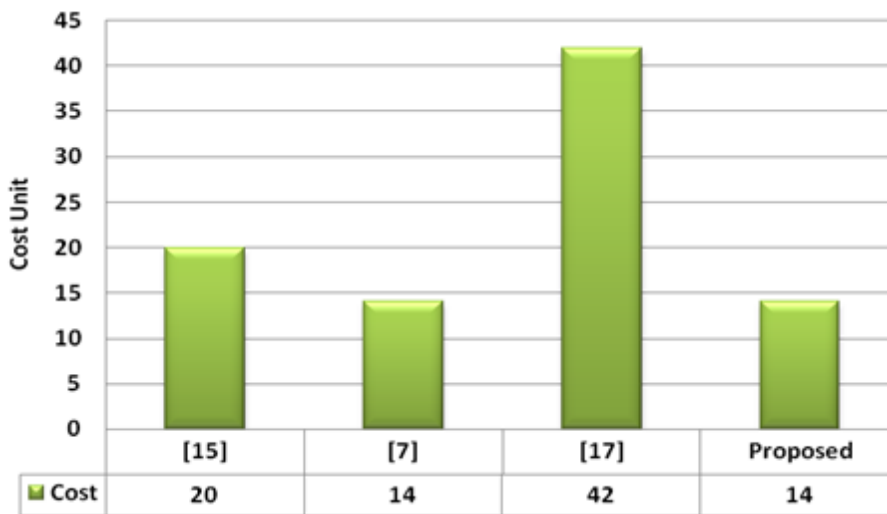


Fig -31: Graphical Representation of Cost Analysis

### 7.2 Graphical Representation of Voltage Analysis

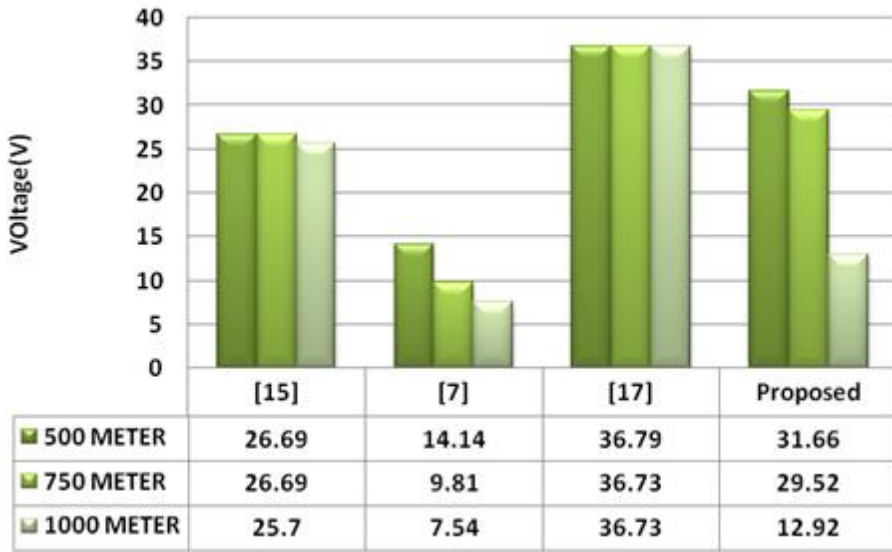


Fig -32: Graphical Representation of Voltage Analysis

### 7.3 Graphical Representation of Current Analysis

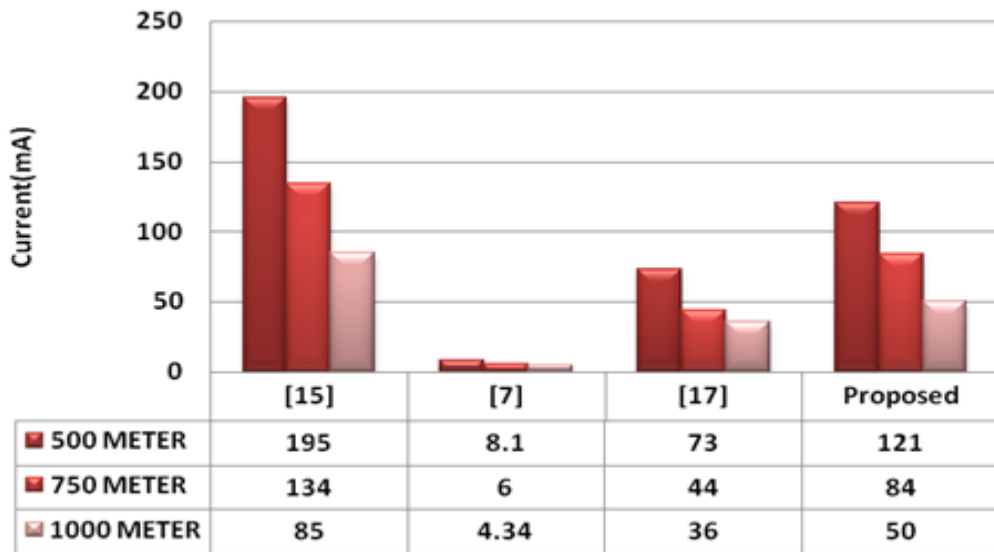


Fig -33: Graphical Representation of Current Analysis

### 7.4 Graphical Representation of Power Analysis

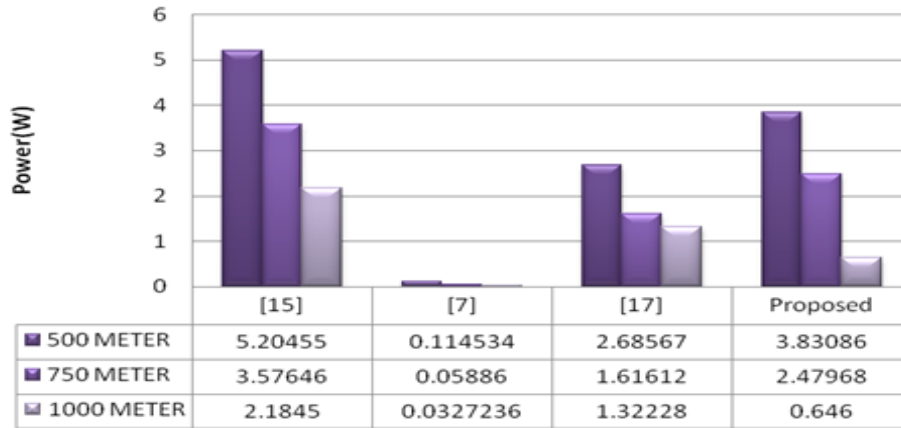


Fig -34: Graphical Representation of Power Analysis

## 8 CONCLUSION

This research is focused on a wireless solar power transmission system that uses PLL logic for high-frequency conversion and power transmission. It makes use of electro-inductive logic for its operation. The engineered device proposed is based on an electromagnetic approach with a 2.4 GHz operating frequency. The suggested design helped us solve the problems of previous established approaches such as distance, power & performance. Comparative analysis of references [15], [7] and [17] is carried out with our proposed model in this thesis. The proposed model's step-by-step comparison is carried out with references that provide better results in terms of voltage, current, power and cost. Estimated cost is quite less as compare to the previous approach of [15], [7], [17] because in our approach we are using total 14 RF diode which is lesser than previous current approach. Our system works for 30dbi here so it is simple to design transmitting and receiving ports, the radiation exposed in the atmosphere is also less. Power generated is around 83.3 W. As a result, for low-powered devices, it can be assumed that the above solution can be accurate and optimal.

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