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# A High Frequency Isolated DC-AC Converter using Dual Active Bridge with Low Decoupling Capacitance

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**Abstract:** *This system represents a dual active bridge (DAB) based high-frequency-isolated DC-AC converter suitable for photovoltaic (PV) micro-inverter application. A high frequency current injection into each of the switch nodes makes ZVS operation of the devices. The topology achieves this functionality while using the same number of devices as conventional Dual Active Bridge. Introducing a boost converter with 20 times the line frequency, thus the size of the isolation transformer is reduced. Further, control-oriented power pulsation, decoupling strategy involving dynamic variation of phase-shift, thereby resulting in reduction in decoupling capacitance requirement. Simulation studies have been verified for circuit operation and exhibit efficiency improvements compared to a similar two-stage solution.*

## I. Introduction

High-frequency ac-link-based architectures represent another category of single-stage isolated topologies and can be further classified into two types. In the first type, a high-frequency square wave or quasi-square wave generated by a primary-side inverter is appropriately modulated by a secondary-side cycloconverter with the objective of rendering a line-frequency sinusoidal profile to the current of an output inductive filter.

The major advantages of this approach are its non-reactive power processing and zero-voltage-switching (ZVS) operation of the devices. But a critical concern with this topology is the voltage spike appearing across the secondary side devices, which necessitates the use of auxiliary voltage clamping circuits.

A major shortcoming of the single-stage topologies is that there is no inherent power decoupling arrangement to account for the mismatch between the steady input dc power and the pulsating output ac power. Thus, a prohibitively high value of decoupling capacitance is necessary, entailing the use of low-lifetime electrolytic capacitors. Reduction in decoupling capacitance requirement is possible by introducing additional energy buffer circuitry, however this increases circuit complexity.

Multistage topologies perform the task of dc-ac conversion in two or more stages typically a front-end isolated dc-dc converter is responsible for voltage boosting while a cascaded inverter synthesizes the line frequency output. Depending on operation of the dc-dc stage, the inverter stage may be line frequency commutated or consist of a high-frequency pulse-width-modulated (PWM) inverter. Such topologies are easier to control and allow easy power decoupling to be affected via the high-voltage secondary-side dc bus capacitor, allowing the use of low-value, long-lifetime film capacitors. However, they suffer from high device count and low efficiency on account of the cascaded power conversion process. Moreover, for the line- frequency inverter-based solution, the dc-dc converter has to be rated for a peak power of twice the nominal power while for the PWM inverter based solution, the MOSFETS of the inverter stage do not undergo ZVS over half of the output line cycle. While classical solutions like the resonant dc link (RDCL) inverter or the auxiliary resonant commutated pole (ARCP) inverter or their modifications can be adopted to achieve ZVS operation of the PWM inverter, the auxiliary commutation circuitry used therein increases circuit complexity. Additionally, the RDCL approach increases voltage and current ratings of the main devices while the ARCP technique has its own challenges like voltage imbalance of split capacitors, difficulty in auxiliary gating control and possible overvoltage across the auxiliary devices

The key advantage of the proposed solution is its ability to realize ZVS turn-on of all switches across the ac line cycle, unlike conventional two-stage solutions, which will miss ZVS over half the ac line cycle. The topology achieves this functionality without using additional circuitry. Though the proposed circuit introduces additional conduction losses compared to two-stage topologies, ZVS operation can lead to better efficiency in cases where switching losses are significant. Further, by

employing a control strategy involving dynamic variation of phase-shift over an AC line cycle, low-frequency power decoupling can be handled by the high voltage secondary dc bus capacitor. This results in substantial reduction in decoupling capacitance requirement, allowing a film-capacitor-based implementation, which is not possible in standard single-stage topologies.

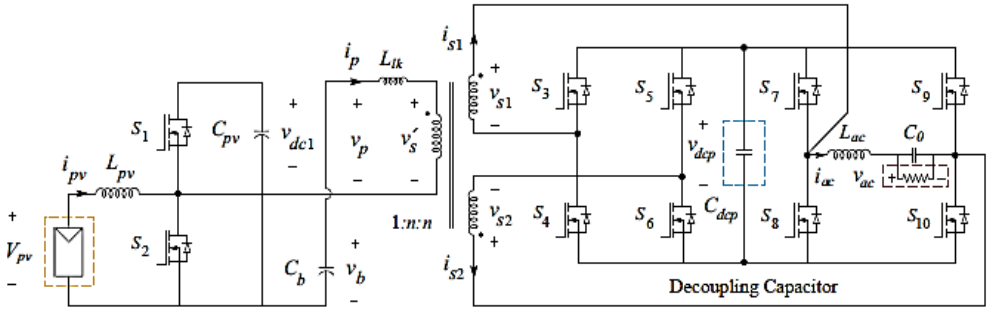


Fig. 1 Dual Active Bridge based DC-AC Converter.

This paper proposes a new high-frequency isolated PV inverter topology which combines the aforementioned ad- vantages of conventional high-frequency link and two-stage solutions. The topology, depicted in Fig. 1, works according to the DAB principle and requires the same number of devices as comparable high-frequency link and two-stage converters. The topological arrangement of the secondary-side switches ensures that each secondary-side switch node is connected to a terminal of the high frequency transformer, which helps in realizing ZVS. In the following sections, operation of the circuit is explained, followed by its steady-state analysis, a discussion on the closed-loop control scheme and detailed ZVS analysis. Finally, simulation and experimental results are presented to illustrate circuit operation and highlight the advantages of the topology.

## II. Proposed System

As shown in Fig. 1, the PV port is connected to the primary winding of a three-winding high-frequency transformer using an integrated-boost half-bridge interface and an external series inductor $L_{lk}$. This structure offers the benefits of boosting the low input voltage. The half-bridge $S_1$ –$S_2$ is operated with a fixed-duty ratio $D_1$ under steady state, the average voltage across capacitor $C_{pv}$ is obtained as

$V_{dc1} = V_{pv}/D_1$

Hence, the average output of $V_b$ under steady state is,

$V_b = V_{pv}$

On switching the half bridge S1 – S2, a zero mean rectangular voltage waveform $V_p$ with positive and negative values of $V_p$ and $-V_p(1-D_1)/(D_1)$ respectively is impressed on the primary side of the transformer.

Since the basic function of the inverter cell is to synthesize a high- frequency voltage across terminals A and B, whose switching- period average has a low-frequency sinusoidal variation, it is evident that the other switch node B cannot be connected to the remaining secondary terminal ($T_4$). Hence, in order to obtain ZVS of the second inverter leg ($S_9$ $S_{10}$), a third winding is introduced, one of whose terminals ($T_5$) is connected to switch node B. To complete the configuration, two auxiliary legs ($S_3$ - $S_4$, $S_5$ - $S_6$) are introduced in Fig. 2d, whose switch nodes are connected to the remaining transformer terminals ($T_4$, $T_6$).

## III. Steady state analysis

As explained in the previous section, a fixed duty-ratio rectangular voltage $v_p$ and a pulse-width modulated quasi-square wave voltage $V_s'$ are impressed on either side of the leakage inductor in series with the transformer's primary winding. Hence, following the DAB principle, power flow from the primary to the secondary side can be achieved by simply ensuring that $V_p$ is phase advanced with respect to $V_s'$.

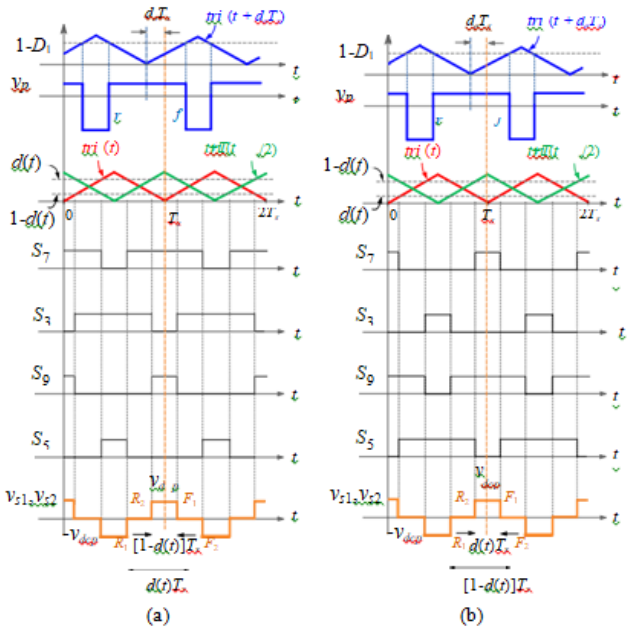

Fig. 2. (a) Positive AC line cycle, $d(t) > 0.5$. (b) Negative AC line cycle, $d(t) < 0.5$.

Depending on the relative values of the phase-shift duty ratio $d_\varphi$ (defined as the angle between the fundamental of $V_p$ and fundamental of $V_s'$ normalized to $2\pi$ radians), the duty-ratio $D_1$ of the dc side half-bridge and the instantaneous for $D_1 < 0.5$. Conditions for operation in each mode are pulse-width $\alpha T_s$ of $v_S'$, six operating modes are possible for $D_1 > 0.5$. Similar modes can be defined transformer current and also loss of ZVS of the primary-side devices and hence ignored. Similarly, it may be noted that the modes are defined such that the maximum value of phase- shift $D_\varphi$ is 0.25. This is because $D_\varphi$ is always limited to be below 0.25, since operation beyond 0.25 results in higher rms currents.

## IV. Simulation Results

A simulation model of the proposed topology, with specifications listed in Table I, has been developed in MATLAB. Components $L_{in}$, $C_{in}$ noted in the table refer to a high- frequency filter added at the input port to attenuate switching ripple in the input current. The results shown correspond to the nominal operating condition of $V_{pv}$ = 24 V, $D_1$ = 0.5 and $V_{dcp}$ = 300 V and for operation with a resistive load, unless otherwise mentioned.

TABLE I

PARAMETER VALUES FOR THE SIMULATION MODEL

| $V_{ac(rms)}$ | $V_{pv}$ | $L_{pv}$ | $L_{in}$ | $C_{in}$ | $L_{pv}$ |
|---|---|---|---|---|---|
| 230 V | 24 V | 140$\mu$H | 545 $\mu$H | 20 $\mu$F | 140 $\mu$H |

| $C_b$ | Turns ratio | $f_s$ | $L_f$ | $C_f$ | $C_{pv}$ |
|---|---|---|---|---|---|
| 40$m$F | 1:64:64 | 1KHz | 3$m$H | 75 $\mu$F | 20 $\mu$F |

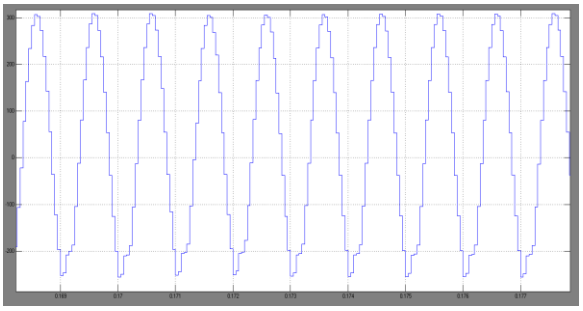

Fig 3. Boost Half bridge output simulation

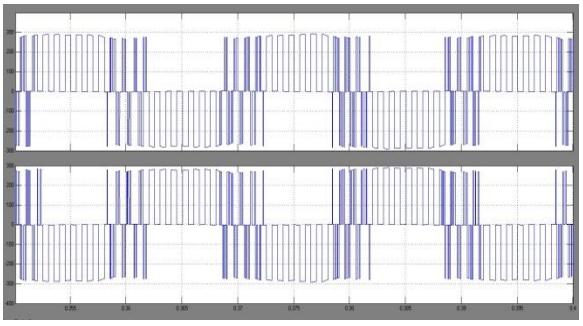

Fig 4. High Frequency Transformer output

The transformer turns-ratio of 2.13 is chosen so as to satisfy the ZVS constraints under this operating condition. The value of 40 $\mu$F for the decoupling capacitor $C_{dcp}$ is based on a design choice of having a peak-peak voltage ripple ($v_{dcp}$) of 50 V about the average value of 300 VAs regards to comparison with the two-stage topology, it is observed that apart from $S_1$, the rms current ratings in the proposed topology is slightly higher, which can be attributed to the additional high- frequency current necessary to achieve ZVS of the secondary switches across the ac line cycle. While this imposes some conduction loss

penalty, the benefit of achieving ZVS for all secondary switches in the proposed topology as opposed to partial ZVS of the inverter-stage MOSFETS ($S_7$-$S_{10}$) in the two-stage solution, could be a greater advantage in high voltage, high switching-frequency applications.

## V. Experimental Result

A 24 V input, 230 V, 50 Hz ac output laboratory prototype of the converter has been built and tested. Details of the components used in the hardware are presented in Table II. Since the objective of the work was to demonstrate the ad- vantages of the proposed solution, the focus was on converter design and operation. Hence, a real PV module or solar array PV source was not employed.

TABLE II

DETAILS OF COMPONENTS USED IN HARDWARE PROTOTYPE

| Component | Description |
|---|---|
| Primary switches | IXTP10P50P (500V, 10A) |
| Secondary Switches | IXTH20P50P (500V, 20A) |
| DC inductor | 140 $\mu$H, 19T/12 wire gauge |
| Primary Capacitor | 20 $\mu$F, 500V, Film |
| Secondary Capacitor | *40*$\mu$F, 500V, Film |
| AC inductor | 3*mH,* 3A, 140T/18 wire gauge |

## VI. Conclusion

A High Frequency isolated DC-AC Converter using Dual Active Bridge with Low Decoupling Capacitance for PV port is proposed. The key advantage of the proposed solution is its ability to realize ZVS turn-on of all switches across the ac line cycle, unlike conventional two-stage solutions, which miss ZVS over half the ac line cycle. ZVS operation can lead to better efficiency in cases where switching losses are significant. Low-frequency power decoupling can be handled by the high voltage secondary dc bus capacitor. This results in substantial reduction in decoupling capacitance requirement. This results in substantial reduction in decoupling capacitance requirement, which is not possible in standard single-stage topologies.

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