HIGH-SPEED LOW-POWER WIRELESS FREQUENCY TO VOLTAGE CONVERTER USING CMOS CONVERTER

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Abstract - *For this work, a high-speed low-power (LHF) wireless converter (FVC) based on two models was developed and implemented. The Multisim program is used to construct the first version. This consists of two RMS-DC converters, a differentiator and a splitter. The proposed converter includes a specific output and a linear transition function without ripples. The second version is designed with the help of the Tanner EDA system. The differentiator consists of two voltages for the new transformer, two RMS-DC converters and a separator. The proposed converter provides a stable output and linear propagation mechanism without ripples and is suitable for high-frequency applications. The downside of the second edition of the first edition is that it can be extended to the GHz frequency range as it is optimized with existing CMOS circuits..*

Key words: - *Frequency to Voltage Converter (FVC), CMOS, RMS-DC, MOSFET, analogue to digital converters (ADCs), digital to analogue converters (DACs), variable gain amplifiers (VGAs).*

1.1 Introduction

In this segment, we have introduced and implemented Frequency to Voltage Converter (FVC) using current CMOS circuits. The simulation of the planned circuit was conducted using the Tanner EDA 180 nm technology with a different supply voltage. Both circuits were tested with the same input condition for a good synthesis of comparative analysis. Within this portion, we have also measured the power consumption of all circuits at various power supply voltages [3, 5].

1.2 Basic principle of proposed FVC using CMOS circuit

We consider that a sinusoidal signal with amplitude A and frequency ω_{in} is applied as input in the FVC circuit.

Assuming that the input signal is a pure sinusoidal signal with a peak amplitude of A and input frequency of ω_{in}

$$V_{in}(t) = A \sin(\omega_{in} t) \quad (1)$$

Then, the derivative of this signal at the output of differentiator can be written as

$$V_d(t) = \frac{dV_{in}(t)}{dt} = A\tau_d \cos(\omega_{in} t) \quad (2)$$

Where τ_d is the time constant of the differentiator.

After applying $V_{in}(t)$ and $V_d(t)$ into the RMS-DC converters, we get

$$I_{RMS1} = \frac{A}{\sqrt{2}} \quad (3)$$

$$I_{RMS2} = \frac{A\tau_d \omega_{in}}{\sqrt{2}} \quad (4)$$

Thus dividing I_{RMS2} in (4) by I_{RMS1} in (3), we get

$$V_{out} = K\omega_{in} \quad (5)$$

Where, $K = K_{div}\tau_d$ is the sensitivity of the converter

And, K_{div} is the scaling factor (gain) of the divider

It is clearly seen from equation (5) that the output signal is linearly proportional to the input frequency, ω_{in}, and insensitive to the input signal amplitude, A.

1.3 Block diagram of proposed system (Model-II)

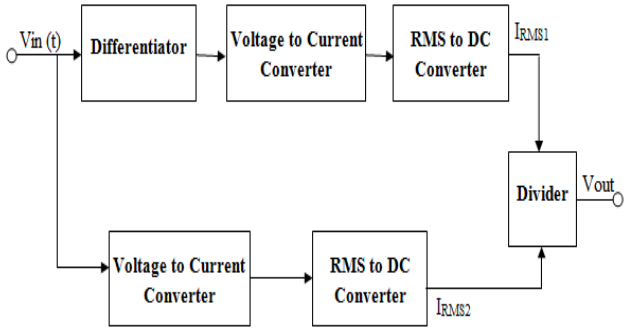

Fig.1.1: Block diagram of proposed frequency to voltage converter

The figure shown above is a basic block diagram of the proposed circuit. This is a clear example of how we have applied our circuit and the different parts of it. This

configuration consists of a differentiator, two voltages to a current converter, two RMS-DC converters, and a divider as seen in the diagram above.

The feedback signal V in(t) is sent to two directions from the above representation. One is fed to the differentiator and then sent to the voltage to the current converter and then to the RMS-DC converter I and the other to the voltage to the current converter and then to the RMS-DC converter II to the output signal. First, these outputs are sent to the divider to control the DC voltage, which reflects the sinusoidal input signal frequency as the FVC output.

1.4 Mathematical analysis of the proposed system

In the mathematical analysis, we performed a small signal model analysis of the two-stage CMOS op-amp circuit [10, 11]. After analyzing this circuit, we designed the differentiator circuit and the voltage for the current converter circuit.

Two-stage CMOS op-amp

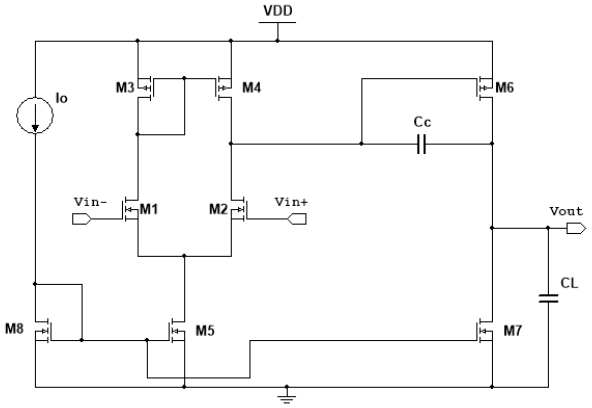

Fig.1.2: Circuit diagram of two stage op-amp

The small signal model for above circuit is given as;

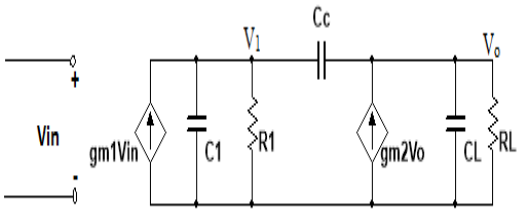

Fig.1.3: Small signal model of two stage op-amp

1.5 Schematic diagram & simulation result of proposed system

The block diagram shown in Fig.1.1 has been implemented here. Here we have built each block that is shown in Fig.1.1 using CMOS current mode circuits. The schematic configuration and simulation is done on the Tanner EDA device in the 180 nm library format.

1.6 Differentiator

The differentiator is often referred to as the circuit shift rate. Within the differentiator, the capacitor is in series with the signal line while the resistor is parallel to the side. In this case, the RC time constant is short compared to the signal period. The working amplifier makes it fairly easy to create high-quality active differentiator circuits[12]. By applying electrical reactions to the feedback loops of the op-amp circuits, we will allow the output to respond to changes in the input voltage over time. Differentiator produces a voltage output equal to the rate of shift of the input voltage. Capacity can be defined as a measure of the resistance of the capacitor to voltage changes. The greater the power, the greater the opposition [6].

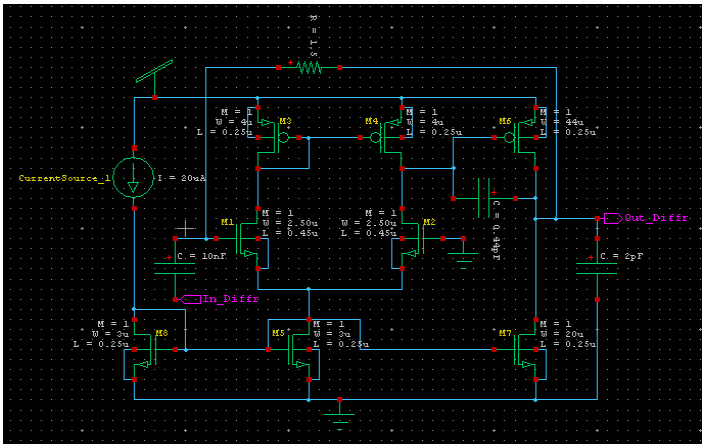

Fig.1.4. Schematic diagram of proposed differentiator circuit

The figure above shows a two-stage, op-amp-based differentiator that detects voltage shift by measuring current through a capacitor and outputs a voltage proportional to that current. The first stage is the differential amplifier stage formed by MOSFET M1 to M5 and the second stage is the common source amplifier stage formed by MOSFET M6 to M7. The simulation of this method is seen in the following section.

1.7 Design simulation

If the sine wave is added to the differentiator origin, the effect is the sine wave output that is transferred to – phase 90 °. The circuit was tested using T-Spice with 180 nm TSMC CMOS device parameters. Vdd=1.6 V, C1=10nF and R1=1.5 ohm is used. Chart. Chart. 4.5 (a) indicates the time response of the differentiator with a sinusoidal input voltage with a peak amplitude of 2V and a frequency of 5

MHz. Production of the differentiator is the cosine wave with a peak amplitude of 800 mV as seen in Fig.4.5 (b).

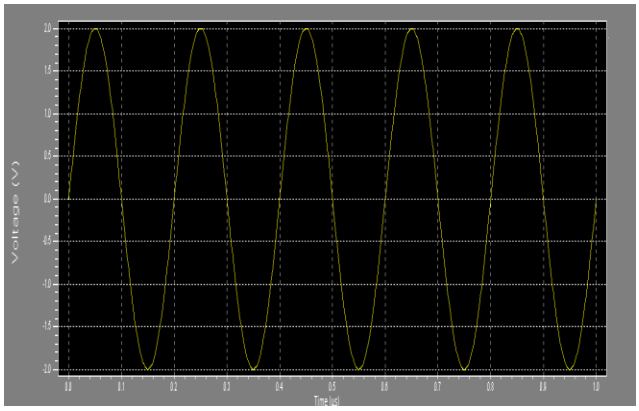

Fig.1.5 (a) Input voltage

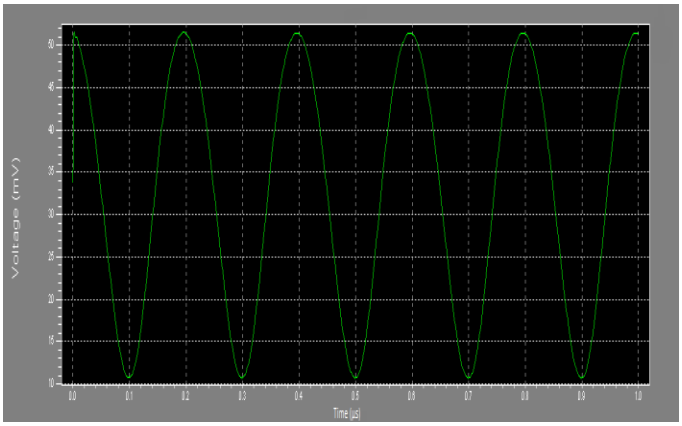

Fig.1.5 (b) Output voltage

1.8 Power consumption

The input voltage ranges from 1.2 to 3.3V and it is possible to receive the electricity used at various supply voltage levels. Table 1 displays the values of the electricity used with the various values of the supply voltage.

1.9 Voltage to current converter- Voltage to current converters were used to connect between voltage mode and current mode circuit[8]. The conversion of the V-I is generally required to be linear. With adequate linearity and precision, V-I converters can be used in analog to digital converters (ADCs), digital to analog converters (DACs), variable gain amplifiers (VGAs), multipliers, filters, modulators, mixers, and many other circuits needing high operating speeds.

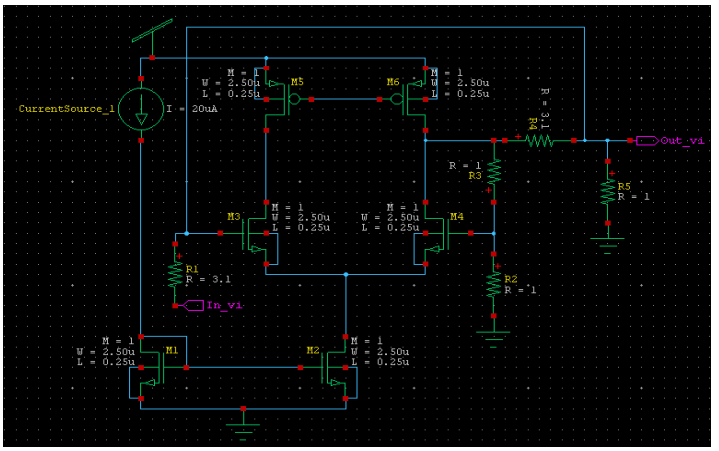

Fig.1.6. Schematic diagram of proposed voltage to current converter circuit

1.10 Simulation of design-The circuit was simulated using T-Spice with 180 nm TSMC CMOS process parameters.

Vdd=1.6V, R1 = R2 = R3 = R4=10 ohms is used. Fig.1.7(a) indicates the time response of the voltage to the current converter for a sinusoidal input voltage of 2V peak amplitude and 5 MHz frequency. The output of the voltage to the current converter has a peak amplitude of 200mA shown in Fig.1.7 (b).

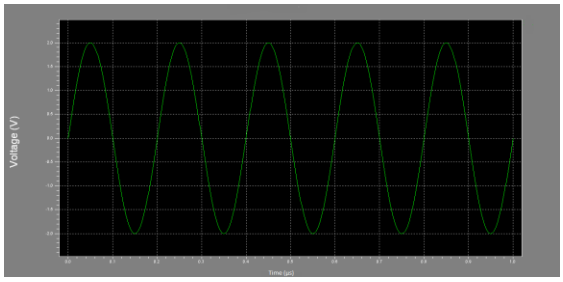

Fig.1.7 (a) Input voltage

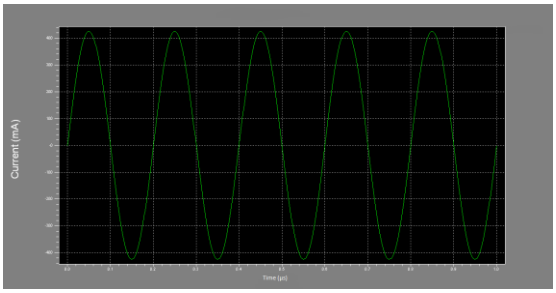

Fig.1.7 (b) Output current

1.11 Power usage – The input voltage ranges from 1.2 to 3.3V and so the electricity expended will be collected at various supply voltage levels. Table 2 displays the values

of the electricity used with the various values of the supply voltage.

1.12 RMS-DC converter-The planned RMS-DC converter circuit contains (a) squarer (b) low-pass filter[7]. Everything built on the basis of the use of CMOS transistors operating in a weak inversion field.

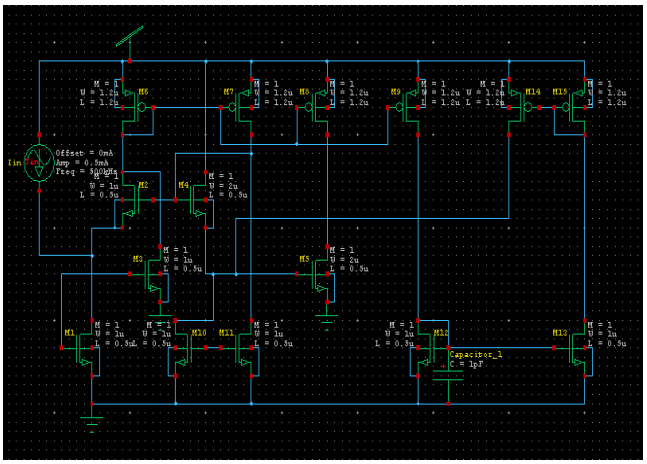

Fig.1.8. Schematic diagram of RMS to DC converter circuit

1.13 Design simulation- The circuit was simulated using T-Spice with 180 nm of TSMC CMOS cycle parameters. Vdd=1.6V, C=10 µF was used. Fig.4.9 (a) indicates the time-response of the voltage to the current converter for a sinusoidal input voltage of 20 µA peak amplitude and 5 MHz frequency. The DC current output of the voltage to the current converter is 7.6 µA, seen in Fig.1.9 (b).

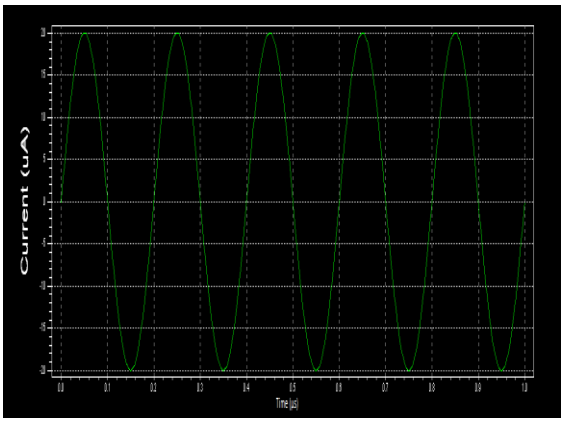

Fig.1.9 (a) Input current

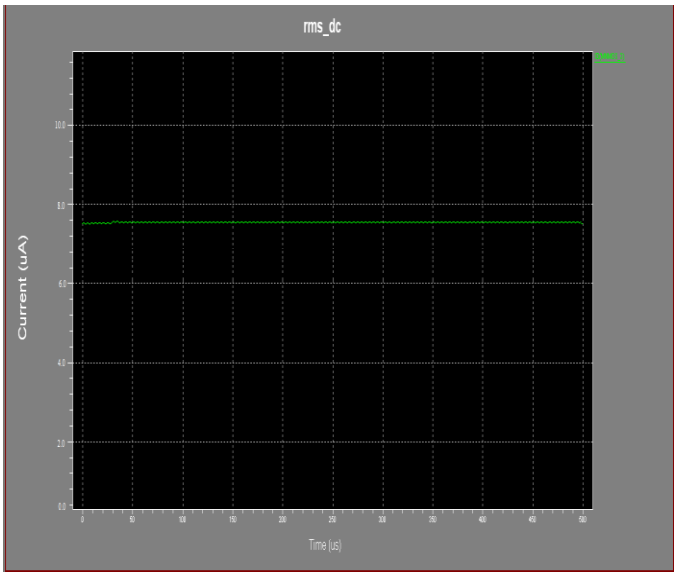

Fig.1.9 (b) output current

1.14 Power consumption

The input voltage ranges from 1.2 to 3.3V and it is possible to receive the electricity used at various supply voltage levels. Table 3 displays the proportions of the electricity used with the various values of the supply voltage.

Table 1: Power consumption with different supply voltage

VDD (in Volts**)**	**POWER CONSUMPTION (**in Watts**)**
1.2	1.6228e-003
1.6	3.1780e-003
2.0	5.0125e-003
2.4	7.3125e-003
2.8	1.0516e-002
3.3	1.6080e-002

1.15 Divider

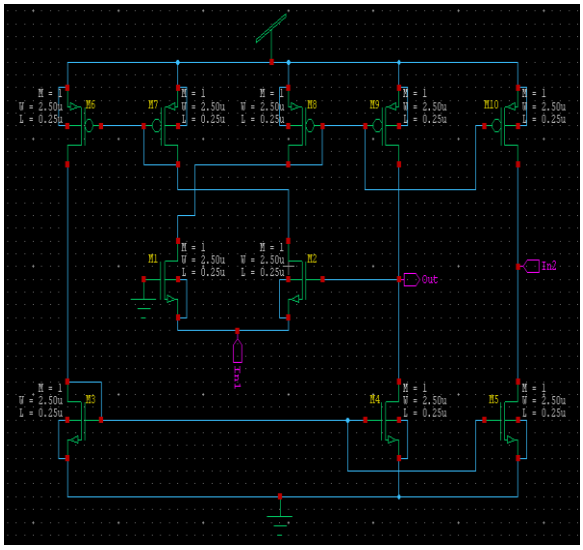

Fig.1.10. Schematic diagram of divider circuit

Analog dividers are used for the mathematical operation of the division of two signals (voltage or current). The idea is shown in the figure above, where all transistors are working in the current saturation mode[11]. In this MOS resistor, M3-M4, M6-M7 and M8-M9 are the current mirror pairs. M5 and M10 are MOS resistor output stage transistors. The output resistance seen through terminal B in the grounded resistor (Input A grounded) is equal to Rout. Input current In2 is applied and the output voltage gives the divisor function specified$V_{out} = In * R$

$$V_{out} = K_{div} \frac{In2}{In1}$$

The circuit was simulated using T-Spice with 180nm TSMC CMOS process parameters Vdd=1.6V were employed.

1.16 Complete schematic diagram of proposed FVC

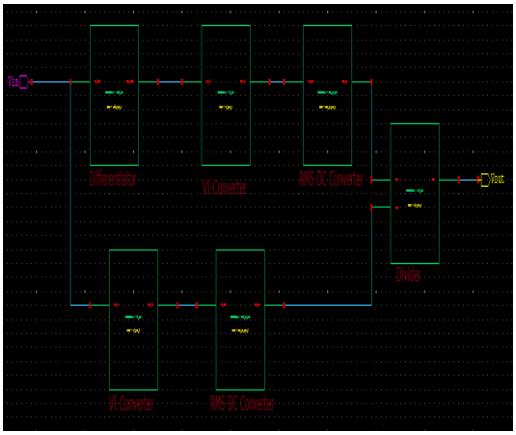

Fig.1.11: Complete schematic diagram of FVC circuit

The figure shown above is the full schematic diagram of the proposed circuit. This is a clear example of how we have applied our circuit and the different parts of it. The schematic diagram consists of a differentiator, two voltages to a current converter, two RMS-DC converters, and a divider as seen in the figure above.

1.17 Simulation of design-The circuit was simulated using T-Spice with 180 nm CMOS process parameters, Vdd=1.6V has been hired. Fig. 1.12(a) displays the frequency response time to the voltage converter for the sinusoidal input voltage of 2V peak amplitude and 5 MHz frequency. The value of the frequency to the voltage converter is 2.35 V DC voltage displayed in Fig.1.12(b).

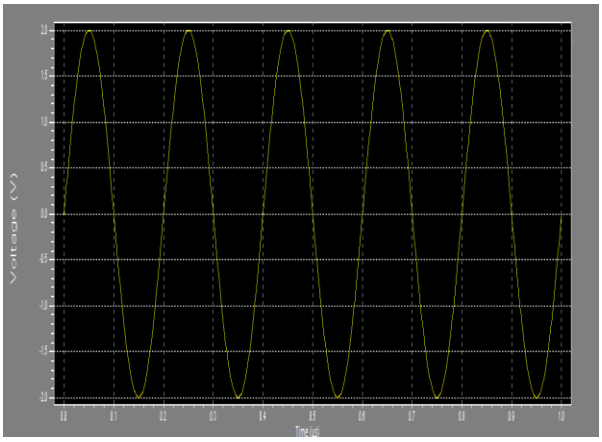

Fig.1.12 (a) Sinusoidal Input of FVC Circuit

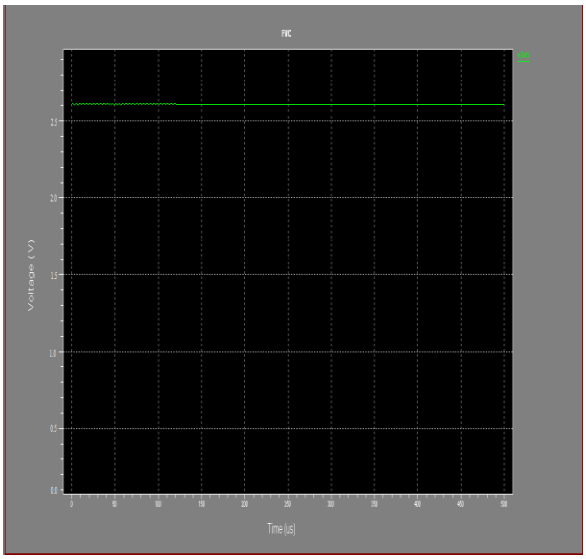

Fig.1.12 (b) DC output of FVC Circuit

The simulation result shown in Fig.1.12(b) shows that the output of the proposed FVC is pure DC without ripples.

1.18 Power consumption-The input voltage ranges from 1.2 to 3.3V and then the electricity used at various supply voltage levels can be measured. Table 2 displays the values of the electricity used with the various values of the supply voltage.

The following table shows that the planned FVC has low power consumption, low power supply voltage and a broad input frequency spectrum.

Table 2: Power consumption with different supply voltage

VDD (in Volts)	**POWER CONSUMPTION** (in Watts)
1.2	4.4800e-003
1.6	1.3444e-003
2.0	3.0668e-003
2.4	5.6616e-003
2.8	9.1418e-003
3.3	1.4739e-002

1.19 Eye diagram analysis

An eye diagram is a timing measurement device that gives you a clear picture of timing and stage mistakes. Errors, like jitter, are impossible to measure in real life because they change too much and are too tiny. The eye diagram is also an ideal method for determining the highest jitter, as well as calculating aberrations, rise periods, dropping periods and other defects. When these errors increase, the white space in the middle of the eye diagram reduces.

An eye diagram is formed by overlaying the various segments of the visual signal. It will include any possible bit series from basic high to low transitions to isolated transitions after long consistency runs. This appears like an pupil when overlapped. Face diagrams provide a tactile means of recognizing the quality of the concept signal. Keep in mind that the eye diagram displays parametric signal detail, but does not recognize logical or protocol issues, such as when it is expected to receive a high signal but sends a low signal. Figure1.13 displays the common jargon for an eye diagram.

A. One level, also called one level, is the key attribute in high logic. The estimated high-level value is based on the mean value of all data measurements obtained in the middle 20% of the eye period.

B. Zero level, also called zero level, is the key attribute in weak logic. This degree shall be calculated in the same area as the high level.

C. The magnitude of the eye diagram is the difference between the high and the low point.

D. The bit time, also referred to as the unit interval (UI), is a calculation of the horizontal opening of the eye diagram at the point of crossing of the eye. It's the opposite of the data size. By making eye diagrams, using the bit length on the horizontal axis instead of time, you can conveniently correlate diagrams of various data levels.

E. The vertical opening of the eye diagram is the height of the eye. Ideally, this would be equal to amplitude, but it rarely happens in the real world because of noise. As such, the height of the eye is smaller the more noise in the system. The height of the head reflects the signal-to - noise ratio.

F. The breadth of the eye is the horizontal opening. It is measured as the difference between the average mean of the crossing points of the head.

G. Eye crossing proportion indicates duty cycle interference or pulse synchronization issues. The ideal signal is 50%; as the percentage deviates, the eye closes and indicates signal degradation.

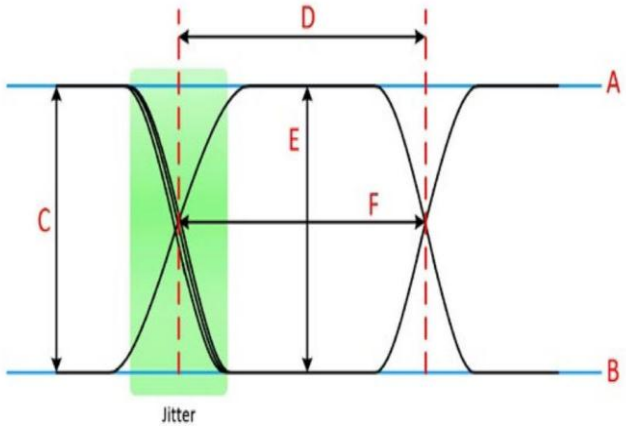

Fig.1.13: The image shows the high level (A), low level (B), amplitude (C), bit period (D), eye height (E), eye width (F), and eye crossing percentage (G) on an eye diagram

A. The time change in the figure is the sum of the actual periods of change. The slope shows the magnitude of the timing error; the lower the better.

B. Fall time in the figure is the sum of the actual dropping periods. The slope shows the magnitude of the timing error; the lower the better.

C. The signal-to - noise level at the sample stage is from the eye width to the edge or from the rational high-voltage spectrum**.**

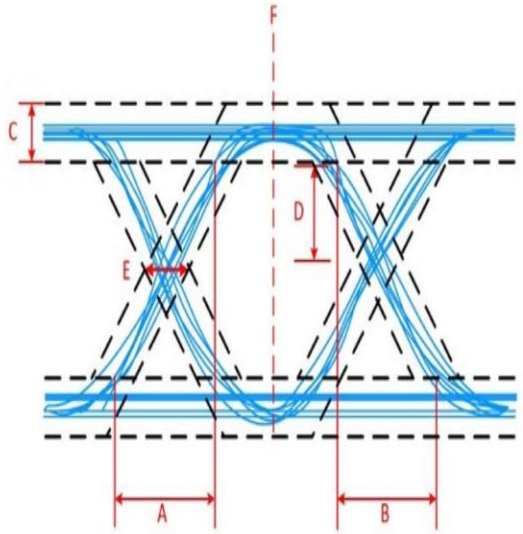

Fig.1.14: The image shows the rise time (A), fall time (B), distortion (C), signal-to-noise ratio (D), jitter (E), and best time to sample (F) on an eye diagram

1.20 Eye pattern of FVC

MATLAB simulated eye pattern result of FVC and corresponding parameters observed at 5MHz sampling frequency is shown below.

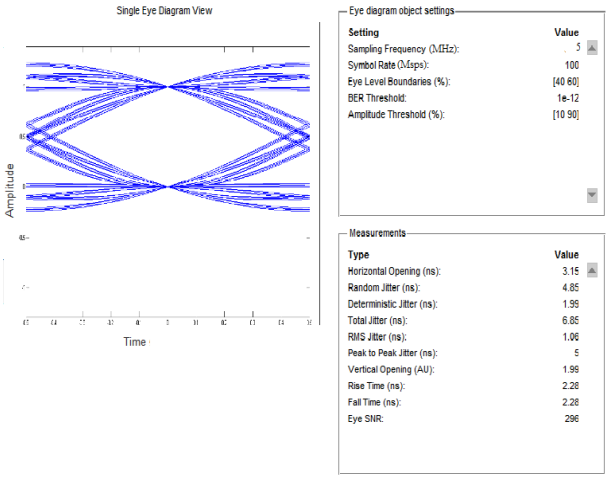

Fig.4.15: Eye pattern result of FVC at 5 MHZ

However, this concept does not benefit us much, so to clarify what the wavelet analysis so wavelet transforms is a better approach.

CONCLUSION

In the proposed analysis, two different FVC models were developed based on the same principle. As no external integrators are required, it is therefore superior to the conventional FVC due to no initial value effect. Model-1 indicates that the output is linearly proportional to the input frequency. The circuit demonstrates both the theoretically and experimentally effective conversion of the sinusoidal signal frequency to the output voltage with fast response time, low ripple and high linearity (< 0.25%) of up to 5 MHz. In Model-II, it is also noted that the output generated is linearly proportional to the input frequency. Of this function, we have calculated the power consumption of each circuit with various supply voltages varying from 1.2 volts to 33 volts, according to which the proposed system efficiency is sufficient with the low single A 1-V single-mode booster converter in the 3.3/5-V model. 0.6-m CMOS deposition, providing 85 percent power conversion Efficiency at 100 mA output current This paper was verified by laboratory testing. Development of a high-precision (94 per cent) inductor-current sensing device, low-voltage VCO and converter that delivers excellent performance. The regulation of voltage also at 1-V supply has been solved. In addition, the start-up circuit to solve sub-1-V start-up problems has already been published. In addition, low-voltage circuits are not only useful for boost-converter architecture, they are also flexible.

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