AN OPTICAL DESIGN, SIMUALTION AND FEASIBILITY STUDY OF PHOTONIC CRYSTALS USING LOGIC GATES

Mr.K.Seetarama Raju*, M.Priyanka[1], N.Venkatesh[2], K.Harsha Kumar[3], K.Akshay Kumar[4]

*Assistant Professor, Department of ECE, Godavari Institute of Engineering and Technology, Rajahmundry, Andhra Pradesh, India

[1,2,3,4]Student, Department of ECE, Godavari Institute of Engineering and Technology, Rajahmundry, Andhra Pradesh, India

---***---

Abstract: *In this paper, an all-optical logic gates like AND, OR and XOR gates is proposed using two- dimensional photonic crystals. The structure is based on principle of beam-interference, using square lattice of plus-shaped waveguides with silicon dielectric rods in air background. The design size is as small as 13a × 13a which makes very compact and efficient, therefore proposed design is suitable for photonic integrated devices. The performance of the device is analyzed using finite-difference-time-domain (FDTD) method.*

Key Words: photonic crystal, logic gates, T-shaped waveguide, beam-interference, FDTD.

1. INTRODUCTION

From the past decade, technology is playing a major role in development of a mankind. How we perceive and get information from the world. Energy is the only way of connection. This energy contains data and information, without this medium there is no communication. Electromagnetic waves are the most important conveyors of energy. But these waves have some disadvantages like signal tapping, loss of data. Optical communication plays a foremost role in future communication using Photonics [1]. Photonic crystals involved the major interest of the researchers because of their capability in controlling electromagnetic waves. PhC's have some unique features such as high speed [2], low power consumption [3] and electromagnetic radiations. In PhCs, control of light flow is done by line and point defects [4]. Point defects are introduced for resonator, whereas line defects are intended for waveguides [5].

All-optical logic gates [6-9] are used for various combinational circuits and sequential circuits, so they are key functional elements in optical signal processing. In order to design these logic gate several techniques such as photonic crystal ring resonator (PCRR) [10], plasmonic waveguides [11], Mach-zender interferometer (MZI) [12] and semiconductor optical amplifier (SOA) [13] etc., are used but these include some limitations such as high latency, large in size [14], less compatibility, so we have chosen beam-interference technique [15]. To our best knowledge by using photonic concept we propose a design of plus-shaped waveguide of square type lattice with silicon dielectric rods in air background. By optimizing the radius of the junction rods, a good contrast ratio with less reflection is obtained. The device performance is simulated and verified using finite-difference-time-domain (FDTD) method.

This paper is systematized as follows. Section 2 describes the design and operating principle of proposed structure. Section 3 deals with discussion on the simulation results. Section 4 concludes the proposed work.

2. DESIGN AND OPERATING PRINCIPLE

The design of all-optical logic gates is plus-shaped waveguide as shown in Fig. 1 and operates at a wavelength of 1.55 µm. The size of the wafer is 7.8 µm × 7.8 µm which may be the smallest photonic crystal logic gate that has ever been proposed. The radius of silicon dielectric rods is 0.2a; where 'a' is a lattice constant of value 0.6 µm and refractive index of these rods is set to 3.45. By optimizing the radius of the junction rods to 0.10266a, we can achieve better output power levels with less reflection for the respective input combinations. In this structure, there are two input ports 'A' and 'B' on left and right side of the plus-shaped waveguide, one reference port 'R' at bottom is introduced which help to provide the output power when both the input are logic '0' and one output port 'Y' at top of the plus-shaped waveguide.

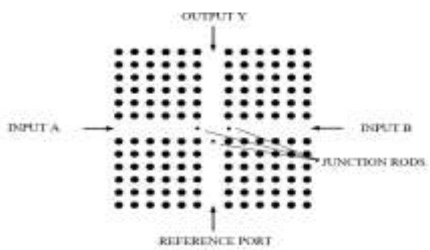

Fig. 1: Layout of proposed all-optical logic gates

The working of this device is based on principle of beam-interference. According to theory of wave optics, the constructive interference occurs when two optical light beams differ by a phase difference of 2kπ (where k = 0, 1, 2,….). Similarly, the destructive interference occurs, when two optical light beams differ by a phase difference of (2k+1)π (where k = 0, 1, 2,….). The performance of the device is optimized by choosing lattice constant 0.6 µm,refractive index 3.45 and silicon rod radius 0.2a which provides contrast ratio of 20.18dB, 11.56dB and 8.04dB for AND, OR, and XOR gates, respectively.

3. OPTIMIZATION OF REFRACTIVE INDEX,LATTICE CONSTANT AND SILICON ROD RADIUS

All-optical logic gates operation is verified by varying refractive index from 3.47 to 3.5 and noted intensity of light for different input levels as shown in Tables 1, 2 and 3 i.e., for AND, OR and XOR.

Table 1: Intensity of light across output Y for different refractive index values of AND gate

AND				
Refractive Index	A=0, B=0	A=0, B=1	A=1, B=0	A=1, B=1
RI = 3.47	0.164	0.055	0.028	1.9
RI = 3.38	0.236	0.047	0.068	2.134
RI = 3.45	0.164	0.164	0.023	2.4
RI = 3.50	0.131	0.321	0.0258	1.653

Table 2: Intensity of light across output Y for different refractive index values of OR gate

OR				
Refractive Index	A=0, B=0	A=0, B=1	A=1, B=0	A=1, B=1
RI = 3.47	0.164	0.802	0.835	1.9
RI = 3.38	0.236	0.820	1.045	2.134
RI = 3.45	0.164	0.8	0.854	2.4
RI = 3.50	0.131	0.810	0.57	1.653

Table 3: Intensity of light across output Y for different refractive index values of XOR gate

XOR				
Refractive Index	A=0, B=0	A=0, B=1	A=1, B=0	A=1, B=1
RI = 3.47	0.164	0.80	0.835	0.1439
RI = 3.38	0.236	0.820	1.045	0.148
RI = 3.45	0.164	0.8	0.854	0.134
RI = 3.50	0.131	0.820	0.579	0.309

According to obtained values we have chosen better refractive index of 3.45 which gives high contrast ratio. Below Tables 4, 5 and 6 represents about lattice constant that differs from 0.58 to 0.62 based on the selected refractive index.

Table 4: Intensity of light across output Y for different lattice constant values of AND gate

AND				
Lattice constant	A=0, B=0	A=O B=1	A=1 B=0	A=1 B=1
a = 0.58	0.211	0.002	0.027	1.616
a = 0.6	0.164	0.164	0.023	2.4
a = 0.62	0.141	0.101	0.037	1.257

Table 5: Intensity of light across output Y for different lattice constant values of OR gate

OR				
Lattice constant	A=0, B=0	A=0 B=1	A=1 B=0	A=1 B=1
a = 0.58	0.211	0.825	0.692	1.616
a = 0.6	0.164	0.8	0.854	2.4
a = 0.62	0.141	0.101	0.037	1.257

Table 6: Intensity of light across output Y for different lattice constant values of XOR gate

XOR				
Lattice constant	A=0, B=0	A=0 B=1	A=1 B=0	A=1 B=1
a = 0.58	0.211	0.825	0.692	0.331
a = 0.6	0.164	0.8	0.850	0.134
a = 0.62	0.141	0.764	0.483	0.507

The high contrast ratio is obtained at lattice constant 0.6µm. Similarly, silicon rod radius values are also varied 0.15a to 0.22a based on the selected lattice constant and refractive index.

Table 7: Intensity of light across output Y for different silicon rod radius values of AND gate

AND				
Radius	A=0, B=0	A=0 B=1	A=1 B=0	A=1 B=1
r = 0.15a	0.290	0.04	0.018	2.50
r = 0.17a	0.237	0.049	0.037	2.153
r = 0.2a	0.164	0.164	0.023	2.4
r = 0.22a	0.112	0.021	0.001	1.26

Table 8: Intensity of light across output Y for different silicon rod radius values of OR gate

OR				
Radius	A=0, B=0	A=0 B=1	A=1 B=0	A=1 B=1
r = 0.15a	0.29	0.04	0.018	2.50
r = 0.17a	0.238	0.933	1.207	2.513
r = 0.2a	0.164	0.8	0.854	2.4
r = 0.22a	0.112	0.572	0.496	1.26

Table 9: Intensity of light across output Y for different silicon rod radius values of XOR gate

XOR				
Radius	A=0, B=0	A=0 B=1	A=1 B=0	A=1 B=1
r = 0.15a	0.290	0.94	1.304	0.1317
r = 0.17a	0.238	0.93	1.207	0.120
r = 0.2a	0.164	0.8	0.854	0.134
r = 0.22a	0.112	0.57	0.500	0.158

Finally from the noted values we have chosen better rod radius value as 0.2a which has high contrast ratio.

4. RESULTS AND DISCUSSION

4.1 Simulation results of AND Gate

AND gate has four different input combinations. In three cases that is A=0, B=0; A=0, B=1 and A=1, B=0 the output is logic '0' so it has minimum probability to get any error. In one case that A=1, B=1 the output is logic "1" to reduce error the threshold value of logic "1" is set to 0.5. The contrast ratio for the proposed AND gate is 20.18dB. All results satisfy the truth table of AND gate as shown in Table 10.

Case (a): A = 0, B = 0

In this case, only reference signal is applied while at input port A and B there is no optical signal. Due to the junction rods, light is reflected back and very low intensity optical signal is obtained at output port Y which is considered as logic '0' as shown in Fig. 2(a).

Case (b): A = 0, B = 1

For the case logic '01', no input pulse is applied at input port A and at input port B logic '1' is applied with phase 180°. The phase of the reference input port is 180°, so destructive interference will occur with minimum optical light pulse at output port Y which can be considered as logic '0' as shown in Fig. 2(b).

Case (c): A = 1, B = 0

For the case logic '10', the input pulse is applied at the input port A with phase 0° and no input pulse is applied at the input port B. Phase of the reference input port is 180°, again destructive interference will occur and the light pulse will not propagate towards the output port Y which can be considered as logic '0' as shown in Fig. 2(c).

Case (d): A = 1, B = 1

In this case logic'1' is applied at both the input ports A and B with a phase of 0° and 180° respectively. The input pulse is also applied at the reference input port with a phase of 0°. For this case constructive interference will takes place and at the output port Y, a strong optical light pulse is observed which can be considered as logic '1' as shown in Fig. 2(d).

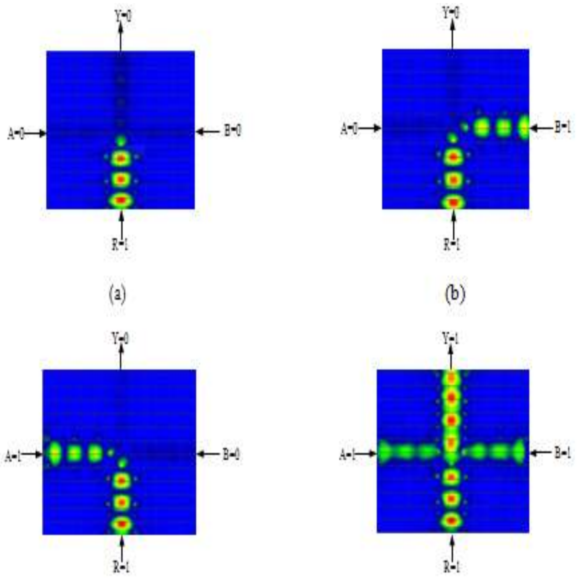

Fig. 2: Field distribution of AND gate for input combinations (a)00 (b)01 (c)10 (d)11

Table 10: Truth table for AND gate where output Y is in terms of input power P

Input (A)	Input (B)	Output (Y)	Normalized Power
0	0	0	0.164
0	1	0	0.023
1	0	0	0.164
1	1	1	2.4

4.2 Simulation results of OR Gate

OR gate has four different input combinations. In one case that is A=0, B=0 the output is logic '0' so it has minimum probability to get any error. In three cases that A=0, B=1; A=1, B=0 and A=1, B=1 the output is logic "1" to reduce error the threshold value of logic "1" is set to 0.5. The contrast ratio for the proposed OR gate is 11.56dB. All results satisfy the truth table of OR gate as shown in Table 11.

Case (a): A = 0, B = 0

In this case, only reference signal is applied while at input port A and B there is no optical signal. Due to the junction rods, light is reflected back and very low intensity optical signal is obtained at output port Y which is considered as logic '0' as shown in Fig. 3(a).

Case (b): A = 0, B = 1

For the case logic '01', no input pulse is applied at input port A and at input port B logic '1' is applied with phase 0°. The phase of the reference input port is 180°, so constructive interference will occur and optical light pulse is obtained at output port Y which can be considered as logic '1' as shown in Fig. 3(b).

Case (c): A = 1, B = 0

For the case logic '10', the input pulse is applied at the input port A with phase 180° and no input pulse is applied at the input port B. Phase of the reference input port is 180°, again constructive interference will occur and the light pulse will propagate towards the output port Y which can be considered as logic '1' as shown in Fig. 3(c).

Case (d): A = 1, B = 1

In this case logic'1' is applied at both the input ports A and B with a phase of 0° and 180° respectively. The input pulse is also applied at the reference input port with a phase of 0°. For this case constructive interference will takes place and at the output port Y, a strong optical light pulse is observed which can be considered as logic '1' as shown in Fig. 3(d).

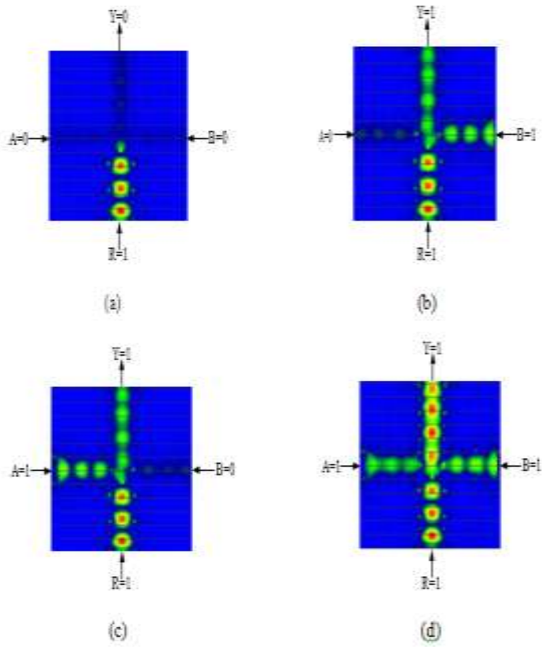

Fig. 3: Field distribution of OR gate for input combinations (a)00 (b)01 (c)10 (d)11

Table 11: Truth table for OR gate where output Y is in terms of input power P

Input (A)	Input (B)	Output (Y)	Normalized Power
0	0	0	0.164
0	1	0	0.8
1	0	0	0.854
1	1	1	2.4

4.3 Simulation results of OR Gate

XOR gate has four different input combinations. In two cases that is A=0, B=0 and A=1, B=1 the output is logic '0' so it has minimum probability to get any error. In three cases that A=0, B=1 and A=1, B=0 the output is logic "1" to reduce error the threshold value of logic "1" is set to 0.5. The contrast ratio for the proposed XOR gate is 8.04dB. All results satisfy the truth table of XOR gate as shown in Table 12.

Case (a): A = 0, B = 0

In this case, only reference signal is applied while at input port A and B there is no optical signal. Due to the junction rods, light is reflected back and very low intensity optical signal is obtained at output port Y which is considered as logic '0' as shown in Fig. 4(a).

Case (b): A = 0, B = 1

For the case logic '01', no input pulse is applied at input port A and at input port B logic '1' is applied with phase 0°. The phase of the reference input port is 180°, so constructive interference will occur and optical light pulse is obtained at output port Y which can be considered as logic '1' as shown in Fig. 4(b).

Case (c): A = 1, B = 0

For the case logic '10', the input pulse is applied at the input port A with phase 180° and no input pulse is applied at the input port B. Phase of the reference input port is 180°, again constructive interference will occur and the light pulse will propagate towards the output port Y which can be considered as logic '1' as shown in Fig. 4(c).

Case (d): A = 1, B = 1

In this case logic'1' is applied at both the input ports A and B with a phase of 0° and 0° respectively. The input pulse is also applied at the reference input port with a phase of 0°. For this case destructive interference will takes place and at the output port Y no optical light pulse is observed which can be considered as logic '0' as shown in Fig. 4(d).

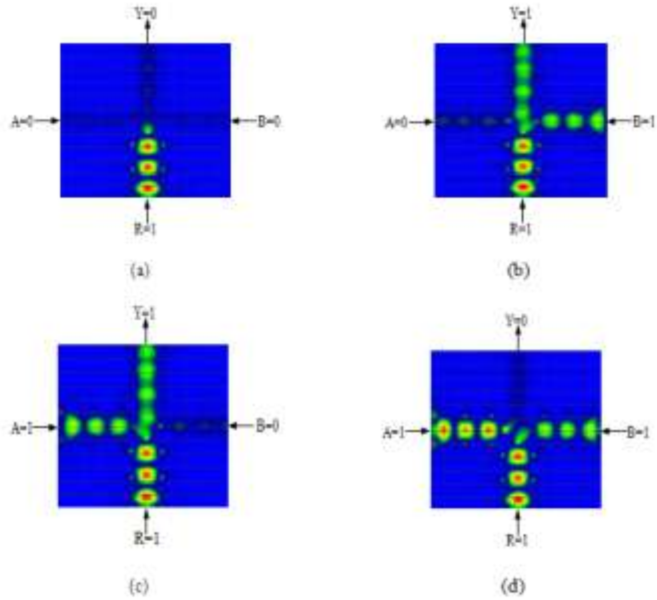

Fig. 4: Field distribution of XOR gate for input combinations (a)00 (b)01 (c)10 (d)11

Table 12: Truth table for XOR gate where output Y is in terms of input power P

Input (A)	Input (B)	Output (Y)	Normalized Power
0	0	0	0.134
0	1	0	0.8
1	0	0	0.854
1	1	1	0.164

An all-optical logic gate is verified for different refractive index varied from 3.35 to 3.5. The device provides better contrast ratio at refractive index of 3.45 as shown in Fig. 5. The design is also optimized by varying lattice constant from 0.58 to 0.62 and it is observed that 0.6 μm is the best lattice constant for the proposed structure; as shown in Fig. 6. The contrast ratio value has been calculated at each value of the rod radius from 0.08a to 0.14a as shown in Fig. 7. The radius of rod at which a high contrast ratio achieved is 0.2a. In Fig. 5, 6, 7 '00' indicates the power level at the output port Y when no input is applied at port A and port B. '01' indicates the power level at the output port Y when a single input is applied at port B. '10' indicates the power level at the output port Y when a single input is applied at port A. Similarly, '11' is the power level at the output port Y when the light beam is applied to both the input ports A and B.

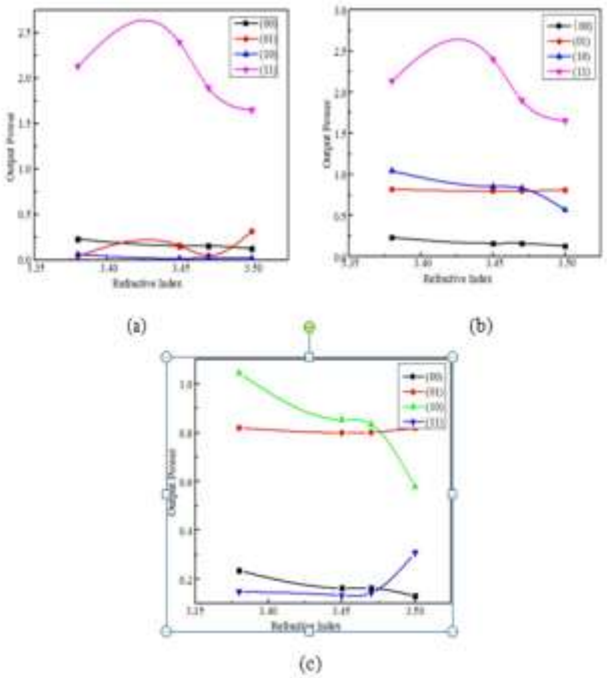

Fig. 5: Graphical representation of varying refractive index for (a) AND (b) OR (c) XOR

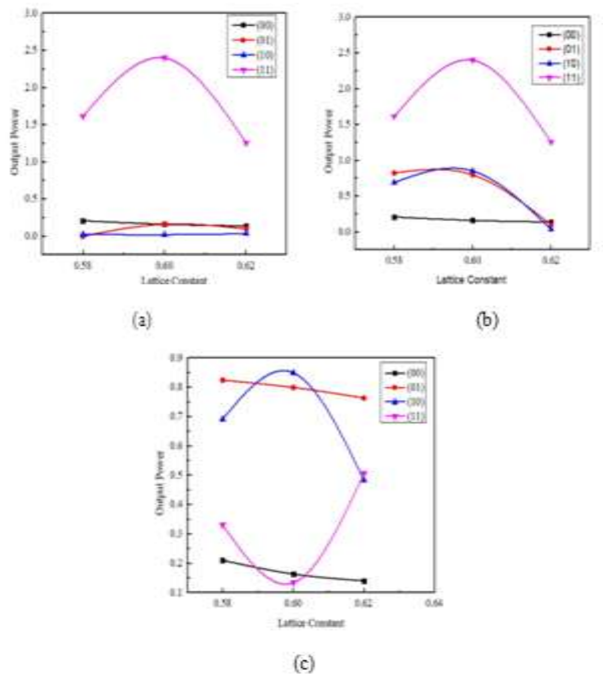

Fig. 6: plot of lattice constant vs normalized power for (a) AND (b) OR (c) XOR

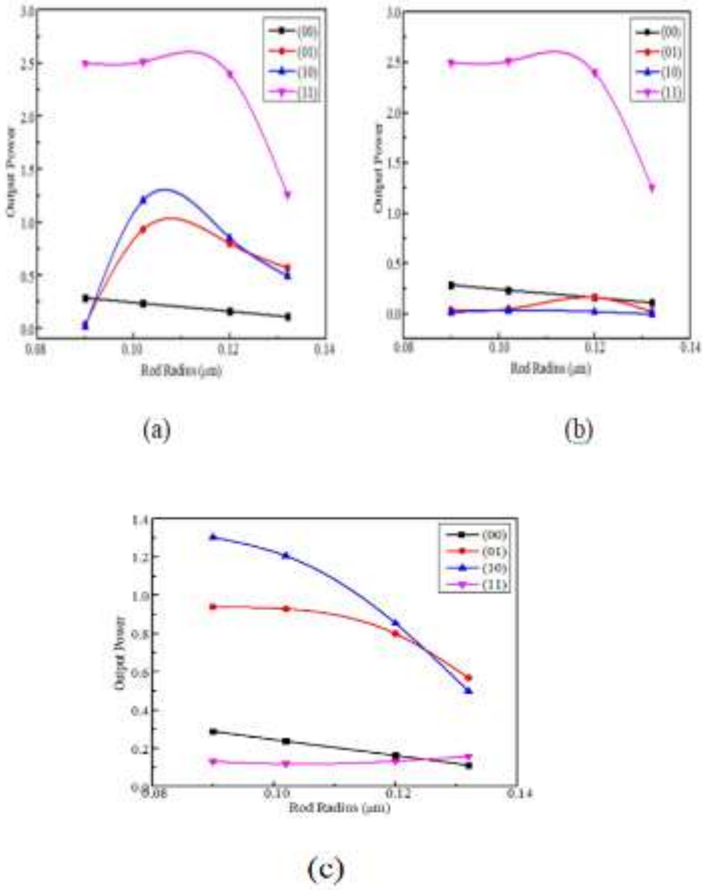

Fig. 7: The spectrum of varying rod radius for (a) AND (b) OR (c) XOR

5. CONCLUSION

In this paper, optical logic gates are designed using plus-shaped waveguide in two-dimensional square lattice photonic crystals of Si rods in air substrate. To reduce back reflection of light the radius of the junction rods is optimized. The proposed structure is very small, simple and no other non-linear material is used as they can be applied for the chip-level integration. The device structure have been simulated using FDTD method, which were resulted with the contrast ratio of 20.18dB, 11.56dB and 8.04dB for AND, OR, and XOR functions. This device has many applications such as demultiplexer/multiplexer, adder, subtractor, comparator, encoder, decoder etc.

REFERENCES

[1]. H. T. Mouftah, M. H. Elmirghani, "Photonic switching technology", IEEE press, New York, 9-10, 1999.

[2]. P. Rani, K. Yogita, R. K. Sinha, "Realization of AND gate in Y-shaped photonic crystal waveguide", Opt. Comm, 298–299, 227–231, 2013.

[3]. J. D. Joannopoulos, S. G. Johnson, J. N. Winn, R. D. Meade, "Photonic Crystal: Molding the Flow of Light", Princeton University Press, Princeton, 1995.

[4]. T. Baba, D. Mori, K. Inoshita, Y. Kuroki, "Light localizations in photonic crystal line defect waveguides", IEEE J Quantum Electron, 10: 574–590, 2004.

[5]. C.J. Wu, C. P. Liu, Z. Ouyang, "Compact and low power optical logic NOT gate based on photonic crystal waveguides without optical amplifiers and nonlinear materials", Appl Opt, 51: 680–85, 2012.

[6]. T. M. Geshiro, T. Kitamura, K. Nishida, S. Sawa, "All-optical logic gates containing a two- mode nonlinear waveguide", IEEE J Quantum Electron, 38: 37–46, 2002.

[7]. C. Porzi, M. Guina, A. Bogoni, L. Poti, "All-optical NAND/NOR logic gates based on semiconductor saturable absorber etalons", IEEE J Sel Top Quantum Electron, 14: 927–937, 2008.

[8]. M. D. Nirmala, M. Vincent, "Interference based square lattice photonic crystal logic gates working with different wavelengths", Opt. Laser Technol, 80: 214–219, 2016.

[9]. X. S. Christina, A. P. Kabilan, P.E. Caroline, "Design of optical logic gates using self- collimated beams in 2D photonic crystal", Photonic Sensors, 2: 1–4, 2012.

[10]. J. Bao, J. Xiao, L. Fan, X. Li, Y. Hai, T. Zhang, C. Yang, "All-optical NOR and NAND gates placed on photonic crystal ring resonator," Opt. Comm, 329: 109–112, 2014.

[11]. Santosh kumar, Lokendra singh, Sandip swarnakar, "Design of one bit magnitude comparator using nonlinear plasmonic waveguides", Plasmonic (springer), 12(2): 369-375, 2016. [12]. T. Yabu, M. Geshibo, T. Kitamura, K. Nishida, S. Sawa, "All-optical logic gates containing a two-mode nonlinear waveguide", IEEE J. Quant Elect, 38: 37–46, 2009.

[13]. X. L. Zhang, J. Q. Sun, D. M. Liu, D. X. Huang, "A novel scheme for XGM wavelength conversion based on single-port-coupled SOA", Chin. Phys, 10: 124-127, 2001.

[14]. M. Farhad, M. Saroosh, A. Hamed, F. Ebrahim, "Ultra-fast analog-to-digital converter based on a nonlinear triplexer and an optical coder with a photonic crystal structure", App. Opt, 56: 1799– 1806, 2017.

[15]. E. H. Shaik, N. Rangaswamy, "Improved design of all-optical photonic crystal logic gates using T-shaped waveguide"' Opt. Quantum Electron, 63(10): 11082-015, 2016.