Dual output Flyback converter with current mode control on primary side and synchronous buck converter at secondary side

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Abstract – *Many of the aerospace and defense applications need Switched Mode Power Supplies (SMPS). SMPS are small in size and deliver desired output voltage. Flyback converter topology has the ability to regulate multiple outputs. The project is intended to design and implement dual output flyback converter with current mode control on primary side and synchronous buck converter on secondary side. The width of the pulse is controlled by applying current mode control technique on primary side of the converter using UC1846 Current Mode (Pulse Width Modulation) PWM controller. The secondary of flyback converter implements buck converter for both the outputs by employing LT3845 for pulse generation. The proposed converter is operating with a switching frequency of 100kHz and delivers output voltages of +6.5V/1.5A and -6.5V/0.66A. The line and load regulation are improved. The converter also emphasizes on protection circuits like undervoltage and overvoltage protection. The hardware implementation of the converter validates the results.*

Key Words: SMPS – Switched Mode Power Supply, Flyback converter, Synchronous buck converter, Current Mode PWM controller, Line regulation.

1.INTRODUCTION

SMPS are extensively utilized in various fields like aerospace, military and space applications because of higher efficiency and small size. SMPS are categorized into isolated converters and non-isolated converters. The transformer helps in isolation between the primary source side and secondary load side. SMPS are highly reliable, efficient and perform well under changing conditions of environment [1]. These distinguished features combined with modern converters in power electronics, has enabled the usage of SMPS in various domains of military and aerospace fields [2].

The converter having multiple outputs is a good advantage because from a single unit of power supply module multiple outputs are derived. The flyback converter is suitable for the necessary specifications. Flyback converter is applicable for applications with low power. The parts count in the converter is less compared to other topologies [3].

The conventional voltage mode control senses the output voltage and compared with a reference signal and given to the switching device. It is a slow response loop. This paper employs current mode control technique on the primary side of the converter. This has a faster response time for changes in input voltages and results in better line and load regulation. In this work a converter is designed for 14W and the switching frequency of 100 kHz. The PWM controller employed for the main mosfet on primary is UC1846 and LT3845 is employed for synchronous buck converters on secondary side for both the outputs [4][5].

1.1 Current mode control

The conventional voltage mode control employs feedback control technique and controls the output voltage by controlling the duty cycle. The voltage mode control has very slow loop response. These drawbacks are overcome by implementing current mode control that has faster loop response. This control helps in meeting the line and load regulation of the converter. The stability and accuracy of the converter depends on the type of controller employed. This control is an inner control loop that senses the primary current and compares with the amplified error signal. The switching pulses for the MOSFET are generated according to the variation in input current. UC1846 Current Mode PWM controller is employed for generation of pulses for the switching device on primary of the converter [6].

1.2 Synchronous buck converter

The secondary side of the converter implements a synchronous buck converter for both the outputs. The diodes in buck converter are replaced with switches to improve the efficiency further. The pulses are generated through LT3845 IC. The output voltage is sensed and taken as feedback loop for the buck converter. The output current is also sensed through a current sense resistor. The sensed output current is feedback to the LT3845 IC. The synchronous operation of the switches reduces the losses due to diode that is replaced by a switch. The line and load regulation in a dual output converter is crucial because it is difficult to maintain the regulation of the converter [7].

2. BLOCK DIAGRAM

The proposed schematic of converter is illustrated in Fig 1.

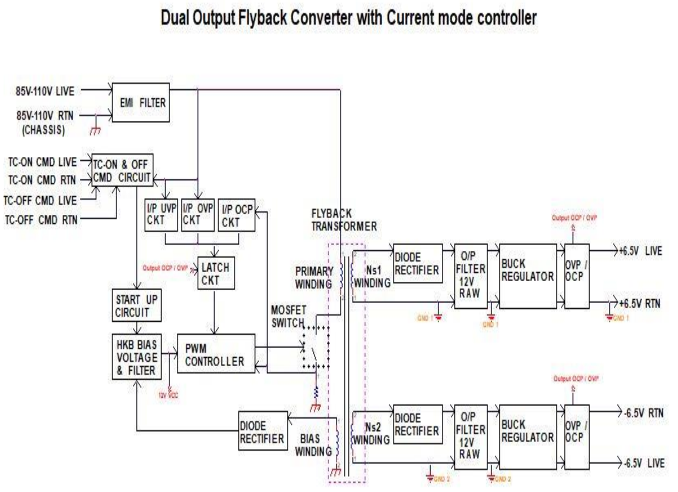

Fig 1: Schematic of proposed converter

The main input voltage is applied from LIVE and RTN through an EMI filter block. The main flyback transformer is connected between EMI filter and MOSFET. The main input supply is also connected to the protection circuits. If any of these protection circuits trigger, then the shutdown pin of IC will be triggered and it turns off the entire circuit. The transformer on the secondary is connected to buck converter through a diode rectifier circuit and output filter circuits. Similarly, there is another winding to give the second output of the converter. The converter delivers two outputs +6.5V/1.5A and -6.5V/0.66A.

The bias voltage is generated from the bias circuit. This is to power the PWM IC on the primary side of the flyback converter. The PWM IC provides gate pulses to MOSFET. The control used is current mode control. This technique uses current sense resistor to measure the current on primary side and compares it with amplified error signal to control the width of the pulse. The changes on the input side are affected in the primary current. Hence this current is also provided to the input over current protection in order to turn off when the current rises on the input supply side.

The secondary side of the converter has buck converter and before these converters there is a diode circuit and also the filter circuit present before giving the supply to buck converter. The buck converter is used to regulate the output voltage and improve the line and load regulation. The overvoltage protection (OVP) and overcurrent protection (OCP) circuits are present after the buck converter in order to detect any over voltages and over currents at the output and detects for any overcurrent and gives the signal to the shutdown pin of the IC. The shutdown pin of UC1846 turns off the entire converter.

The functions of various blocks are illustrated in Table 1.

Table -1: Functions of various blocks

SL. NO.	BLOCK	FUNCTION
1	EMI Filter	To eliminate noise
2	Turn on and off command	To turn and turn off the converter externally
3	Startup circuit	To provide supply to PWM IC until bias is generated
4	PWM controller	To generate pulses to the MOSFET
5	Protection circuits	To protect the converter from input overvoltage, over current and under voltages
6	Bias winding	To power the PWM IC and protection circuits
7	Buck regulator	To provide regulated output at output side
8	Output filter	To limit the ripple on output side
9	MOSFET	Switching device for flyback converter
10	Flyback transformer	To provide the isolation between load and input side
11	Diode rectifier	To rectify the output voltage at transformer secondary

The proposed converter specifications are specified as follows.

Minimum input voltage (Vin_{min})	: 90V
Nominal input voltage	: 100V
Maximum input voltage (Vin_{max})	: 110V
Output Voltage V_{out}	: +6.5V, -6.5V
Output current I_{out}	: 1.5A, 0.66A
Efficiency	: >70%
Line regulation	: ±1%
Load regulation	: ±1%
Maximum voltage Ripple	: 300mV

3. DESIGN OF COMPONENTS

The transformer chosen has a cross sectional area A_c = 23.2mm² and flux density Bm of 0.15T.

- Calculation of turns ratio

$$T_{ratio1} = \frac{|V_{out1}|+VD1}{V_{in(min)}} * \frac{(1-D)}{D} = 0.205 \quad (1)$$

$$T_{ratio2} = \frac{|V_{out2}|+VD2}{V_{in(min)}} * \frac{(1-D)}{D} = 0.205 \quad (2)$$

- Calculation of turns on primary

$$N_P = \frac{L_P * I_{PP}}{B_m * A_C * 10^{-6}} = 100 \quad (3)$$

- Calculation of turns on secondary

$$N_{s1} = T_{ratio1} \times Np = 20 \quad (4)$$

$$N_{s2} = T_{ratio2} \times Np = 20 \quad (5)$$

- Calculation of output inductance

$$L = \frac{V_{out}.(1-D).T_s}{I_{out}.K} = 133\mu H \quad (6)$$

- Calculation of output capacitance

$$C = \frac{K.I_{out}}{8 * F_{sw} * \Delta V} = 10\mu F \quad (7)$$

4. HARDWARE IMPLEMENTATION

The proposed converter is implemented with the design that is proposed. The converter is on an eight layer printed circuit board. The PCB utilizes the eight layer board for heat transfer. Fig 2 shows the top view of the converter.

Fig 2: Top view of the converter

The bottom view of the PCB is shown in Fig 3.

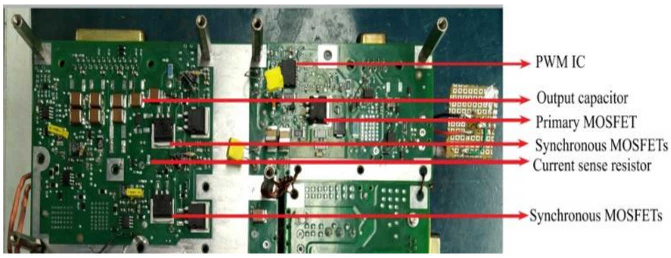

Fig 3: Bottom view of the PCB

The hardware test setup is shown in Fig 4.

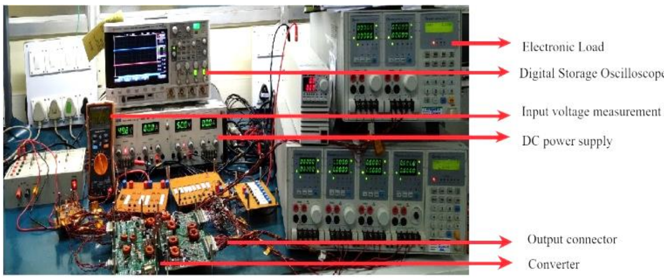

Fig 4: Hardware test setup

A DC power supply provides the input for the converter. The waveforms of various parameters and components are captured through a DSO. An electronic load is used to load the converter for various load conditions like minimum load, nominal load condition and maximum load condition. The output connectors are used in order to provide loading for the electronic load. The load condition is set before turning on the converter and input DC supply.

The supply is turned on and the turn on command is given to the converter in order to start the converter. The converter achieves desired results. The converter turn off command is used to turn off the converter.

5. RESULTS AND WAVEFORMS

The results obtained from the hardware setup are tabulated and the design specification for line and load regulation is less than 1%.

5.1 Efficiency

The converter efficiency is calculated for input voltage range of 90V to 110V. The converter efficiency is defined as

$$\eta = \frac{V_o * I_o}{V_{in} * I_{in}} * 100$$

The converter efficiency is calculated and is as shown in Table 2.

Table 2: Efficiency at 100% Load Condition

Input Voltage (volts)	Input Current (Amps)	Output Voltage (volts)		Efficiency (η) in %
		+6.5V/ 1.5A	-6.5V/ 0.66A	
90	0.21	6.55	-6.51	74.2
100	0.19	6.55	-6.51	73.8
110	0.17	6.56	-6.52	73.93

The experimental results of the converter prove that the converter efficiency is above 70% at full load condition for different input voltages. The converter has a maximum efficiency of 74% at full load condition.

5.2 Calculation of line and load regulation

The line regulation of the converter is given by

$$\%Line\ regulation = \frac{V_{out\ Max\_input} - V_{out\ Min\_input}}{V_{out\ Nom\_input}} \times 100$$

The line regulation for both the output voltages is as shown in Table 3.

Table 3: Line regulation

Load	Line regulation (%)	
	+6.5V/1.5A	-6.5V/0.66A
Full load	0.001	0.001
10% load	0.003	0.002

$$\%Load\ regulation = \frac{V_{out\ Min\_load} - V_{out\ Max\_load}}{V_{out\ Nom\ load}} \times 100$$

The load regulation of the converter for both inputs is as illustrated in Table 4.

Table 4: Load regulation

Input Voltage (volts)	Load regulation (%)	
	+6.5V/1.5A	-6.5V/0.66A
90	0.09	0.21
100	0.1	0.18
110	0.17	0.12

5.3 Output ripple voltage

Ripple voltage is the unwanted AC content present in the output DC voltage. In order to decrease the output ripple voltage, suitable capacitor is chosen with low ESR value. The ripple voltage is determined at full load condition for various input voltages is as shown in Table 5.

Table 5: Readings of Output ripple voltage

Input voltage (volts)	Output voltage (volts)		Ripple voltage (mV)	
	+6.5/ 1.5A	-6.5/ 0.66A	+6.5/1.5A	-6.5/ 0.66A
90	6.56	-6.51	92	84
100	6.55	-6.51	157	105
110	6.56	-6.52	165	92

5.4 Output hardware waveforms

The output ripple is captured on DSO for various input voltages. The output ripple voltage for the input of 90V is as shown in Figure 5.

Fig 5: Ripple voltage for 90V input

The output ripple voltage for input of 100V is as shown in Figure 6.

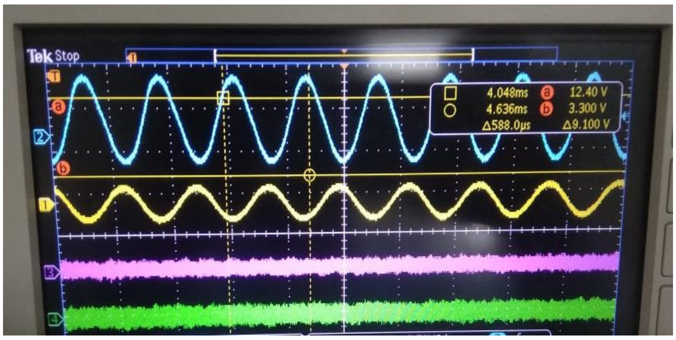

Fig 6: Ripple voltage for 100V input

The output ripple voltage for input of 110V is as shown in Figure 7.

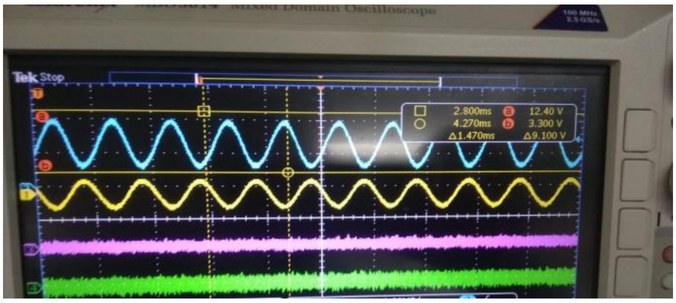

Fig 7: Ripple voltage for 110V input

The output voltage during startup is captured and is shown in Fig 8.

Fig 8: Output voltage of both the outputs during start-up

6. CONCLUSION

Current mode control on primary side and synchronous buck converter on the secondary side is implemented. The result analysis shows that the efficiency of the converter is greater than 70% and meets the specifications. The line and load regulation of the converter are less than ±1% and the output ripple voltage is below 300mV. The output voltage is constant for varying input voltage. The experimental results carried out validate and justify the design of the converter.

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