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5 – 15 Gbit/s Adaptive Continuous Time Linear Equalizers based on Statistic Eye Monitoring – A Survey

Sanjana V Ghate[1], Sahana B[2]

[1]*Sanjana V Ghate, Student, Dept. of Electronics and Communication Engineering, RV College of Engineering, Bengaluru – 59, Karnataka, India.*
[2]*Sahana B, Assistant Professor, Dept. of Electronics and Communication Engineering, RV College of Engineering, Bengaluru – 59, Karnataka, India.*

Abstract - *This paper provides an overview on evolved work in the recent years in the field of Continuous Time Linear Equalization. With the increase in data rates, the time interval available for data transmission has reduced leading to the effects like ISI, Skin Effect and noise introduction to the data as a result of which data obtained at the receiver gets degraded. Equalization is the signal conditioning technique to mitigate the channel effects of ISI and noise. CTLE is the technique implemented at receiver to boost the higher frequency signals to bring all frequency components of the signal to a similar amplitude, which in turn boosts jitter and eye-diagram performance. This brief presents review on three different CTLE architectures, their outcomes and their limitations.*

Key Words: **Adaptive CTLE, Capacitive Source Degeneration, Gain Boosting, pole zero adaptation, eye diagram**

1. INTRODUCTION

Data travelling through a channel at high speed is subjected to degradation through high frequency impairments such as reflections, dielectric loss and skin effect loss. These impairments reduce the signal quality making it difficult for a receiver to interpret it correctly. Equalization is a signal conditioning technique for signal conditioning in order to compensate for the distortions caused due to channel.

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2. REALIZATION OF CONVENTIONAL CTLE

In order to achieve the high pass behavior of equalizer, we need to have transconductance proportional to the frequency. The capacitive source degeneration circuit is shown in Fig-1 provides high gain at a frequency typically half the data rate.

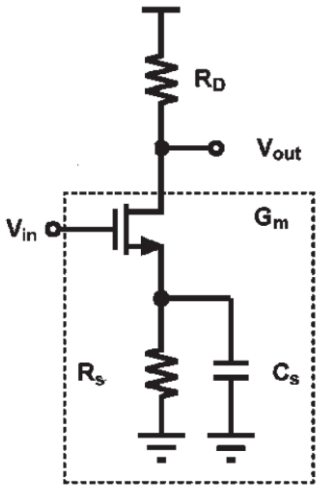

Fig-1: CS Amplifier with Capacitive Source Degeneration

At very low frequencies, the capacitor acts as open and hence the value of transconductance is given by,

$$\frac{i_d}{v_i} = \frac{g_m}{1+g_m R} \quad (1)$$

where i_d is the drain current, v_i is the gate input voltage, g_m is the transconductance and R is the source resistance.

At very high frequencies, the capacitor acts as short and hence the value of transconductance at very high frequencies is given by,

$$\frac{i_d}{v_i} = g_m \quad (2)$$

The frequency of the pole is given by,

$$\frac{g_m + \frac{1}{R}}{C} \quad (3)$$

where *C* is the source capacitance.

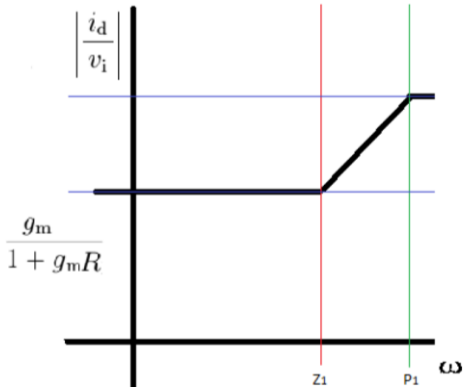

Fig-2: Plot of Transconductance vs Frequency

2.1 Differential Implementation of conventional CTLE

A fully differential CS amplifier with capacitive source degeneration is shown in Fig-3.

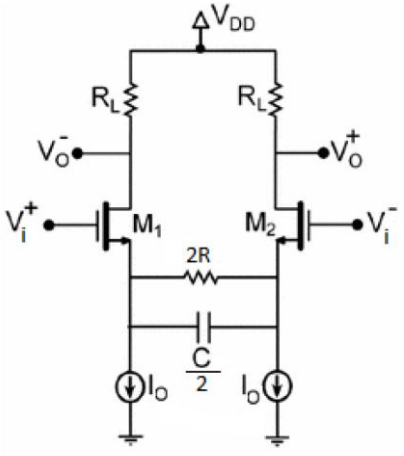

Fig-3: Differential Implementation of conventional CTLE

For the circuit shown if Fig-3, the transconductance is given by,

$$\frac{i_d}{v_i} = \frac{1}{2}\frac{g_m}{1+g_mZ} \tag{4}$$

where Z is given by,

$$Z = \frac{R}{1+sRC} \tag{5}$$

The gain of the amplifier is given by,

$$\frac{V_o}{V_i} = \frac{g_mR_L}{1+g_mZ} \tag{6}$$

where v_o is the output drain voltage.

At low frequencies, the amplifier gain is given by,

$$\frac{i_d}{v_i} = g_mR_L\frac{1+sRC}{1+g_mR_L+sRC} \tag{7}$$

where R_L is the load resistance.

At high frequencies, the transconductance is given by,

$$\frac{i_d}{v_i} = g_mR_L \tag{8}$$

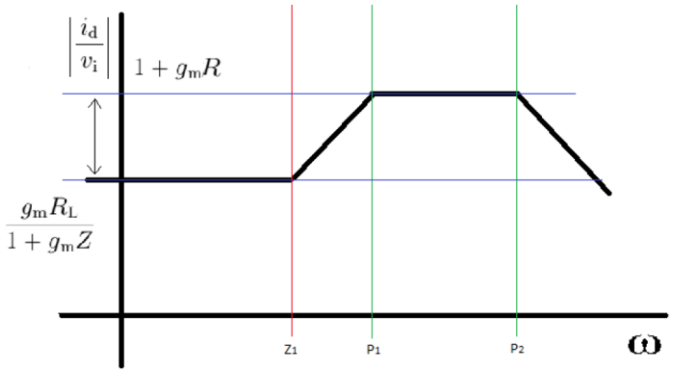

Fig-4: Transconductance vs Frequency

In reality, because of the existence of parasitic capacitances, there exists a minimum of two poles.

The plot of transconductance vs frequency for the circuit shown in Figure 3.32 depends on the occurrence of two poles in relation to the zero. For the scenario where poles are widely separated, the Fig-4: shows the plot. In the Figure, at a region between two poles disappear if the two poles are coincident. The maximum gain boosting at high frequency is given by,

$$\frac{Peak\ Gain}{DC\ Gain} = 1 + g_mR_L \tag{9}$$

which nullifies the attenuation provided by the channel at half the data rate (A generalized estimation is that the attenuation provided by the channel is 20 dB, at half the data rate. Therefore, the capacitive source degeneration amplifier provides a gain boosting of 20 dB in between occurrence of the zero and first pole so as to remove the channel effect.

In order to achieve a variable amount of gain, the resistors R, R_L and capacitor C can programmed to be variable.

2.2 Review on different CTLE architectures

The [1] presents an adaptation scheme based on the asynchronous under - sampling. The channel characteristics are first measured using a network analyzer and it is found that channel has about 5.9 to 15.7 dB loss at 2.7 GHz which is exactly half the data rate. The CTLE presented in this paper provides 4 - 18 dB with a precision of 1.4 dB compensation for channel loss. The implementation shown in Fig-5 has an active equalizing filter with capacitive source degeneration and adaptive circuits which consist of four track and hold circuits, a comparator, two digital-to-analog converters (DACs), a clock generator, and a digital controller [1]. The clock generator is made up of 5 stage inverter chain to generate clocks that are 5 different phases apart. These clocks are later used to perform asynchronous sampling in track and hold circuits. The amplitude levels of the incoming sampled data are compared with a reference voltage that is provided by a 5 bit DAC providing 32 amplitude levels. The decision on the received incoming data is made in a decision slicer.

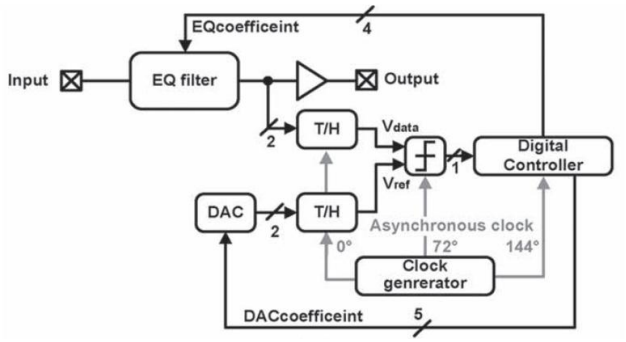

Fig-5: Block diagram of adaptive CTLE [1]

In [2], an adaptive CTLE that can vary its poles and zero locations based on the channel behavior is presented. The CTLE proposed consists of differential pair along with RC coupled source degeneration as shown in Fig-6. The resistors are connected in parallel with a ratio of 1:2:4:8. The resistor values are chosen based on the pole and zero requirement chosen by the pole-zero adaptation circuit. This arrangement provides 16 different combination of resistances and hence, 16 combinations of poles and zeros that provide different gains.

An inductor is added to provide an extra zero as shown. With the extra zero, the gain is given by,

$$\frac{-v_{out}}{v_{in}} = \frac{(g_{m1}+g_{mb1})(1+sC_{gs}R_g)\left[1+s\left(R_sC_s+\frac{R_s}{2}C_{in}\right)\right]}{\left[1+s\left(R_sC_s+\frac{R_s}{2}C_{in}\right)+(g_{m1}+g_{mb1})\frac{R_s}{2}\right]B} \quad (10)$$

where B is given by,

$$B = s^2C_{gs}C_LR_{gs} + s(C_{gs}+C_L) + g_{m2} + g_{mb2} \quad (11)$$

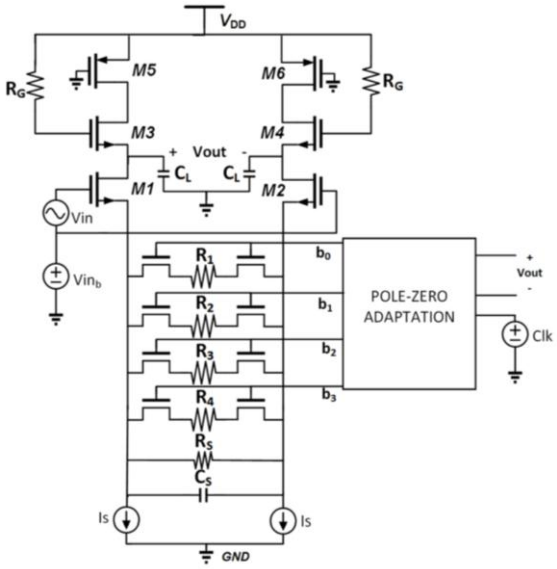

Fig-6: Schematic of adaptive CTLE [2]

The active inductors are designed from combination of M_3, M_5 and the resistor R_G and combination of M_4, M_6 and R_G. Since C_L is large, the parasitic capacitances due to M_1 and M_2 are neglected.

The pole-zero adaptation block is implemented in Verilog-A code and the differential output obtained from this block is sampled at positive edge of a clock whose frequency is half the signal frequency. This value is then compared with a reference signal. The channel loss at half the data rate, i.e 2.5 GHz is seen to be 6.8 dB. The circuit implemented can provide a gain upto maximum of 11 dB.

The paper [3] presents a common gate continuous time linear equalizer (CG CTLE) with charge mode adaptation with power supply of 1.1 V. The implementation is adaptive to the time varying ISI and it can operate in multi-loss environments. As compared to a conventional CTLE, the implemented architecture in [3] consumes less area. The implementation is shown in Fig-7.

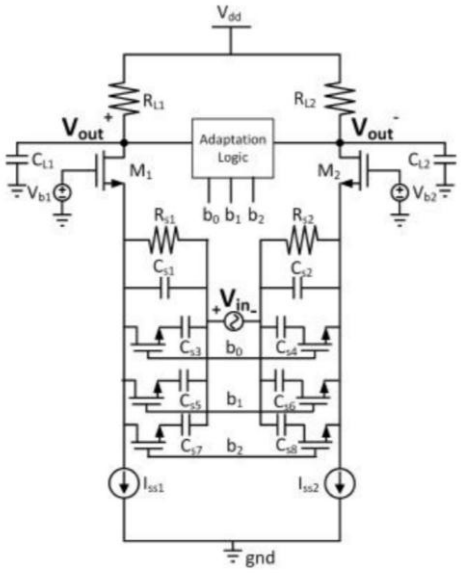

Fig-7: Schematic of Adaptive CTLE [3]

The CG CTLE has higher bandwidth and can compensate channel effects for higher data rates as compared to CS CTLE.

3. OBSERVATIONS

The results obtained from [1] are as follows: The adaptive equalization is measured using on-chip monitoring. The CTLE provides equalization for data rate of 5.4 Gbps with an asynchronous data sampling speed of 114 MHz. The total power consumption of the circuit is 35mW with a total area consumption of 0.18 sq.mm.

The CTLE presented in [2] operates at a data rate of 5 Gbps and provides a maximum of 11 dB gain boosting at 2.5 GHz. It is designed in 0.18um standard CMOS technology and consumes a power of 1.8 mW with a supply voltage of 1.8 V. Eye monitoring is used to check for the compensation values for the time varying channel properties. The jitter at eye opening after equalization is seen to have reduced by more than 50 % and amplitude of eye opening is seen to have increased by more than 1500 mV as compared to the input. The data sampling is done synchronously.

The CTLE presented in [3] operating at 15 GHz and is implemented in 65 nm standard CMOS technology and consumes power of 13.2 mW for 1.1 V power supply. It offers a low input impedance and it is adaptive to different channel loss. The eye opening after equalization offers a 10ps jitter and 182 mV eye opening. CG CTLE detects the low current received signal as it has high sensitivity.

4. CONCLUSIONS

In the paper [1], it is said that "data amplitude histograms are obtained at various equalizing filter coefficient settings, and the one producing the histogram with the largest peak value is selected as the optimum coefficient.". It is noteworthy that the three different histograms providing three different amplitudes at one particular coefficient setting is not accurate enough to determine the amplitude of the incoming data at that particular sampling point. Information regarding amplitudes can be drawn from the voltage values of reference signal generated by DAC.

From the noise analysis of schematic presented in [2], it is seen that the output referred noise is greater than the input referred in the range of frequencies where gain boosting is provided. This implies the filter is boosting the noise levels as well.

It is seen that the output noise figure in [3] is reduced as compared to architecture proposed in [2]. But the amplitude of the eye opening obtained by architecture presented in [2] is seen much higher not only compared to its input amplitude, but also as compared to eye opening amplitude obtained in [3].

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