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ANALYSIS OF HYBRID FULL ADDERS USING LOGICAL EFFORT

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***Abstract*— Estimation of timing behavior is one of the critical issues in the advancement of very-large-scale integration circuits. The concept of logical effort provides a way to assess timing behavior. Hybrid structures are fast and consume less power when compared to conventional CMOS(C-CMOS) structure. Most popular circuits with the hybrid structure are XOR and XNOR gates. These are the core of full adders. In this paper new hybrid full adders (HFAs) are compared with C-CMOS in terms of speed and power consumption. This paper also provides the analysis of hybrid full adders in multistage networks. Circuit designs are implemented using 130nm technology in Mentor Graphics tool and simulation results of various hybrid full adders like transistor function full adder (TFA), transmission gate full adder (TGA), Hybrid pass transistor logic with static CMOS (HPSC), HFA-20T, HFA-17T, HFA-B-26T, HFA-NB-26T and HFA-22T are compared with C-CMOS.

***Keywords*— Hybrid CMOS, full adders, logical effort, XOR-XNOR gates, timing behavior.**

1. INTRODUCTION

Several logical styles can be used to design a full adder but structure with conventional pull-up and pull-down networks gives a good performance in terms of drive capabilities and full output swing. On the other hand, C-CMOS circuits cause more short circuit current and more dynamic current at switching time, which causes more power consumption in comparison with the hybrid logic ones. In general, there is less connection to the power supply and ground in hybrid structure circuits when compared with C-CMOS circuits. There is a decrease in the speed of C-CMOS due to the presence of large input capacitance because of the number of connections to the pMOS and nMOS transistors. The implementation of hybrid logical styles utilizes the characteristics of distinct logical styles to enhance the performance of the design. The most popular logic style is conventional CMOS (C-CMOS) which has pull-up and pull-down transistor networks. The pull-up network is based on series and parallel pMOS transistors, and a pull-down network is based on series and parallel nMOS transistors. The C-CMOS style full adder is the general CMOS three-input XOR and XNOR circuits. Despite many advantages which are reported for many hybrid full adders like an area–power–energy efficiency, noise-tolerant, and high speed, the main problem in their utilization is irregularity and complexity of their structure. The transistor function full adder (TFA), transmission gate full adder (TGA), New-HPSC as the most popular hybrid full adders with different input–output drive conditions are selected in comparison with C-CMOS full adder for running this new method. The XOR-XNOR gate is the major consumer of power in the FA cell and it can be reduced by optimum designing of the gates. Also, new FA circuits for various applications were proposed and these are employed with hybrid logic style, and designed by using the proposed XOR-XNOR circuits.

In this paper the circuits for hybrid full adders i.e., C-CMOS, TGA, TFA, and New-HPSC (Fig.1) and also the hybrid full adders using XOR- XNOR circuits such as HFA-20T, HFA-22, HFA-B-26, HFA-NB-26T, and HFA-22T (Fig.2). The delay problems in the investigated circuits are implemented with and without logical effort. All the investigated circuits are implemented with and without logical effort, the results are compared.

2. IMPLEMENTED CIRCUITS

A. Hybrid full adders

CMOS logic styles are used to implement the low-power adder cells and they can be divided into two major categories: The Complementary CMOS and the Pass-Transistor logic circuits. The conventional CMOS full adder is based on the regular CMOS structure. The advantage of conventional CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage with arbitrary transistor sizes. The TGA (Transmission Gate Full Adder) is based on the transmission gates theory, which consists of a pMOS and an nMOS transistors connected in parallel, being a special type of pass transistor. The semiconductor performs Full Adder (TFA) uses pull-up and pull-down methods to create the inverters. It additionally utilizes some transmission gates for the remainder of the logic getting economical implementations for XOR-XNOR gates. TFA includes a less complicates circuit-styles than the C-CMOS full adder as shown in Fig.1. (c). TFA consists of 26 transistors, whereas the C-CMOS full adder needs 28 transistors. TFA provides buffered outputs for each sum (s) and carry-out (Co). Its disadvantage is low speed and dynamical consumption. A hybrid pass-logic with static CMOS output drive, full adder (HPSC) is proposed to

feature a hybrid CMOS logic style, as shown in Fig.1. (d). In the HPSC circuit, XOR and XNOR functions are simultaneously generated by pass-logic module with only six transistors and propagated to the successive CMOS module to produce full-swing outputs. To overcome the weak signals caused by pass transistors the two complementary transistors form the feedback loop. By pulling the pMOS to the supply voltage or down through nMOS to the ground they restore non-full-swing output. Due to the need for restoring and driving both modules for sum and carry out, the pass-logic module eliminates the whole propagation speed of the full adder.

B. Hybrid full adders using XOR-XNOR gates

Fig.2. (a) shows the circuit of initial planned hybrid FA (HFA-20T) which is formed by two 2-to-1 MUX gates and therefore the XOR-XNOR gate. The circuit of HFA-20T has no high-power consumption NOT gates on the critical path and it consists of 20 transistors. The benefits of this structure are low power dissipation and very high speed. The only problem of HFA-20T is the reduction of the output driving capability once it's utilized in the chain structure applications like ripple carry adder. The downside exists within the circuits that use the transmission function theory in their implementation while no buffering output. A way to reduce the power consumption of the FA structures is to use an XOR-XNOR gate and a NOT gates to get the opposite XOR or XNOR signal. The planned hybrid FA cell (HFA-17T) shown in Fig.2. (d) is designed by using the XOR gate. This structure is formed by 17 transistors that have- three transistors less than the HFA-20T. The delay of HFA-17T is on the top of HFA-20T due to the addition of NOT gates on the critical path of the HFA-17T. Fig.2. (b) presents the third proposed hybrid FA using XOR-XNOR gates with buffers on the *Sum* and *C*out outputs (HFA-B-26T), and it's created with 26 transistors. Fig2. (c) presents another proposed hybrid FA with new buffers (HFA-NB-26T), where they are placed within the data inputs of 2-1-MUX gates rather than inserting the buffers within the outputs. If the input signals of *A* and *C* are produced by the buffer, then for all double input combos, the *Sum* and *C*out outputs don't seem to be driven by the inputs of the circuit. To do this work, three further NOT gates are enough, because there was already *A* signal and can be made the buffered *A* signal with an additional NOT gate. So, the HFA-NB-26T FA circuit is formed by 26 transistors. The delay is reduced when compared with the HFA-B-26T.HFA-NB-26T is less than that of HFA-B-26T due to existing of 2-1-MUX gate between the buffer and the output node which increases the resistance from output node to the sources VDD.

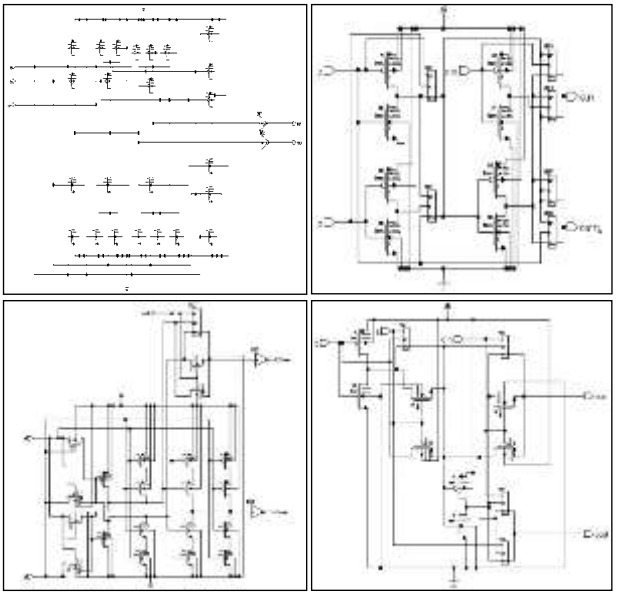

Fig.1. (a) C-CMOS (b) TGA (c) TFA (d) NEW-HPSC

The circuits of HFA-20T and HFA-17T have been designed so that the smaller number of transistors has been used. To produce the output *Sum* signal, the XOR, between the buffer and the output node which increases the resistance from the output node to the sources VDD and GND. The circuits of HFA-20T and HFA-17T have been designed so that the smaller number of transistors has been used. To produce the output *Sum* signal, the XOR, XNOR, and *C* signals are only used so no additional NOT gates needs to generate the *C* signal, whereas if the *C* signal is also used to produce the *Sum* output, then XOR and XNOR signals will not drive the *Sum* output through the TG multiplexer, but only they will be connected to the data select lines of 2-1-MUX. So, the capacitance of XOR and XNOR nodes become smaller and the delay of the circuit will be improved. The circuits of Fig.2. (e) have been created by applying the above idea to HFA-20T. The delay of the HFA-22T is less than the above circuits as shown in Fig.2.

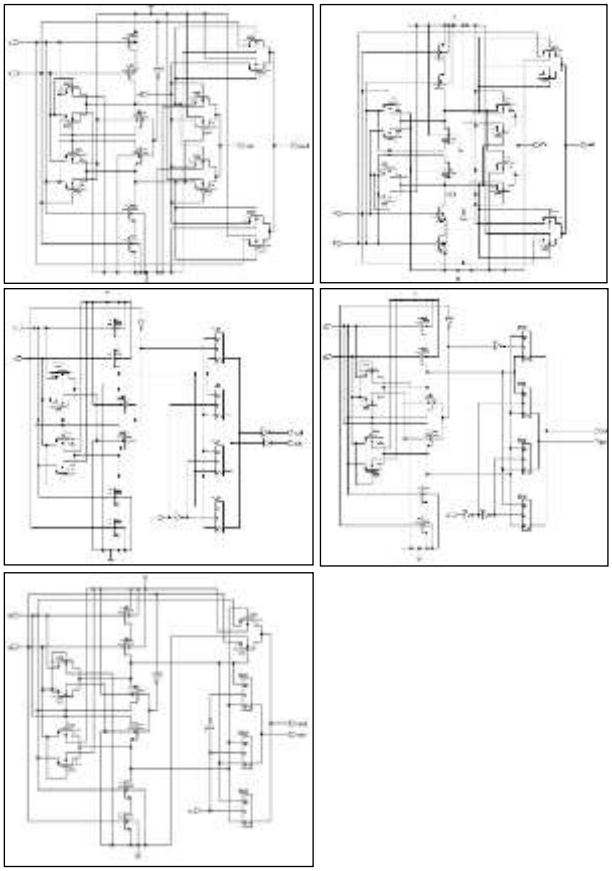

Fig.2. (a) HFA-20T (b) HFA-B-26T (c) HFA-NB-26T (d) HFA-17T (e) HFA-22T

C. Hybrid full adders in multistage

The adder, multiplier circuits are the fundamental building blocks of the arithmetic unit. By using the Low power full adder circuit, Ripple Carry Adder (RCA) or Parallel Adder is designed. The ripple carry adder is made by cascading full adders blocks in series. One full adder is accountable for the addition of two binary digits at any stage of the ripple carry. The carry-out of one stage is fed on the carry-in of consecutive stage. Schematic diagrams of Ripple carry Adder (RCA) is shown in Fig.3. (a).

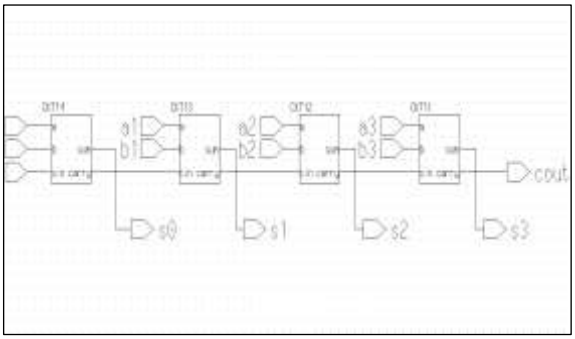

Fig.3. (a) Ripple carry adder for extraction of sum behavior

6:2 compressor is employed for the extraction of carry behavior in multistage full adders. The output of sum is given as input of next stage. The schematic of the 6:2 compressor is shown in Fig.3. (b).

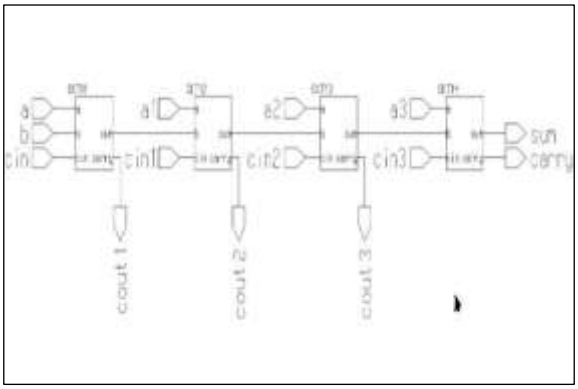

Fig.3. (b) 6:2 compressor for extraction of carry behavior

3. PROPOSED METHOD

To reduce the delay of hybrid full adders a brand-new technique known as the logical effort has been introduced. The method of logical effort is an easy way to minimize the delay in a logical circuit. By comparing the delay estimates of various logical structures, the fastest circuit is often selected or designed. The ratio of the input capacitance to the input capacitance of the inverter that delivers equal output current of a logic gate is called logical effort. To compute the logical effort of a gate, pick transistor sizes for it that creates it nearly as good at delivering output current as a regular inverter, and then tally up the input capacitance of every input. The logical effort of a gate tells what proportion worse it's at producing output current than is an inverter providing each of its inputs may contain only the identical input capacitance as the inverter. Initially, the hybrid full adders by applying logical effort are implemented and compared to the delay results. And also tried to use the logical effort to the multistage networks and also designed the layouts for basic gates (Inverter, NAND, and NOR) and delay is observed. The C-CMOS layout is newly designed in 130nm technology using a mentor graphics tool and simulated the results.

A. Calculating Logical Effort for basic gates

Inverter acts as a reference for the calculation of logical effort for other logic gates. For inverter, the input capacitance (Cin) is 3. The logical effort (g) of an inverter is 1 and it is shown in Fig.4. (a). The logical effort of logic gate NAND in the Fig.4. (b) can be calculated by extracting capacitances from the circuit schematic. The input capacitance of one input signal is the sum of the width of the pull-down transistor and the pull-up transistor, 2+2 = 4. The input capacitance of the inverter with identical output drive is Cin = 1+2 = 3.

According to the definition, the logical effort per input of the 2-input NAND gate is g = 4/3. The NOR gate in Fig.4. (c) is designed in a similar way. To get the identical pull-down drive as the inverter, pull-down transistors one unit wide suffice. To obtain the same pull-up drive, transistors four units wide are required. since two of them in series must be equivalent to one transistor two units wide within the inverter. Summing the input capacitance on one input, we discover that the NOR gate has logical effort, g = 5/3. Logical effort can be applied to logic gates with n number of inputs. The logical effort of gates with n number of inputs is shown in the table below.

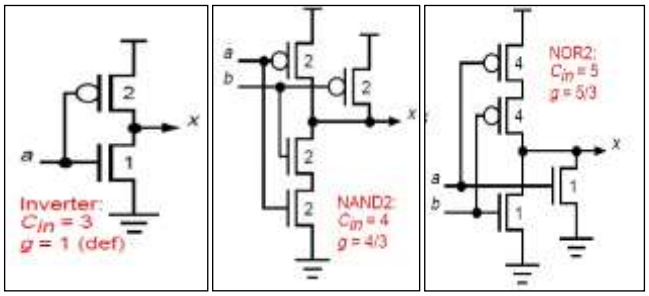

Fig.4. (a) Inverter (b) NAND (c) NOR

Table1: Logical effort of gates with n inputs

Logic Gate	No of Inputs			
	1	2	3	n
Inverter	1	-	-	-
NAND	-	4/3	5/3	(n+2)/3
NOR	-	5/3	7/3	(2n+1)/3

B. Logical effort for Transmission Gate

Many transmission gate circuits may be analyzed with the technique of logical effort by incorporating the transmission gate into the logic gate that drives it. Fig.5 shows an inverter driving a transmission gate, and then shows the same circuit redrawn. The pMOS and nMOS transistors in the transmission gate should be equal in width because both the transistors operate in parallel while driving the output. During arising output transition the strong nMOS transistor helps the weaker pMOS transistor. The model of two transistors in parallel as a perfect switch with resistance equal to that of an nMOS transistor for both rising and falling transitions.

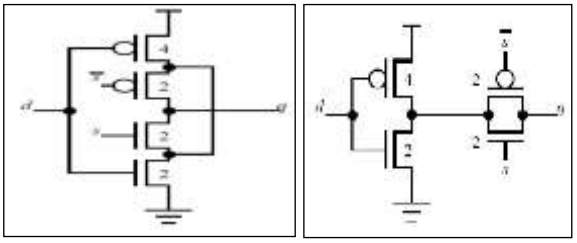

Fig.5 Inverter driving transmission gate and its equivalent circuit for logical effort calculation

4. SIMULATION RESULTS

A. Experimental setup

In this paper, circuit designs are implemented using 130nm technology in mentor graphics tool and simulation results of various hybrid full adders. Mentor graphics tool is a technology leader in electronic design automation (EDA), providing software and hardware design solutions that enable users to develop better electronic products faster and more cost-effectively. It helps to overcome the design challenges by facing the increasingly complex worlds of board and chip design.

B. Results of hybrid full adders

From Fig.6 a full adder adds binary numbers and accounts for values carried in likewise as out. A 1-bit full adder adds three 1-bit numbers these can be written as A, B, and Cin. A and B are the operands, and Cin could be a bit carried in from the previous less-significant stage. Schematic diagram of hybrid full adders in Fig.6. Table2 shows the delay comparisons of full adders with and without logical effort. Here, the C-CMOS logic style is high compared to the other full adders, and therefore the delay of adders has been reduced by using the concept of logical effort.

Table2: Comparison of delay of hybrid full adders with and without logical effort

CIRCUIT	DELAY	DELAY WITH LOGICAL EFFORT
C-CMOS	266.425 Ns	205.80pS
TFA	91.4pS	77.085pS
TGA	105.28pS	93.45pS
HPSC	94.63pS	52.31pS

Table3: Comparison of full adders using XOR-XNOR gates using logical effort

CIRCUIT	DELAY	DELAY WITH LOGICAL EFFORT
HFA-20T	52.3pS	40.19pS
HFA-17T	83.5pS	72.64pS
HFA-22T	36.52pS	32.9pS
HFA-B-26T	68.95pS	64.42pS
HFA-NB-26T	46.88pS	41.18pS

Table4: Comparison of delay for sum behavior in multistage

CIRCUIT	DELAY	DELAY WITH LOGICAL EFFORT
C-CMOS	725.5pS	603.6pS
TFA	210pS	190.4pS
TGA	195pS	194pS
HPSC	652pS	650pS

Table5: Comparison of delay for carry behavior in multistage

CIRCUIT	DELAY	DELAY WITH LOGICAL EFFORT
C-CMOS	71.75pS	52.02pS
TFA	7pS	6.4pS
TGA	6.5pS	5pS
HPSC	67.75pS	66pS

C. Layout

The C-CMOS layout is designed as shown in the Fig.6 and the resultant waveform is obtained as shown below Fig.7.

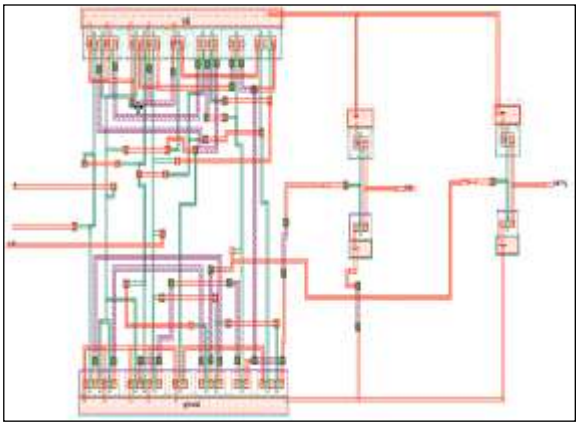

Fig.6 Layout of C-CMOS

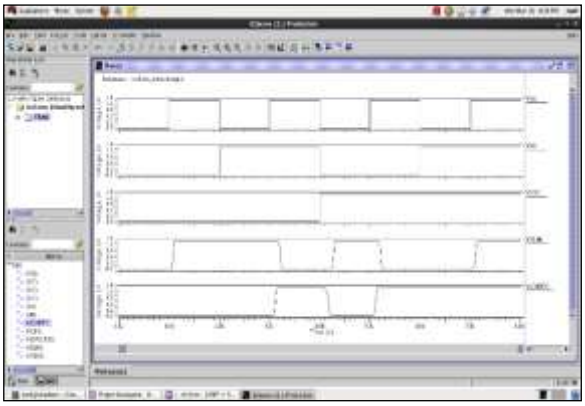

Fig.7 Post layout simulation waveforms of C-CMOS

5. CONCLUSION

Adders are the core of arithmetic circuits. As delay is one of the important problems faced with C-CMOS full adder, the concept of hybrid full adders came into existence. In this project, to reduce the delay of hybrid full adders, the concept of logical effort is used. All the hybrid full adders have been implemented by using 130nm technology in mentor graphics throughout the project. From the results obtained by using the concept of logical effort the delay of implemented full adders has been reduced and the power dissipation remained same. This concept has been extended and all the hybrid full adders are implemented in multistage. In multistage, the carry and sum behavior of hybrid full adders has been extracted. The delay of C-CMOS full adder has reduced by using logical effort in multistage and the delay of hybrid full adders with and without logical effort in multistage.

Layout of C-CMOS full adder is implemented and post layout simulations delay have been compared.

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