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# Design of QCA based One-Bit Memory Cell

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**Abstract -** *The Quantum Dot Cellular Automata is the Nanoscale technology which is used in designing circuits at very lesser size. The Quantum Dots are of high importance because it has less power dissipation, lesser delay, lesser area when compared to the CMOS technology. In this work the design and implementation of the Basic SRAM cell and Majority gate based SRAM cell has been discussed and also the comparison of both the architectures for performance parameters like area, delay and power values has been done. The QCA Designer-E tool has been used to design the circuits. The basic SRAM cell has been implemented using the basic circuits. The Majority gate-based SRAM cell has been implemented and its output operation has been verified. The results of the simulation revealed that the power and delay values of the Basic SRAM cell are 25.9 pW and 3/4th of the clock cycle respectively. The power and delay values of the Majority gate SRAM cell are 20.2 pW and 1/4th of the clock cycle respectively. The number of QCA cells used in the Basic SRAM cell is 52 and the Majority gate-based SRAM cell uses 63 cells. Therefore, the Majority-Gate based SRAM cell has lesser power and delay when compared to the Basic-SRAM cell. In the future, the Majority-gate based SRAM cell can be further optimised by reducing the number of cells and the Memory array can be designed using the single bit SRAM cell.*

***Key Words***: **QCA (Quantum Dot Cellular Automata), SRAM (Static Random-Access Memory), QCA Clocking, CMOS (Complementary Metal Oxide Semiconductor), Majority Gate, QCA Designer.**

## 1.INTRODUCTION

The QCA technology is in big trend because it uses Quantum dot cells. The QCA is growing very rapidly as it is in nano-scale technology. In CMOS technology there will be high static power dissipation and the dynamic power dissipation due to the transistor switching action [1]. This trade off of CMOS circuits can be overcome using QCA technology which has very less energy consumption and less power dissipation. The research suggests that the QCA has many features when compared to CMOS technology. The main features of the QCA technology are it has less power, less delay and consumes less area when compared to CMOS circuits. The QCA circuit has no voltage source. The electrons in the QCA cells position themselves to form logic 0 and logic 1. The transfer of logic value in the circuits will be based on the electron positions in the QCA cells. The QCA technology operates on the concept of clock. All the cells in the QCA operate in different phases of the clock. The clocking scheme of the QCA cell makes them hard to understand easily. But it has many advantages over other technology after designing the circuits.

The QCA based Memory cells have gained more importance in recent times because it has very less read and write energy consumption. The various researchers gave various QCA architectures for memory designs. SRAM is one of the memories used in computer architecture for cache design. So, the SRAM device optimization is at most important for high speed systems [2]. These SRAM circuits can also be simulated using QCA technology by drafting the layout of it in the QCA Designer tool [3].

The organization of this paper as follows. In Section 2 QCA cells operations, Clocking phases in a QCA and different basic elements needed to design a memory cell has been discussed. In Section 3 QCA based Basic SRAM cell has been designed. In Section 4 the Majority-Gate based SRAM has been discussed. In Section 5 the results and comparison of the both memory cell has been explained. Finally, Conclusion has been discussed in Section 6.

## 2. QCA OPERATION

Quantum Dot Cellular Automata is the emerging nanoscale technology which is widely used in various researches for optimizing the circuit at nanoscale level. The QCA has gained significant importance because its feature size is very less, or the area consumed by QCA based circuits are less when compared to other technologies [4]. The power consumption of the QCA cell is very low. The switching speed of QCA cells are very high and it has very much less delays. Hence, these QCA based circuits are gaining much more importance than the CMOS based circuits.

The QCA uses quantum effects which means the migration of the electrons inside the QCA cell makes them store the logic value [5]. The basic QCA cell is square in shape and it has four vacant positions for the electrons to occupy. Only two of the four vacant positions will be occupied by the electrons in the QCA cell. The electrons will only occupy the diagonals of the square. The electrons will not occupy the adjacent positions because there will be the electrostatic repulsion between the electrons. The position of occupancy of Quantum dot cells tells the logic value stored in the cell. If the electrons occupy the principal diagonal positions, then the QCA cell stores the logic '0'. If the electrons occupy the non-principal diagonal positions, then the QCA cell stores the

logic '1' value [6]. The representation of logic '0' and logic '1' storage is shown in Fig 1.

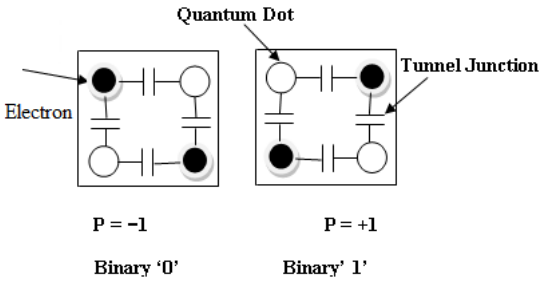


**Fig -1:** QCA Cell

## 2.1 Clocking in QCA

The QCA will work on clocks. There are four different clocks and there are four clock Zones in each clock [7]. The different Clocks are Clock 0, Clock 1, Clock 2 and Clock 3. The four clocking zones of QCA are:

1. Switch Phase
2. Hold Phase
3. Release Phase
4. Relax Phase

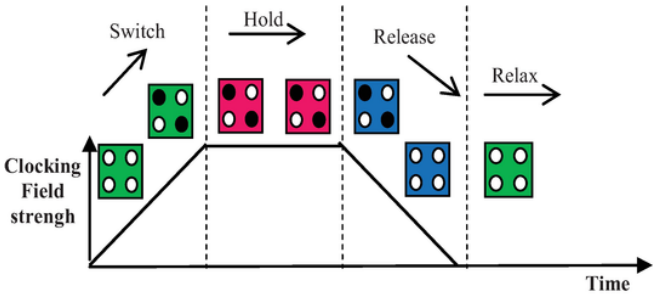


**Fig -2:** Clocking Operation in QCA

Switch Phase: During this phase, the QCA cells are initially unpolarised and at the start of the clock the QCA cell will be ready for the operation. The QCA cells will get polarised in the switch phase and the computation of the logic starts.

Hold Phase: In this phase, the logic value will be stored and helps in stabilizing the output. The final computation logic output will be available here in its stable state. Here the QCA cell acts as a Latch.

Release and Relax phase: In this phase, the QCA cell will become unpolarised and the output value will no longer act as a Latch. In this phase, the output goes to zero potential irrespective of input.

Hence, the QCA computation can only be observed in the switch phase and the hold phase. The QCA clocking scheme representing all the clocking zones is shown in the Fig 2.

## 2.2 Inverter Design

QCA inverter has a single input and output pin, where input is given at the one end of the pin and the inverted output taken at the other end. The layout of the inverter is shown in the Fig 3. where IN is the input signal and OUT is output signal.

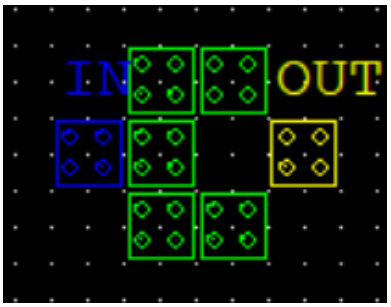


**Fig -3: Inverter Layout**

## 2.3 Majority Gate Design

Majority gate is used as a basic element in QCA circuit. This will use the majority logic to implement any logic functions without using any of the Boolean logical operations. Majority gate can also use to implement a AND or OR logic. A three input Majority gate can be used to implement a two input AND and OR function.

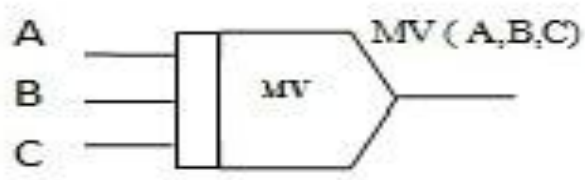


**Fig -4: Majority Gate Symbol**

Majority gate will produce the output as high when most of the inputs to the majority gate is '1'. Similarly, to get output as low the most of the inputs to the majority gate should be '0'. Symbol of the three input majority gate is shown in the Fig 4, where A, B and C are inputs and output is calculated by using this logical equation (AB+BC+CA).Layout of the three input majority gate is shown in Fig 5 where A, B and C are inputs and OUT is output signal.

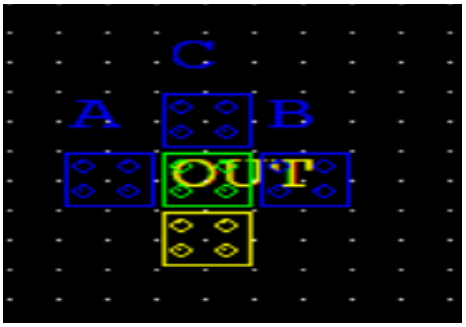


**Fig -5:** Majority Gate Layout

### 2.4 AND Gate Design

The AND gate can be implemented using the Majority gate concept [8]. In the majority gate one of its cells is polarized to low and is done by applying '-1'to that cell and output value can be changed to low or high depending upon the inputs value which is applied to its two input. In two input AND gate one of its cell is polarised to logical value '-1' and when both the inputs are '1' then it will produce the output as '1' or else it produces output as '0. Layout of the two-input AND gate is shown in Fig 6. where A and B are two inputs and OUT is output signal and remaining cell is polarised to low.

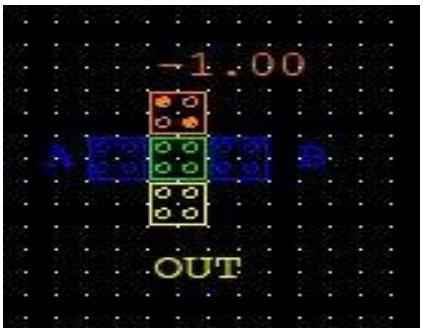


**Fig -6:** AND Gate Layout

### 2.5 OR Gate Design

The OR gate can be implemented using the Majority gate concept. In the majority gate one of its cells is polarized to High and is done by applying '1'to that cell and output value can be changed to low or high depending upon the inputs value which is applied to its two input. In two input OR gate one of its cell is polarised to logical value '1' and when both the inputs are '0' then it will produce the output as '0' or else it produces output as '1. Layout of the two-input OR gate is shown in Fig 7. where A and B are two inputs and OUT is output signal.

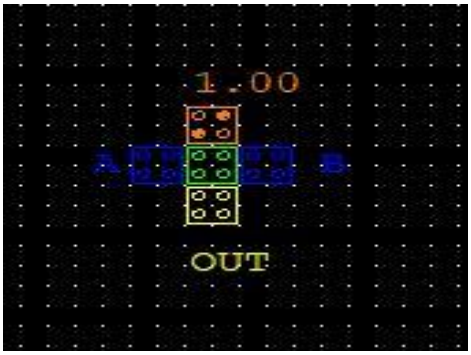


**Fig -7:** OR Gate Design

## 3. BASIC SRAM DESIGN USING QCA

The QCA based SRAM memory cell is composed of AND, OR and NOT gates [9]. This memory cell stores one-bit information in it. The circuit diagram of the single bit SRAM cell is shown in Fig 8. It has three inputs namely D, EN, R/W and one output.

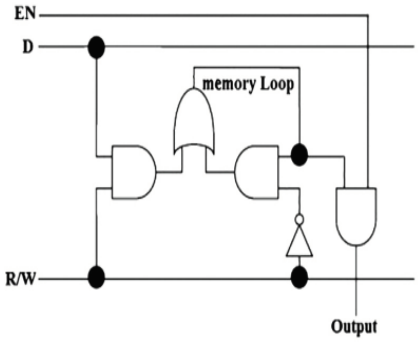


**Fig -8:** Basic SRAM Cell

The D input is the data input, EN is the enable input and R/W is the Read or Write pin. When R/W is logic '0', the memory cell is in Read mode and if R/W is logic'1' then the memory cell is in Write mode. The memory loop present in the circuit diagram basically acts as a hold circuitry.

When R/W is '1' the first AND gate output will be same as D input and if EN pin value is '1' then the output will take the value same as D input. This operation is known as Write operation. When R/W is'0' the output of the first AND gate is '0' and the Memory loop value will be in hold mode. During Read operation, the output is same as the Memory loop value when EN is '1'. The layout of the Basic SRAM designed using QCA technology is shown in Fig 9. The different basic gates like AND gate, OR gate and NOT gate are designed and integrated to get the full Memory cell layout. The clocking of all the cells has been designed in such a way that we get undistorted output.

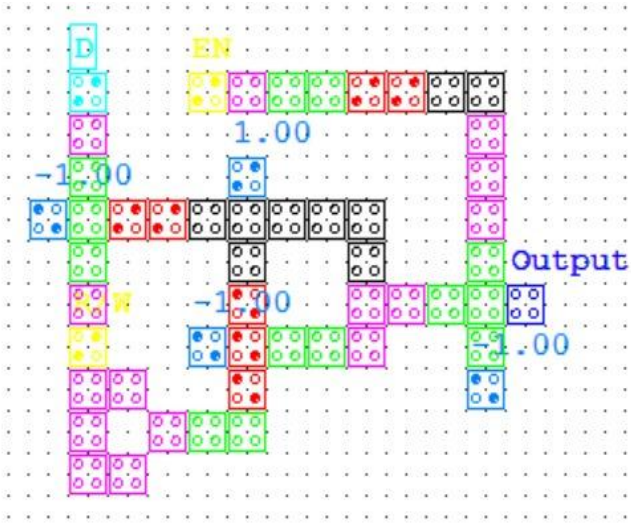


**Fig -9:** Layout of Basic SRAM using QCA

## 4. MAJORITY GATE BASED SRAM DESIGN USING QCA

The Majority gate is a customised gate which produces output equivalent to majority of input logic levels. If most of the inputs to the gate is '1', then the output of the majority is '1', else the output is 0. The majority gate-based memory cell has been designed and the logic diagram is shown in Fig 10.

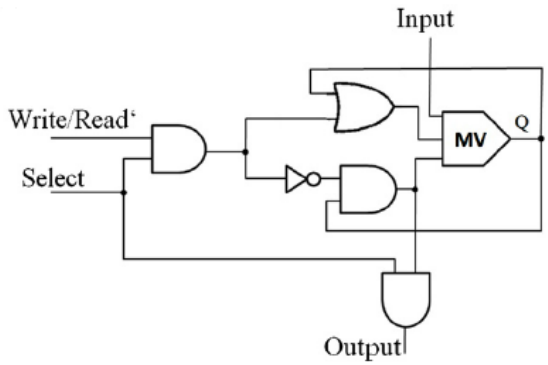


**Fig -10:** Majority Gate based SRAM Cell

The designed memory cell has basically write/read' signal, select signal, input signal and output signal. The select line can be used as a row select or column select when using in large array. The row or column decoder outputs can be connected to select line for selecting the cell. When Select='0', irrespective of other input lines the output goes to '0'. This states that the particular cell will not be selected for memory operation and the circuit will be in the hold state. When Select ='1' the write, read operation will be performed based on the Write/Read' input. When Write/Read' ='1' the Write operation will be performed. If the input ='1' then the Q='1' because most inputs to majority gate is '1' and similarly for write '0'. During read operation Write/Read' ='0' and the Q will be in hold mode and the previous data stored will be read.

The layout of the Majority gate-based SRAM designed using QCA technology is shown in Fig 11. The different basic gates like AND gate, OR gate, NOT gate, and Majority gate are designed and integrated to get the full Memory cell layout. The clocking of all the cells has been designed in such a way that we get undistorted output.

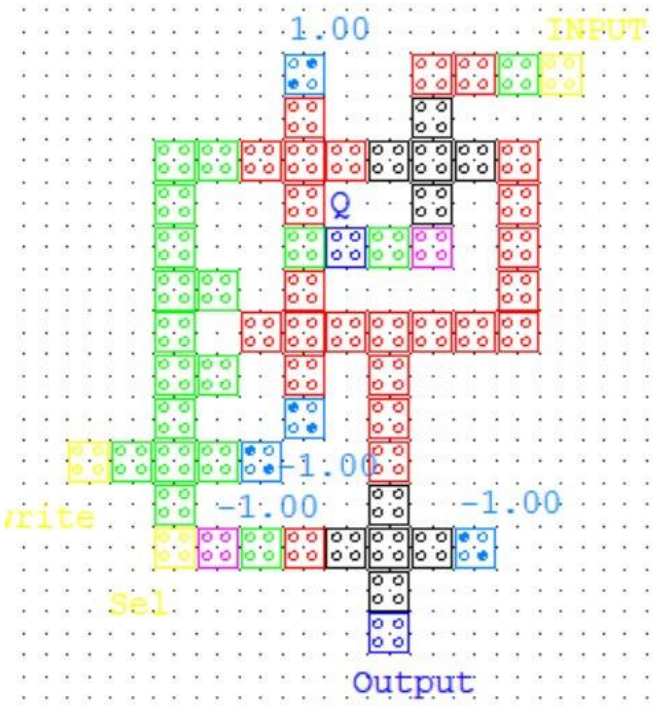


**Fig -11:** Layout of Majority Gate based SRAM Cell

## 5. SIMULATION RESULTS AND DISCUSSIONS

The Basic SRAM is implemented in QCA Designer-E tool and verified for the Read and Write operations.

**Write operation**: The SRAM is in Write operation mode, when the R/W pin is in logic '1'. In the output graph when EN='1', D='1' and R/W ='1' the output value will go to '1' and the output is arriving at the clock 3. Similarly, if D='0' then the data 0 will be written onto the output pin.

**Read operation**: When the R/W is logic '0' then the SRAM is in Read operation mode. When EN='1' and R/W='0' irrespective of data value, the output will be in hold mode indicating that the SRAM is in read operation. The output results are shown in Fig 12.

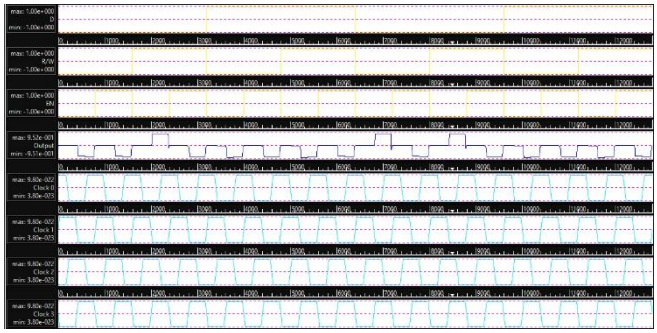

**Fig -12:** Results of Basic SRAM using QCA

The Majority gate has been incorporated in the design to implement the SRAM cell. The Majority gate-based SRAM cell has been designed in QCA Designer-E tool and its output Read and Write operations are verified.

**Write operation:** During Write operation the select line and Write/Read input is kept high. Based on the input value the output will go high or low. If the input is '1' most of the inputs to the Majority gate is '1' and hence the output will go high. Similarly, if the input is '0' the majority of the inputs to the Majority gate is low and hence the output will go low. The output is arriving at clock 1.

**Read operation:** During Read operation, the Write/Read input is kept low and Select line is kept high. Irrespective of the value of the input the output will follow the memory loop Q pin. The output operation is shown in Fig 13.

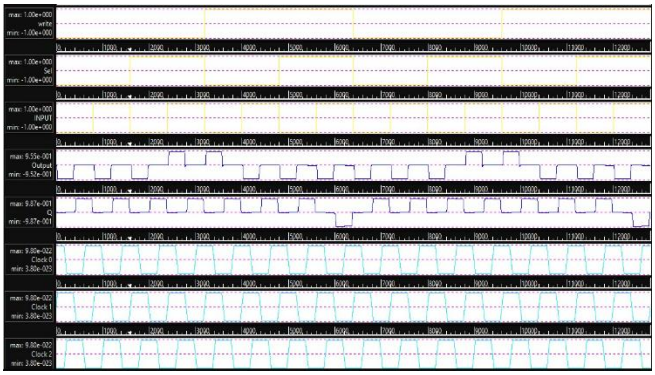

**Fig -13:** Results of Majority Gate based SRAM using QCA

The comparison of Basic SRAM and Majority-Gate based SRAM is shown in Table1. Power, Area, Number of cells, Delay and Energy parameters are used to measure the performance of the Basic and Majority Gate based SRAM. The Majority-Gate based SRAM uses less power and Energy when compared to basic SRAM. Majority-Gate Based SRAM takes lesser amount of time to change an output compare to the Basic-SRAM. The Majority-Gate based SRAM requires more cells than Basic SRAM, so it needs more Area.

**Table 1:** Comparison of Results

| Parameters | Basic-SRAM | Majority-Gate SRAM |
|---|---|---|
| Power | 25.9 pW | 20.2 pW |
| Area | 0.08 um^2 | 0.1 um^2 |
| No. of cells | 52 | 63 |
| Delay | ¾*Clock Period(T) | ¼*Clock Period(T) |
| Energy | 2.75e-2 eV | 2.7e-2 eV |

## 6. CONCLUSION

This paper gives the overview of QCA Designer tool and working and clocking of the QCA cells have been explained. The different circuits like inverter, majority gate, AND gate, OR gate and Memory cell has been designed. The memory cell is designed for Basic-SRAM and Majority-Gate based SRAM cell. Both the cells are designed using QCA Designer-E tool and the clocking phases are properly matched to analyse the results of the both Memory Cells. The working of the Basic SRAM cell and Majority-Gate based SRAM cell are analysed for both Read and Write operations. The results of both the architectures are compared based on different parameters like area, power, delay, energy. The Power and Delay of a Basic SRAM is 25.9pW and 3/4$^{th}$ of the clock cycle respectively and the Majority-Gate based SRAM cell has power and delay of 20.2pW and 1/4$^{th}$ of the clock cycle respectively. The results show that the Majority-Gate based SRAM circuit provides high efficiency in terms of Power, Energy and Latency when compared to the Basic SRAM cell.

## REFERENCES

[1] M. Kianpour and R. Sabbaghi-Nadooshan, "A Novel Quantum-Dot Cellular Automata X-bit × 32-bit SRAM", IEEE Transaction on VLSI, 2015.

[2] D. Gracia Nirmala Rani and M. Saranya, "Design Of Static Random Access Memory Using Qca Technology",IEEE Third International Conference on Devices, Circuits and Systems, 2016.

[3] Orestis Liolis and Vassilios A. Mardiris "Quantum-dot Cellular Automata RAM design using Crossbar Architecture",IEEE Proc. Circuits, Devices Systems, 2018.

[4] Moein Kianpour and Reza Sabbaghi-Nadooshan "A Novel Design And Simulation of 16 Bits RAM Implementation In Quantum-dot Cellular Automata (QCA)",IEEE Transactions on Computers, 2012.

[5] Mohammed Niamat and Sowmya Panuganti "QCA Design and Implementation of SRAM based FPGA Configurable Logic Block",IEEE Proceedings in Nanoscience and Nanotechnology, 2010.

[6] Vamsi Vankamamidi and Marco Ottavi "A Serial Memory by Quantum-Dot Cellular Automata (QCA)", IEEE Conference on nanotechnology, 2008.

[7] Konrad Walus, Timothy J. Dysart, "QCADesigner: A Rapid Design and Simulation Tool for Quantum-Dot Cellular

Automata" IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 3, NO. 1, 2011.

[8] I. Amlani, A. O. Orlov, G. Toth, G. H. Bernstein, C. S. Lent, and G. L. Snider, "Digital logic gate using quantum-dot cellular automata," Science, vol. 284, no. 5412, pp. 289–291, 2013.

[9] Walus, K., Vetteth, A., Jullien, G.A., and Dimitrov, "RAM design using quantum-dot cellular automata", Technical Proc. 2003Nanotechnology Conf. and Trade Show, Vol. 2, pp. 160–163, March 2003.

[10] M. Ottavi and S. Pontarelli "QCA memory with parallel read/serial write: design and analysis", IEEE Proc.-Circuits Devices System, 2010.

[11] C.S. Lent, P.D. Tougaw, W. Porod, G.H. Bernstein, "Quantum cellular automata", Nanotechnology, Vol. 4, No. 1, pp. 49–57, 2014.

[12] J. Huang, M. Momenzadeh, and F. Lombardi, "Analysis of missing and additional cell defects in sequential quantum-dot cellular automata," Integr., VLSI J., vol. 40, no. 4, pp. 503–515, 2007.

[13] W. Liu, S. Srivastava, L. Lu, M. O'Neill, and E. E. Swartzlander, "Are QCA cryptographic circuits resistant to power analysis attack?" IEEE Trans. Nanotechnol., vol. 11, no. 6, pp. 1239–1251, Nov. 2012.

[14] Blair, E.P., and Lent "Quantum-dot cellular automata: an architecture for molecular computing", Int. Conf. on Simulation of Semiconductor Processes and Devices SISPAD 2003, Vol. 2, pp. 14–18, Sept. 2013