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A NINE LEVEL INVERTER WITH REDUCED SWITCH COUNT

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Abstract - *In this modern world carbon foot prints are keep on increasing, inorder to reduce them the world is moving towards the renewable energy resources .The multilevel inverters can be effectively used for both stand alone and renewable energy resources that are connected to the grid . Researches are going on inorder to reduce the number of components used and increasing the level of output voltage we are getting from the multilevel inverters. In this paper lets us discuss about a new nine level inverter with reduced switch count.*

Key Words: *multilevel inverter, ladder based level adder, H – bridge, switches, output voltage.*

1. INTRODUCTION

Today all over the world the energy demand is keep on increasing due to that the depletion of fossil fuels is also increasing. In order to reduce the depletion of the fossil fuels the world is turning its face towards the conventional energy resource. In current scenario about 10% to 20% of the total load is being shared by wind and solar energy systems. But the output voltage we get from these renewable resources are highly fluctuating.

Solid state converters and intermediate storage elements are being used in order to regulate the fluctuating output voltage we are getting from this renewable resources. With multiple dc sources multilevel inverters will provide near sinusoidal output voltage. Hence in the field of solar photovoltaic power generation these multilevel inverters are getting attention.

DC voltage from multiple dc sources will be converted into AC voltage of desired magnitude by using the multi level inverter. The number of sources or capacitors available at the input side of the multilevel inverter decides the magnitude of the output AC voltage. The output voltage of the multilevel inverter will be a stepped sinusoidal waveform.

The number of steps in the stepped waveform is proportional to the number of sources being used to the input side. This makes the multilevel inverter more suitable for medium voltage, and high voltage applications. Output voltage THD, dv/dt stress and electromagnetic interference can be reduced and a nearly perfect sine wave can be obtained with higher amplitude of fundamental components by using higher number of levels in the inverters.

A number of topologies have been proposed so far and all these topologies come under the three topologies namely the Cascaded H – bridge converter (CHB), Flying capacitor (FC) based converter, Neutral point clamped (NPC) converter.

The Neutral point clamped converter has unequal voltage sharing because of the load power factor and it requires large number of clamping diodes. Thus the cost and complexity of the control circuit is increased. Hence it is less reliable.

In flying capacitor based converters the number of levels can be easily extended come factor such as large capacitor banks and pre - charging circuitry requirement and uneven voltage distribution makes it less attractive.

The cascaded H–bridge converters has simple expansion and less number of components as compared to neutral point clamped converter and flying capacitor based converters. But as the number of voltage level rises the number of switches and isolated dc sources also increases.

2. LITERATURE SURVE

The number of research works are going on in order to reduced the number of switches and gate driving circuits for a given number of DC sources.

Babaei E, Mohammad Farhadi K, Farshid Nazaty M, proposed "A Cascaded multilevel inverter using sub-multilevel cells" in the Journal of Electric Power Systems Research.

Saara L, Babaei E, proposed Optimum structures of proposed "A new cascaded multilevel invert with reduced number of components" in IEEE Transactions on Industrial Electronics.

Mohammad Reza J O, Masoumeh K, Sajad Najafi R, Gevork B.G, proposed "An innovative scheme of symmetric multilevel voltage source inverter with lower number of circuit devices" in IEEE transactions on Industrial Electronics.

P. Prem and R. Baranikumar, proposed "A new multilevel inverter topology with reduced switch count for domestic solar PV units". In this topology the number of components used will be much reduced the other topologies given above. Hence this topology for our nine level inverter with reduced switch count and with high switching frequency.

3 .TOPOLOGY USED

Let the figure 1 represents our proposed ladder type sub multilevel inverter. Our proposed topology consists of a H bridge and a ladder based level adder. Let S1,S2,...Sn be switches used in the ladder based level adder used along with the snubber resistance and B1,B2,B2 and B4 be the switches used in the H bridge. We have used MOSFET switches in the ladder circuit and in H bridge MOSFET switches along with anti-parallel diodes are used. In the given sub module any number of isolated DC sources can be added.

The number of isolated DC sources being used decides the rating of the switches. For n number of sources used the number of switches needed is given in equation no (1).

$$N_{switch} = n + 4 \quad (1)$$

Through a suitable driver circuit the switches can be controlled using various PWM scheme. The number of driver circuit is given by following expression,(2)

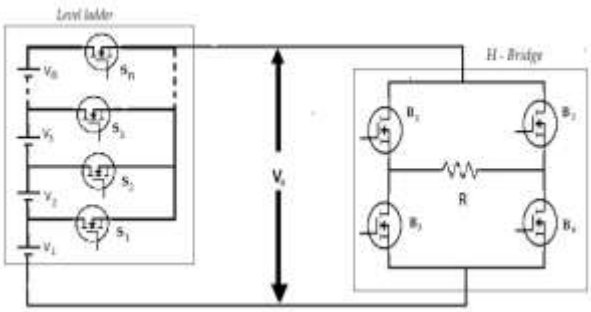

FIG.1.Basic circuit of topology used

$$N_{driver} = N_{switch} \quad (2)$$

For any number of levels the number of diodes in the circuit will be equal to it. The following equation (3) given the maximum output voltage of H- bridge.

$$V_{0max} = nv_{dc} \quad (3)$$

The necessary blocking voltage across the switching terminal and current through it decider the type of switch has to be used the following equcation (4) given the blocking voltage of the switches in the level ladder i.e.,S1,S2,S3... Sn.

$$V_{block} = vs1 = v_{s2} = v_{s3} = v_{s4} = V_{dc} \quad (4)$$

The following equation (5) given the blocking voltage across the switches B1,B2,B3&B4 in H- bridge,

$$V_{block} = v_{B1} = v_{B2} = v_{B3} = v_{B4} = nv_{dc} \quad (5)$$

The converters maximum blocking voltage is given by,

$$V_{blockmax} = nv_{dc} + 4 \text{ x } nv_{dc} \quad (6)$$

The following equation gives the number of levels,

$$N_{level} = 2n + 1 \quad (7)$$

4 .PROPOSED NINE LEVEL INVERTER

As discuss in the above topology we have used the ladder based level ladder in source side and H- bridge in the load side for nine level we have used four sources and eight switches, with four switches in level ladder and four switches in the H-bridge . The switches used are MOSFET's. In level ladder one switch and in H-bridge two switches will be closed during each conduction period. For gate triggering of the MOSFET's the PWM scheme is utilized. For multilevel inverters numerous PWM scheme are available.

Sinusoidal PWM scheme is used in our work. The below given figure represents our proposed nine level inverter circuit.

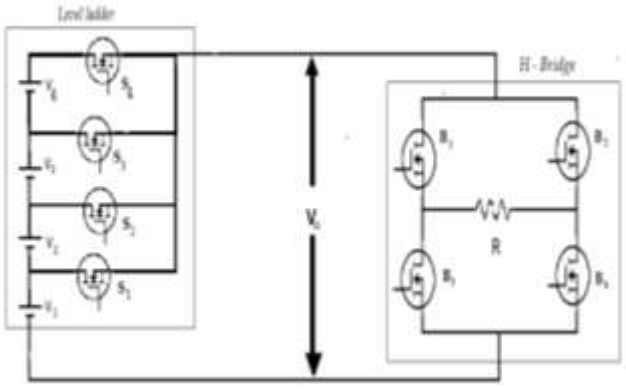

Fig.2 Nine level inverter circuit

In the above given figure S1,S2,S3&S4 are the switches used in the level ladder and B1,B2,B3&B4 are the switches used in the H-bridge. MOSFET is an unipolar device. Hence we get unipolar output voltage from the H-bridge.the DC voltage in the input side is increased by switching the switches S1,S2,S3,&S4. The output voltage waveform is given below.

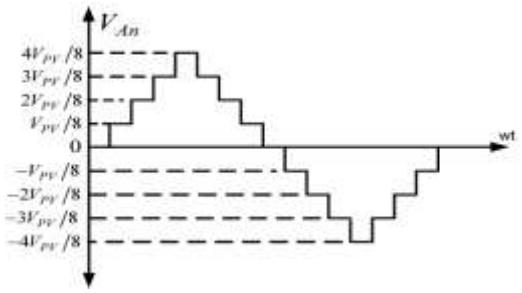

Fig.3 output voltage waveform

The table 1 gives the switching states for positive half cycle of the output waveform. The table 2 which is below gives the switching states for the negative half cycle of the output waveform.

According to the switching states of switches given in the table 1 & table 2 different modes are being operated. The switching circuit at each mode and for each mode of the switching the corresponding output waveform is given in the below given figures 4(a) to 4(h).

Table -1 : Switching states for positive half cycle of the proposed Nine level inverter

Output voltage	Switches in level ladder				Switches in H - Bridge			
V_O	S1	S2	S3	S4	B1	B2	B3	B4
0V	0	0	0	0	1	0	0	1
V1	1	0	0	0	1	0	0	1
V1+V2	0	1	0	0	1	0	0	1
V1+V2+ V3	0	0	1	0	1	0	0	1
V1+V2+ V3+V4	0	0	0	1	1	0	0	1
V1+V2+ V3+V4	0	0	0	1	1	0	0	1
V1+V2+ V3	0	0	1	0	1	0	0	1
V1+V2	0	1	0	0	1	0	0	1
V1	1	0	0	0	1	0	0	1
0V	0	0	0	0	1	0	0	1

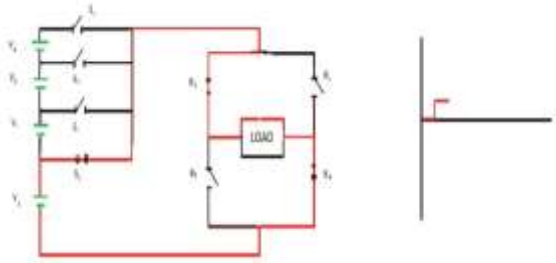

Fig.4(a)

Table -2 : Switching states for negative half cycle of the proposed nine level inverter

Output voltage	Switches in level ladder				Switches in H - Bridge			
V_O	S1	S2	S3	S4	B1	B2	B3	B4
0V	0	0	0	0	0	1	1	0
-V1	1	0	0	0	0	1	1`	0
-(V1+V2)	0	1	0	0	0	1	1	0
-(V1+V2+V3)	0	0	1	0	0	1	1	0
-(V1+V2+V3+V4)	0	0	0	1	0	1	1	0
-(V1+V2+V3+V4)	0	0	0	1	0	1	1	0
-(V1+V2+V3)	0	0	1	0	0	1	1	0
-(V1+V2)	0	1	0	0	0	1	1	0
V1	1	0	0	0	0	1	1	0
0V	0	0	0	0	0	1	1	0

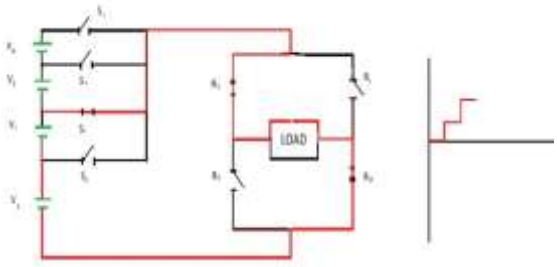

Fig.4(b)

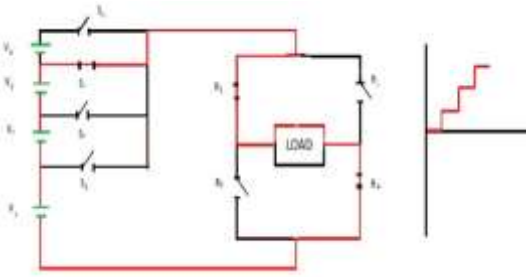

Fig.4(c)

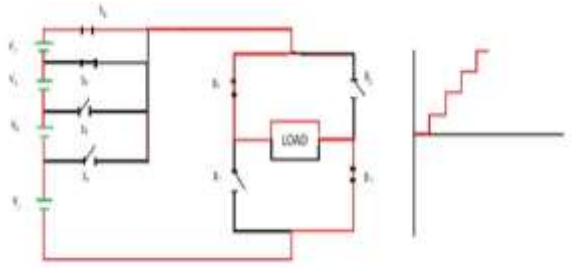

Fig.4(d)

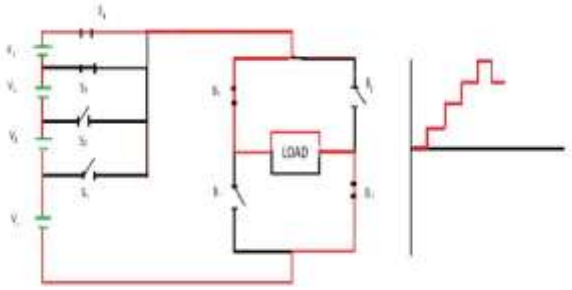

Fig.4(e)

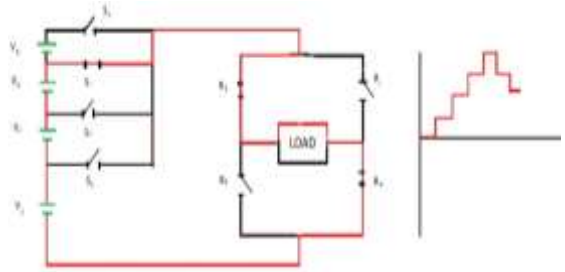

Fig.4(f)

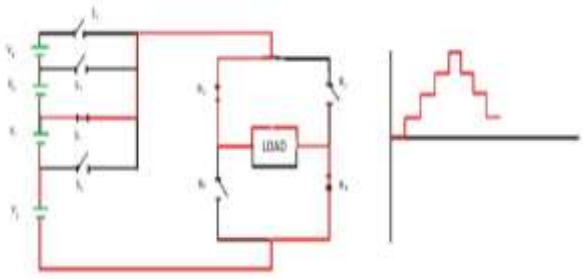

Fig.4(g)

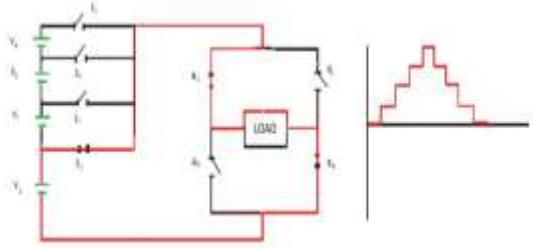

Fig.4(h)

The above given figures indicate the positive half cycle of the output voltage waveform. The below given figures 5(a) to 5(h) represents the negative half cycle of the output voltage waveform.

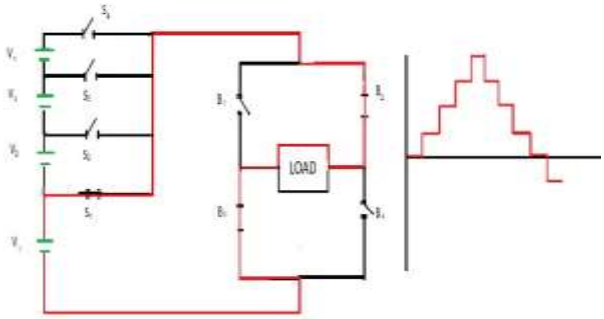

Fig.5(a)

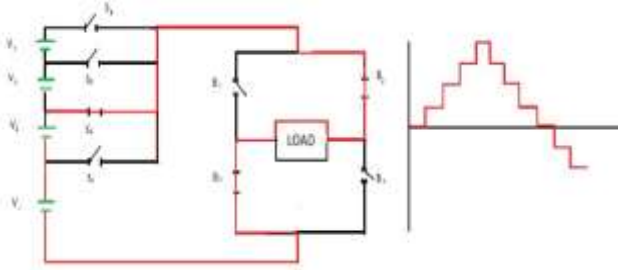

Fig.5(b)

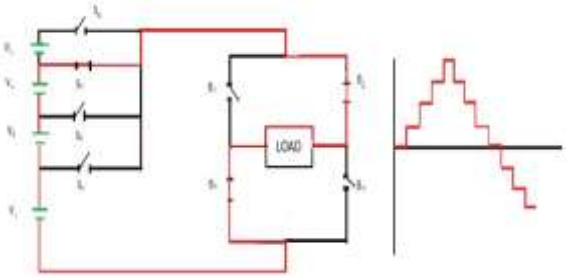

Fig.5(c)

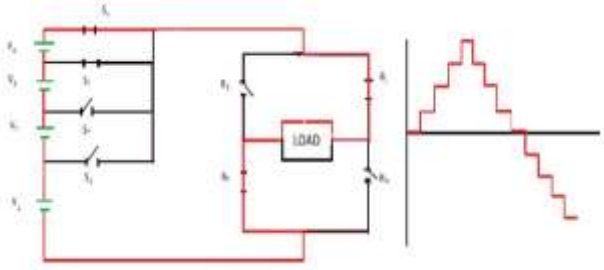

Fig.5(d)

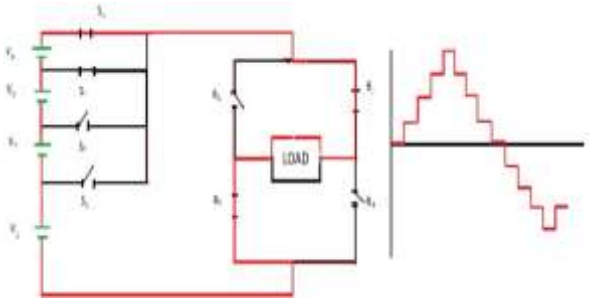

Fig.5(e)

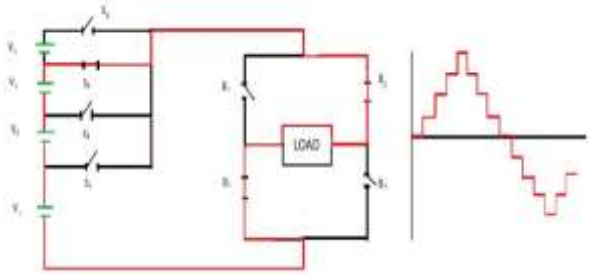

Fig.5(f)

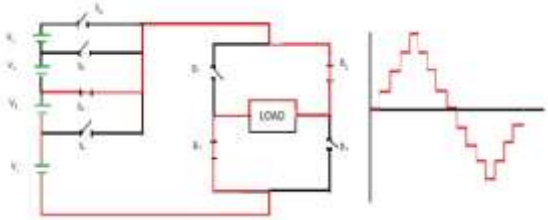

Fig.5(g)

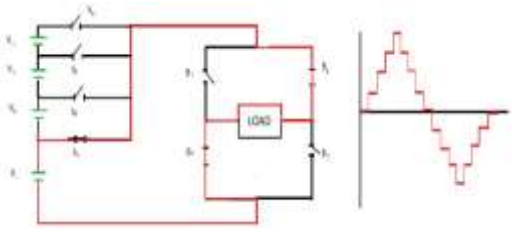

Fig.5(h)

5 .MATLAB SIMULATION

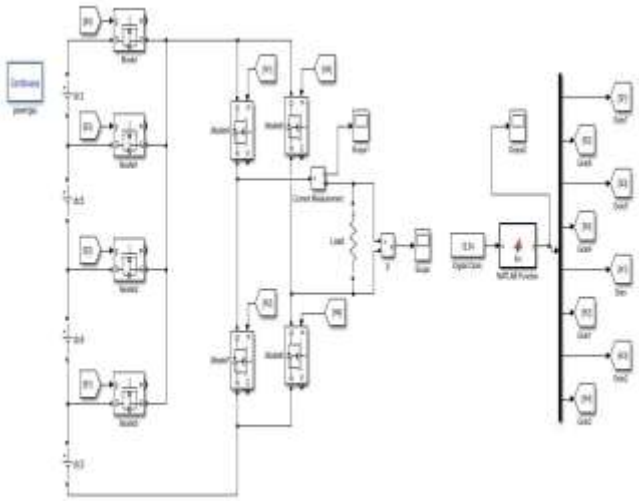

Fig.6

For stimulating our circuit in MATLAB software was used. Four isolated dc sources were used. In the input side each dc sources has 12V supply each. MOSFET switches were used for both level ladder circuit and H–Bridge circuit. R load with 5W capacity was used in the load side. The gate driving circuit was shown separately.

6. COMPARISON

The comparison table of the topology used with the reference topology is given below in table 3.

The number of switches (MOSFET 's), drivers, diodes used in the reference topologies and the topology which has been used in this work is compared in the figure 6(a) to 6(c) given below.

Table – 3 : Comparison table of topology used

Parameter	Reference 5	Reference 6	Reference 7	Conventional CHB	Topology used
Number of switches	[2 (n + 1)] + 4	4n + 2	$\frac{4n + 10}{3}$	4n	n + 4
Gate drivers	[2 (n + 1)] + 4	4n + 2	$\frac{4n + 10}{3}$	4n	n + 4
Number of diodes	[2 (n + 1)] + 4	4n + 2	$\frac{4n + 10}{3}$	4n	4
Maximum blocking voltage	[2 (n + 1)] + $4nV_{dc}$	$4 * [(3*5^{m-1} + 1)^n - 1]V_{dc}$	$(6n - 4)V_{dc}$	$n * 16\ nV_{dc}$	$nV_{dc} + 4nV_{dc}$

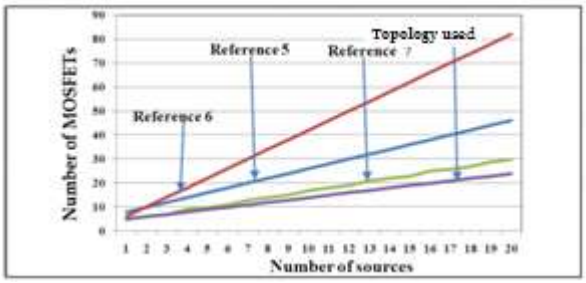

Fig.6(a)

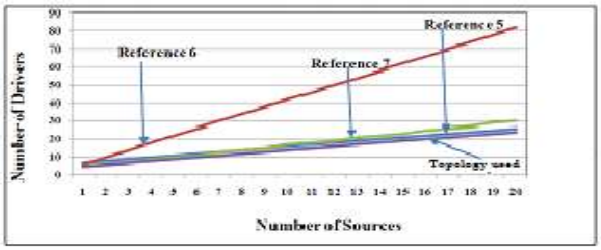

Fig.6(b)

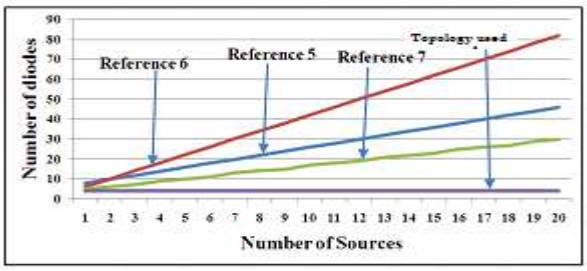

Fig.6(c)

From the above figures we come to know that the number of MOSFET 's, drivers, diodes used in this work is less than other topologies.

7 .HARDWARE MODEL

In this experiment four DC voltage sources with 12 V each is used. The block diagram of our hardware kit is shown in the below figure 7. The R load at the load side is with a 5W capacity. The switches used in the nine level inverter topology will be MOSFET switches. The isolator and driver used is 6N137 and the microcontroller used is DSPIC30F2010. The isolator is used for the purpose of protecting the microcontroller circuit from the high rating inverter and the driver is for driving the gates of the switches used. Our hardware kit is shown in the below figure 8.

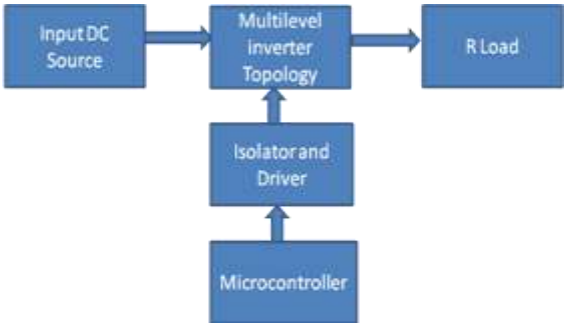

Fig.7

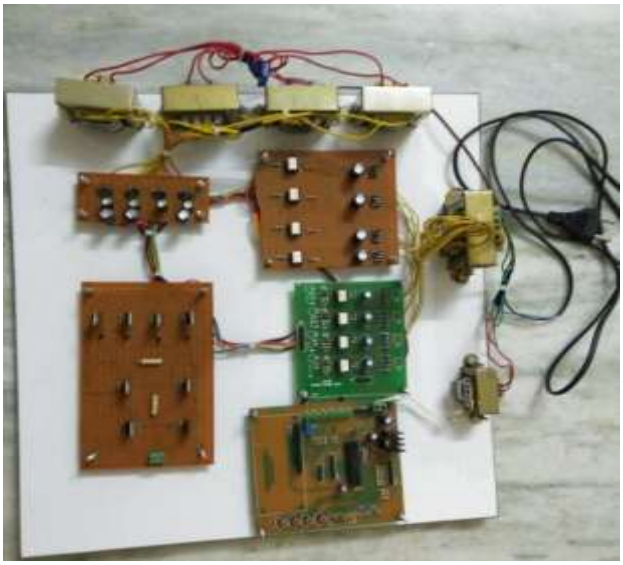

fig.8

8. CONCLUSION

From the comparisons made above this topology used in our work is the best one. MOSFET switches are used inorder to reduces the switching loss and to get a high switching frequency. In our work the number of components used is less with a efficient performance with reduced switching losses and with high switching frequency.

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