International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 07 Issue: 03 | Mar 2020 www.irjet.net p-ISSN: 2395-0072

Low Power Design for Fast Full Adder

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Abstract - In the era of digitalization, the unbending drive in the semiconductor industry for smaller, faster, cheaper integrated circuits has brought the industry to the 45nm technology. In this paper, the design for full adder which is highly optimized in terms of power consumption and area, featuring hybrid CMOS design style. To examine the performance of the proposed system, Tanner EDA simulations based on 45nm Complementary Metal-Oxide Semiconductor (CMOS) process technology used. This technology significantly reduces the power of the circuit during idle periods such that leakage power is no longer factor. This, in turn, helps extend battery life in battery-operated portable devices and has major advancement over previous. This paper explores the fast full adder circuit using XOR/XNOR gates and optimizes the PDP (Power Delay Product). By reducing area and power consumption, this circuit has high speed, optimized PDP. The proposed full adder has the good driving capability, power consumption and so on. The proposed architecture results are compared to area, power and delay of the existing.

Key Words: 45nm, Area, Full Adder, Hybrid-CMOS design style, PDP, XOR/XNOR.

1. INTRODUCTION

In the past decades, the major challenge for the VLSI designer was area, performance, cost and power consumption. In recent years, the trend for CMOS technology has improved and need to integrate more functions in a given silicon area. According to Moore's law, number of transistor in a chip doubles every two year at the same time the cost of the computer is halved. In detail, the speed and capability of computer increases for every two year and cost will reduced. As increase in no. of transistor in a chip, power will be increased and processing time of each transistor also increases. Thus, there will be loss in performance, to compensate for the performance loss use of either parallel or pipelined implementations [2]. A parallel implementation just doubles hardware thus pipelining is for low power solutions. Many full adder circuits were designed using various logic styles; each of them has its own merits and demerits. A full adder is a basic circuit that does all computations from counting to multiplication to filtering. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. These in turn, form the core of any system and thereby influence the overall performance of the entire system.

1.1 65nm to 45nm CMOS TECHNOLOGY

CMOS manufacturing for the design of processor to shrink in the size of the transistors, which means more can be fitted in the same space, with a number of implications. At the starting stage, today's processor design cannot be implemented as it is unfeasibly massive. Power consumption is also another issue. Smaller transistor consumes less power but practically there will more transistors than with a larger process technology. Due to low power consumption, transistor won't get hot thus at higher frequency the processor performs without burning or overloading the mother-board power supply [11]. The production cost will become cheaper to make. Thus, a 45nm processor takes up half the area of a 65nm one with the same design. It has 23% gate delay reduction compared to 65nm at the I_{off} and 10% lower $V_{DD.}$ It has less power leakage and greater power efficiency [12].

1.2 LOW POWER DESIGN

As VLSI technology advances, the complexity and speed of the circuit increases, resulting in high power dissipation. Power dissipation has become important constraint in semiconductor industry. The two major power dissipations are

1. Dynamic power dissipation, which is caused by two factors:

- Charging and discharging of the capacitor
- Short-circuit current, when both pMOS and nMOS are partially ON.

2. Static power dissipation, when the circuit remains in the idle state over a period of time, then there will leakage of current. These leakage current are caused by factors:

- Sub-threshold leakage
- Gate leakage
- Diode leakage
- Gate oxide tunneling

Increased usage of the battery-operated portable devices like, cellular phones, personal digital assistants (PDAs) and tablets demand VLSI and ULSI (Ultra-Large-Scale Integration) designs, with an improved power-delay characteristic [3]. For all the aforementioned devices, most or all of them switching activity may be stopped when it arrive in idle i.e., sleep mode. Consequently, in addition to

dynamic power, static power consumption limits the battery life while idle. Dynamic power dissipation dominates chip when active and it can written as

$$P_{dynamic}=\alpha CV_{DD}^2 f$$

Thus, by reducing the activity factor (α), switching capacitance (C), power-supply (V_{DD}) and operating frequency (f) dynamic power can be reduced. As mentioned before static power appears when the device in the idle state and it can be written as

$$P_{static}=I_{static}V_{DD}$$

Static power dissipation is the product of total leakage current (I_{static}) and the supply voltage (V_{DD}), thus by minimizing the I_{static} static power is reduced.

2. DESIGN APPORACH

Hybrid FAs are designed using more than one logic style and these adders are made of three modules, XOR/XNOR gate to generate S_o and 2 to 1 multiplexer to generate C_o[3] in fig-1. Optimum design of XOR/XNOR is required, as it consumes more power, there will be performance loss. Based on the output voltage level, circuits can be divided into full swing and non-full swing categories [1].

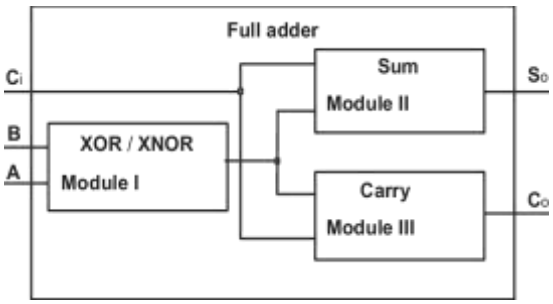

Fig-1: MODULE OF FULL ADDER

2.1 GATE LOGIC STYLE

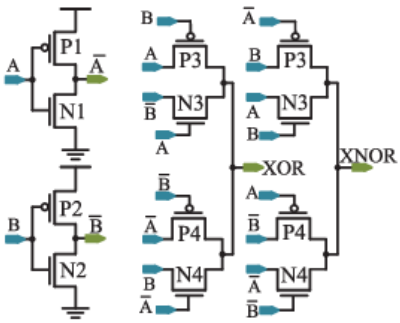

Fig-2: FULL SWING XOR/XNOR USING DPL

Fig-2, the full swing XOR/XNOR gate circuits [6] based on the Double Pass-transistor Logic (DPL) style. The model contains 8 transistors but the problem associated with this structure is that it has NOT gate on the critical path which consumes more power. The increasing size of the transistor in NOT gate will lower the critical path delay but it causes large output capacitance.

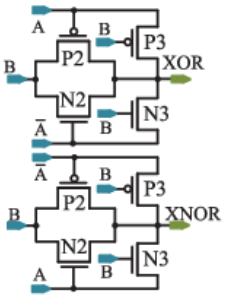

Fig-3: FULL SWING XOR/XNOR USING PASS-TRANSISTOR

Fig-3 [7] is based on the Pass-transistor logic style. This model consists of 6 transistors. The problem associated with this structure is that the XOR circuit has lower delay than the XNOR circuit since the critical path of the XNOR circuit has pMOS and NOT gate which is slower than nMOS transistor.

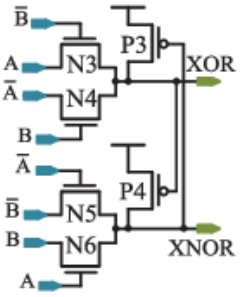

Fig-4: XOR/XNOR CIRCUIT USING CPL

Fig-4 [6], the circuit is based on Complementary Pass transistor Logic (CPL) this increase the speed and overcome the above drawback but problem associated with this is that is cross-coupled (feedback)which increase the delay of the circuit, another drawback is that existence of the two NOT gates on the circuit.

2.2 XOR/XNOR CIRCUITS

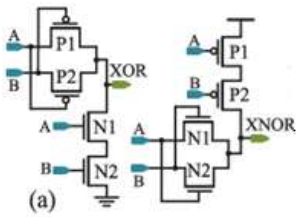

Fig-5(a): NON-FULL SWING XOR/XNOR

The non-full swing XOR/XNOR fig-5(a) is efficient in terms of the power and delay, but this structure has one drawback that at one logical value there is an output voltage drop problem. To overcome, they introduce the NOT gates. Thus

for all possible input combinations, the output of the structure is full swing in fig-5(b) [1].

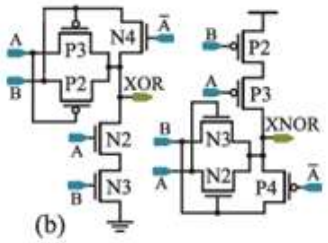

Fig-5(b): FULL SWING XOR/XNOR GATE

2.3 SIMULTANEOUS XOR/XNOR

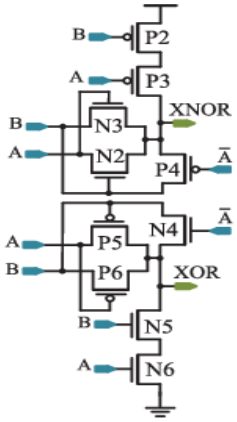

Fig-6: SIMULTANEOUS XOR/XNOR CIRCUIT

This structure made of 12 transistors shown in the fig-6. The model is obtained by combining two fig-5(b) [1].This model doesn't have any NOT gate on the critical path of the circuit and there will be very small output capacitance, thus the performance of the system is high i.e., processing speed is high and it consumes less power. Due to this, it has the good driving capability.

3. PROPOSED FULL ADDER

The proposed full adder is implemented based on the Swith hybrid logic style, in 45nm CMOS process technology. For the module I, implementation of 6 new hybrid full adders and for module 3,2to1 MUX been used to generate C_o. The most common implementation of MUX is using Transmission gates (TG) in fig-7.But the problem with that, it cannot provide a good driving capability to drive cascaded stages [3].Thus introducing output buffer which overcome that problem.

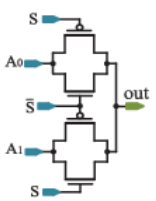

Fig-7: 2-1MUX USING TG LOGIC STYLE

The new hybrid full adder is designed with 20T, 17T, 26T, 22T, 19T in fig-8. The first hybrid FA is designed using 20T along with MUX.

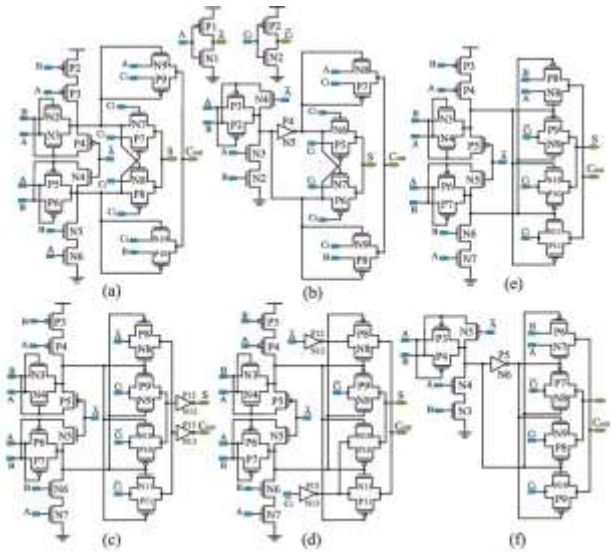

Fig-8: PROPOSED 6 NEW HYBRID FULL ADDER CIRCUITS

The structure doesn't have NOT gate on the critical path of the circuit, thus it has high speed and low power dissipation. But when this structure is used in cascaded stages, output driving capability will reduce. To, overcome the implementation of 17T in fig-8 (b). In this structure, NOT gate is used. The usage of NOT gate slightly improves the driving capability. The power consumption is almost the same as the 20T model as using NOT gate consumes power. For good driving capability, using a buffer is important. As VLSI technology improves its driving capability degrades due to the presence of the parasitic capacitance and resistance, the output buffers improve the situation [1]. Fig-8(c) HFA-26T designed with 26 transistors, MUX, buffer and NOT gate. The output nodes are driven by input which reduces the resistance but the delay and power consumption will be more when compared with the HFA-20T and HFA-17T. The new buffer is introduced at the input nodes. Fig-8(d) implements HFA-NB-26T buffer at the input that doesn't drive the output node. Using of NOT gate will improve the driving capability. The delay will be low when compared with the HFA-26T. The outputs are produced by Sum, C_o, and XOR/XNOR.

The output S_o can also be produced by $\bar{C}_o$. Goel et al. :[3]

$$\bar{C}_o = \bar{A} \text{ ?H?+ } \bar{C}_{in} \text{ ?H}$$

This will produce S_o output. Thus XOR/XNOR will not drive S_o, through data select lines of MUX it produces the output. The above mentioned is implemented in HFA-19T and HFA-22T in Fig-8(e) and 8(f). The capacitance of the circuit is

reduced. The power consumption and delay of the design is much smaller than HFA-20T and HFA-17T.The outputs of transistor are compared in the Table-1.

Table-1: SIMULATION RESULTS(POWER IN e-6W, DELAY IN μs, AREA IN mm, PDP IN J)

	65 NM				45 NM			
	POWER	**AREA**	**DELAY**	**PDP**	**POWER**	**AREA**	**DELAY**	**PDP**
17T	3.18	1.10	-0.12	**-0.38**	1.51	0.76	-0.01	**-0.02**
19T	4.25	1.23	-0.10	**-0.43**	2.29	0.85	-0.12	**-0.27**
20T	2.55	1.30	-0.10	**-0.26**	1.26	0.90	-0.14	**-0.17**
22T	3.87	1.43	-0.08	**-0.31**	2.00	0.99	-0.16	**-0.32**
26T	15.8	1.69	-0.03	**-0.61**	7.10	1.17	-0.11	**-0.78**

The energy delay product is another metrics in low-power design. The Table-2 shows the improvement of PDP and EDP of the 45nm hybrid full adder than 65nm.

Table-2: IMPROVED VALUE OF 45 nm PDP AND EDP

	PDP%	**EDP%**
HFA-17T	35.4	4.53
HFA-19T	15.9	1.91
HFA-20T	8.3	0.2
HFA-22T	1.2	2.19
HFA-26T	16.8	6.26

4. SIMULATION ENVIRONMENT

The circuits are simulated using TANNER EDA in the 45 nm CMOS process technology and were supplied with 1.0V.All circuits at the supply voltage of 1.5V in 65 nm CMOS process technology in TANNER EDA performed. Tanner tool used is for minimizing time in designing huge IC's, it is also used to eliminate the maqnfacture errors, there by reducing manufacturing costs. Due to this pros and also simplicity of usage and optimizing the IC design Tanner is used. The results are compared in the chart-1 to chart-4.

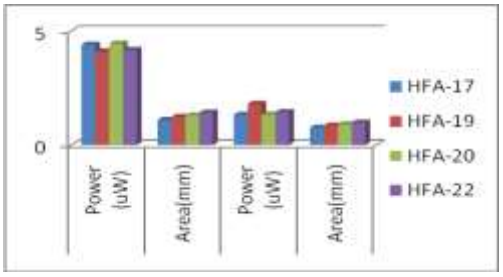

Chart-1: SIMULATION RESULTS OF FA's OF POWER, AREA 65 NM VS. 45 NM

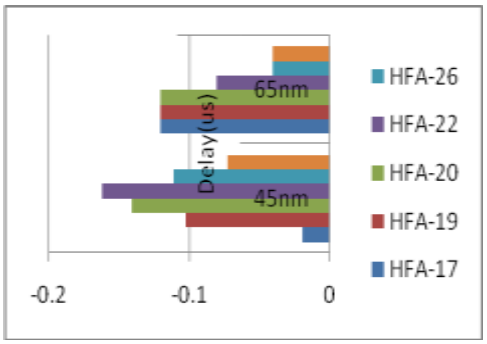

Chart-2: SIMULATION RESULTS OF FA's DELAYS 65 NM VS. 45 NM

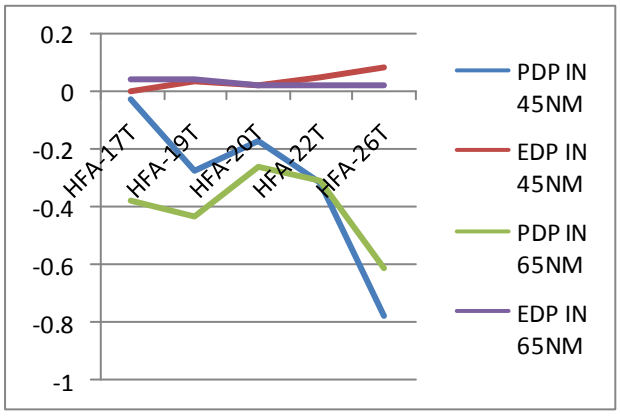

Chart-3: SIMULATION RESULT OF FA's VERSUS V_{DD} PDP, EDP OF 45 NM VS. 65 NM

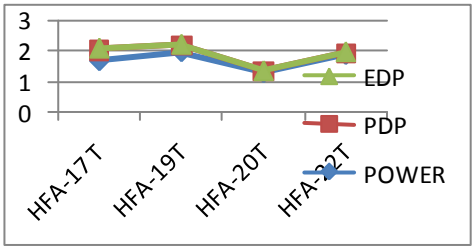

Chart-4: SIMULATION RESULT OF FA's FOR POWER, PDP AND EDP IMPROVEMENT OF 45 NM

4.1 SIMULATION RESULTS

Simulations are performed in the Tanner tool, are given in the fig-9 to fig-14.

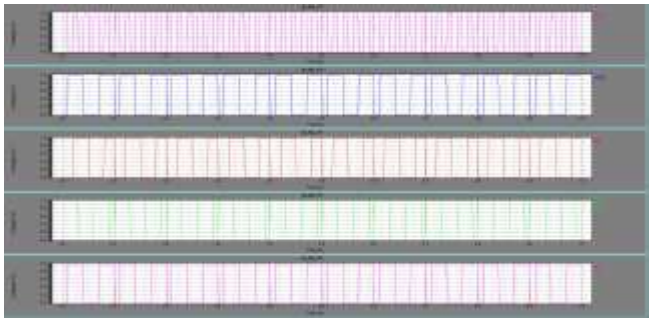

Fig-9: SIMULATION RESULT OF HFA-17T

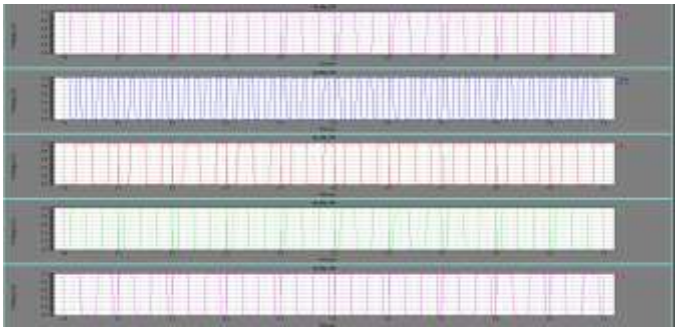

Fig-10: SIMULATION RESULT OF HFA-19T

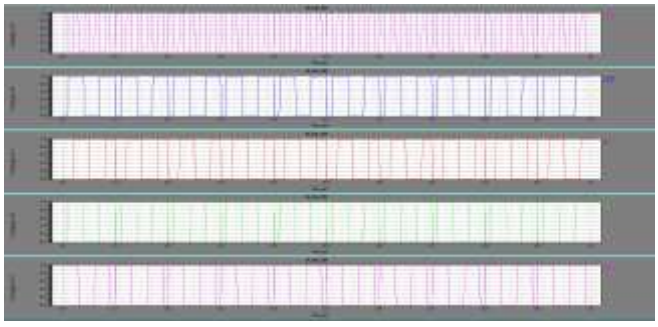

Fig-11: SIMULATION RESULT OF HFA-20T

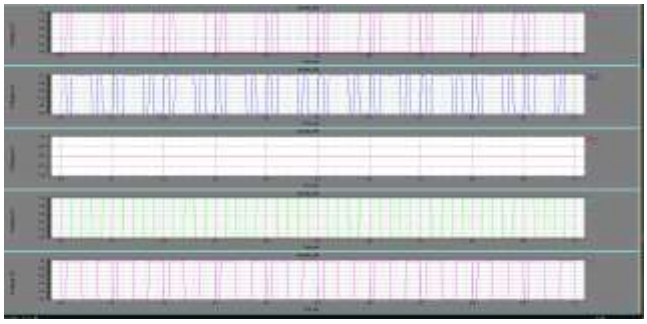

Fig-12: SIMULATION RESULT OF HFA-22T

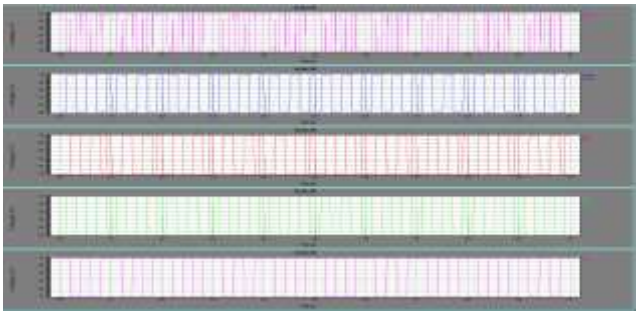

Fig-13: SIMULATION RESULT OF HFA-26T

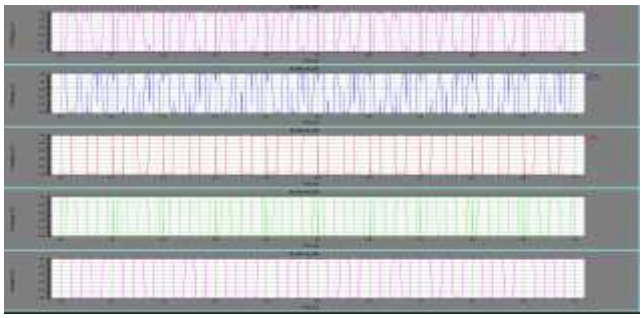

Fig-14: SIMULATION RESULT OF HFA-26BT

5. CONCLUSIONS

The XOR/XNOR circuits have been simulated in 45-nm CMOS process technology. Using hybrid-CMOS design style presented to have low PDP and area. The assessment of XOR/XNOR shows the main problem of this circuit, usage of two-high-power consumption NOT gates on the critical path of the circuit. The proposed circuit doesn't have above drawback. The proposed circuit has hybrid full adders can be used for many applications. The full adders have the good driving capability. Using hybrid-CMOS design style for the designs provide high performance in the circuit. From simulation results, the proposed 17T saves PDP and EDP up to 35.4% and 4.53% compared to the existing. The proposed HFA has superior speed and energy against previous designs.

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