# PREDICTING THE MAXIMUM COMPUTATIONAL POWER OF MICROPROCESSORS USING MULTIPLE REGRESSION 

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#### Abstract

This is the era of information with computers as a vital source. In one way or the other each and every one is linked to them. The building block of these computers is transistors which is being doubled every 18 months according to Moore's Law. Gordon Moore(Co founder of Intel) gave this law which states that computational power of Microprocessors doubles every year which is now being increased to 18 months since the size of transistors is being halved in that period of time. There had been a myth that the concept of Moore's law will be obsolete by this year i.e. 2020 but it's a false statement, the fact is that Moore's law had been slowing down but it will still work in the coming future. This paper represents the predict the maximum computational power of microprocessors by Multiple Regression to prove that the concept of Moore's law can still be implemented and after a particular point it will become constant like a straight line on a graph.


Key Words: Regression, Multiple Regression, Prediction, Moore's Law.

## I. INTRODUCTION

Regression is the effective technique which can be used for prediction of maximum computational power. According to Moore Law more the no. of transistors faster will be the speed of microprocessor. With this coming age of AI and IoT we need faster and powerful computers. Using Multiple Regression we will also be able to know whether we can implement these technologies using current transistor methods or we need new kind of computers such as quantum or optical computers.

Moore's Law is not exactly a law but an observation that the number of transistor in a dense integrated circuit doubles about every 2 years. The observation is named after Gordon Moore, the co-founder of fear child semiconductor and was the CEO of Intel, whose 1965 paper describes the doubling every year in the number of components per integrated circuit. Moore's Law is closely related to MOSFET scaling, as the rapid scaling and miniaturization metal-oxide-silicon feel - effect transistors is the key driving force behind Moore's Law.

At present time already the billions of transistors are embedded on a microprocessor chip. A transistor reduces, amplifies and directs an electrical signal using 3 leads, a source, a gate and a drain. ${ }^{[5]}$ When voltage is applied to the gate lead, an incoming current at the source lead will be allowed to pass through the drain lead. ${ }^{[5]}$ Take the voltage away from the gate lead and the current cannot pass through. When this does is produced a way to compute logical values 0 s and 1 s in computer terms. ${ }^{[5]}$ It's true that Moore's Law will end eventually. The reason behind this is electrical leakage. ${ }^{[5]}$ For years as transistors gets smaller they become more energy efficient but now they have gotten so small as small as 10 nm , that the channel that carries the electrical current through the transistors cannot always contain it. ${ }^{[5]}$ Because of this heat is generated which wear out the transistor more quickly making them more susceptible to leakage. ${ }^{[5]}$ Now heat generated by 1 transistor cannot be a problem but if billions of transistors generate this heat, it affects the whole microprocessor chip. ${ }^{[5]}$

The latest microprocessor chip is Ryzen 2 which was produced by AMD which uses the transistors of $7 \mathrm{~nm} .{ }^{[1]}$ Some experts are saying that this is the limit of scaling the transistors. However at Semicon West 2013 the annual Mecca for chip makers, applied materials has detailed the road beyond 14 nm , all the way down to 3 nm and possibly beyond. ${ }^{[2]}$ This can be done by moving from using current design i.e. Fin field effect transistor(FinFET) to Gate All Around Field Effect transistor (GAAFET).

In 2019, Samsung announced plans for the commercial production of a 3nm GAAFET process by 2021. Also using MBC FET we can go further down to $2 \mathrm{~nm}, 1 \mathrm{~nm}$ and possibly to $0.5 \mathrm{~nm} .{ }^{[3]}$. So based on this valid information sources we are going to predict the maximum computational power and minimum cost of microprocessor chips using multiple regression.
It is used when we want to predict the value of a variable based on the value of two or more other variables. The variable we want to predict is called the dependent variable (or sometimes, the outcome, target or criterion variable). The variables we are using to predict the value of the dependent variable are called the independent variables (or sometimes, the predictor, explanatory or regressor variables).

The representation of multiple Regressions will be like

$$
\begin{equation*}
\mathrm{Y}=\mathrm{m}_{1} \mathrm{x}_{1}+\mathrm{m}_{2} \mathrm{x}_{2}+\mathrm{m}_{3} \mathrm{X}_{3}+\mathrm{m}_{4} \mathrm{X}_{4}+\mathrm{C} / \mathrm{m}_{0} \tag{1}
\end{equation*}
$$

Multiple regression also allows you to determine the overall fit (variance explained) of the model and the relative contribution of each of the predictors to the total variance explained.

## II. DESIGN OF DATA SET

We used the data on microprocessors of Intel. Taking into account the no. of transistors, Process, clock cycles we will provide a formula to calculate approximate clock cycles (Computational Power).

Table 1: Data set representation considered from past to current

| year | model | No. Of <br> Transistors(million) | Process(nm) | Cores | Word <br> size(bit) | clock Cycle(GHz) |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| 1977 | 8085 | 0.0065 | 3000 | 1 | 8 | 0.003 |
| 1978 | 8086 | 0.029 | 3000 | 1 | 16 | 0.005 |
| 1982 | 80286 | 0.134 | 1500 | 1 | 16 | 0.006 |
| 1985 | 80386 | 0.275 | 1500 | 1 | 32 | 0.04 |
| 1993 | Pentium | 3.1 | 800 | 1 | 32 | 0.06 |
| 1995 | Pentium pro | 5.5 | 350 | 1 | 32 | 0.2 |
| 1997 | Pentium 2 | 7.5 | 350 | 1 | 32 | 0.3 |
| 1999 | Pentium 3 | 9.5 | 250 | 1 | 32 | 0.6 |
| 2000 | Pentium 4 | 42 | 180 | 1 | 64 | 2 |
| 2003 | Pentium M | 77 | 130 | 1 | 64 | 1.7 |
| 2005 | Pentium D | 115 | 90 | 2 | 64 | 3.2 |
| 2006 | core 2 | 291 | 45 | 4 | 64 | 2.6 |
| 2008 | corei7 | 730 | 32 | 6 | 64 | 3.2 |
| 2013 | Haswell | 1400 | 22 | 4 | 64 | 4.4 |

## III. EVALUATION OF EQUATION

Based on this data we performed Multiple Regression Taking Clock cycle as dependent Variable (Y), No of Transistors as first independent variable ( $\mathrm{X}_{1}$ ) and Process as second independent variable ( $\mathrm{x}_{2}$ ), Cores as third independent variable ( $\mathrm{x}_{3}$ ) and Word size as fourth independent variable ( $\mathrm{x}_{4}$ ).

Then we get the following Values.
Intercept and correlation coefficient corresponds $\mathrm{C} / \mathrm{m}_{0}=-1.526288$,

$$
\begin{aligned}
& \mathrm{m}_{1}=0.001556 \\
& \mathrm{~m}_{2}=.00023448 \\
& \mathrm{~m}_{2}=0.06527811 \\
& \mathrm{~m}_{4}=0.053378
\end{aligned}
$$

Interdependence between variables or whole data set in other words can be used to measure statistical relation or association of impactness between the variables can be analyzed using coefficient concept.

Clock Cycle $=001556^{*}$ No of transistors $+.00023448 *$ Process $+.06527811^{*}$ cores $+.053378^{*}$ word size

Using this equation we can find approximate clock cycle values for no. of transistors, process, cores word size. While performing regression we find that the regression line follows $93 \%$ of data .and the regression line can predict data more accurately as we approached final values, As shown in Table Below.

Table 2: Real and Estimated predictive values

| Clock Cycle (Actual -Y) | Predicted Y |
| :---: | :---: |
| 0.003 | -0.330528895 |
| 0.005 | 0.09653661 |
| 0.006 | -0.255020391 |
| 0.04 | 0.599260074 |
| 0.06 | 0.439521884 |
| 0.2 | 0.337742122 |
| 0.3 | 0.34085577 |
| 0.6 | 0.320521387 |
| 2 | 2.062826454 |
| 1.7 | 2.105591283 |
| 3.2 | 2.220649505 |
| 2.6 | 2.614655173 |
| 3.2 | 3.425608953 |
| 4.4 | 4.335780071 |

## IV. RESULTS AND DISCUSSION

In this section we present the result of calculated data using the multiple regressions on the values such as number of transistors $\left(\mathrm{x}_{1}\right)$, process $\left(\mathrm{x}_{2}\right)$, cores $\left(\mathrm{x}_{3}\right)$, word size( x 4 ) and clock cycle( y ). So these are the maximum clock cycles we get based on some Assumed Values.

Table 3: Future statistics Results of Predictive Statistics of Variables

|  | Assumed Values |  |  |  | Predicted <br> Values |
| :--- | :---: | :---: | :---: | :---: | :---: |
| S. <br> No | No of <br> transistors(million) | Process(nm) | Cores | Word size(bit) | Maximum <br> Clock Cycle |
| 1 | 2000 | 14 | 4 | 64 | 5.26578 |
| 2 | 3000 | 10 | 4 | 64 | 6.82086 |
| 3 | 6000 | 7 | 4 | 64 | 11.48817 |
| 4 | 8,500 | 5 | 4 | 64 | 15.37771 |
| 5 | 11000 | 3 | 4 | 64 | 19.26725 |

## V.CONCLUSION

Moore's Law will stop eventually as already stated but not in the coming decade based on the references. Using these references we had calculated the maximum computational power in the table 3 . This is the concept of prediction of microprocessors; these are approximate values not the exact values because we know these values could be altered due to different factors such as new technology implementation, economy, and new observation in these transistors.

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## BIOGRAPHIES



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