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Hardware of Nine Level MLI using Cascaded H-Bridge

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Abstract - *Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. This project presents the most important topologies like diode-clamped inverter*

(neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multilevel with separate dc sources. This project compares three different topologies of inverters (Diode-clamped inverter, flying capacitor clamped inverter and Cascaded H-bridge inverter). The switching pattern for inverters is explained as well. For each inverter, IGBTs and MOSFETs are used as switching devices to make the comparisons more accurate. The switches that are used for different inverters are the same for all of the inverters. If the THD is important, the 9-level inverters should be used, since it has a lower THD than the 5-level and the 7-level inverter. The 9-level multilevel inverters have the lowest THD when filters are not used. If the cost is important the two-level inverter should be used, since it has the lowest cost between all of the inverter topologies. The most important part is to decide which one is more important. This project is hardware model and simulation of 9-level MLI using Cascaded H-bridge inverter.)

***Key Words*: Diode-clamped inverter, flying capacitor clamped inverter and Cascaded H-bridge inverter, IGBTs and MOSFETs**

1. INTRODUCTION

A device that converts DC power into AC power at desired output voltage and frequency is called an Inverter. Phase controlled converters when operated in the inverter mode are called line commutated inverters. The power in the battery is in DC mode and the motor that drives the wheels usually uses AC power, therefore there should be a conversion from DC to AC by a power converter. The simplest topology that can be used for this conversion is the nine-level inverter that consists of sixteen switches. A multilevel inverter is a power electronic system which gives sinusoidal voltage output from several DC sources. These DC sources can be fuel cells, solar cells, ultra-capacitors, etc. Since many switches are put in series the switching angles are important in the multilevel inverters because all of the switches should be switched in such a way that the output voltage and current have low harmonic distortion. Multilevel inverters have three types. Diode clamped multilevel inverters, flying capacitor multilevel inverters and cascaded H-bridge multilevel inverter.

The THD will be decreased by increasing the number of levels. It is obvious that an output voltage with low THD is desirable, but increasing the number of levels needs more hardware, also the control will be more complicated. It is a trade-off between price, weight, complexity and a very good output voltage with lower THD.

1.1 Block Diagram:

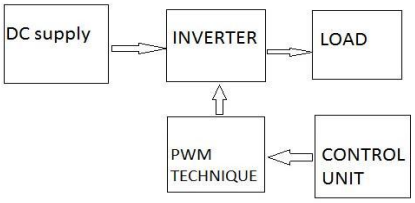

Fig 1.1 Block Diagram

The diagram shows the model of 9 level cascaded h bridge MLI. There are mainly 5 parts:

1. DC supply

2. Inverter circuit

3. PWM technique

4. Control unit

5. Load

The 48v Dc supply is given to the 9 level MLI. This 9-level MLI is convert 48V DC to the 48V peak Ac supply. The PWM technique use in the inverter. The MOSFET switches is control by micro-controller. The output of the inverter is given to the load. Inverters can be classified into single phase inverter and three phase inverters. Switching devices used in inverter uses PWM control signal for producing an AC output voltage. If input voltage remains constant the inverter called VSI and if current remains constant it is known as CSI. Three phase inverters are normally used for high power application.

2. TYPES OF MLI

3.1 Diode clamped MLI

The diode-clamped multilevel inverter employs clamping diodes and cascaded dc capacitors to produce ac voltage waveforms with multiple levels. The inverter can be generally configured as a three, or five-level or seven level topologies, often known as neutral-point clamped (NPC) inverter, has found wide application in high-power medium-voltage (MV)

drives. The main features of the NPC inverter include reduced dv/dt.

LIMITATIONS No. Of diodes are more use. In diode clamp inverter we have getting distortion due to the spikes. So, we have added a filter in this inverter to remove the distortion.

3.1.1 5 level diodes clamped MLI

In a 5-level diode clamped multilevel: n=5

Therefore:

Number of switches=2(n-1) =8

Number of diodes= (n-1) (n-2) =12

For example, to have Vdc/2 in the output, switches S1 to S4 should conduct at the same time. For each voltage level four switches should conduct. As it can be seen in switching table the maximum output voltage in the output is half of the DC source. It is a drawback of the diode clamped multilevel inverter. This problem can be solved by using a two Hardware of Nine level MLI using cascaded H-Bridge 6 times voltage source or cascading two diode clamped multilevel inverters.

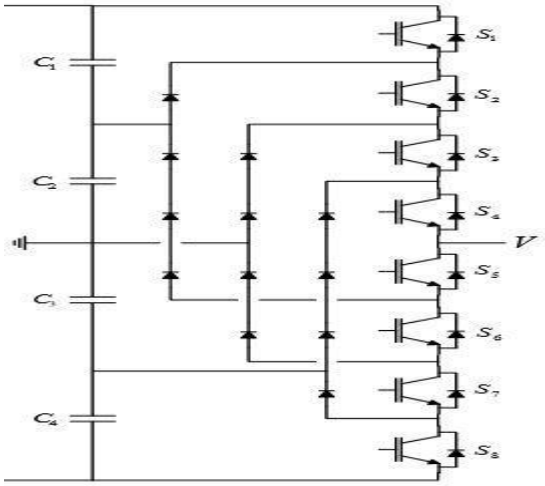

Figure 3.1: theoretical Circuit diagram (5 level)

V_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

Table 2: Switching table (5 level)

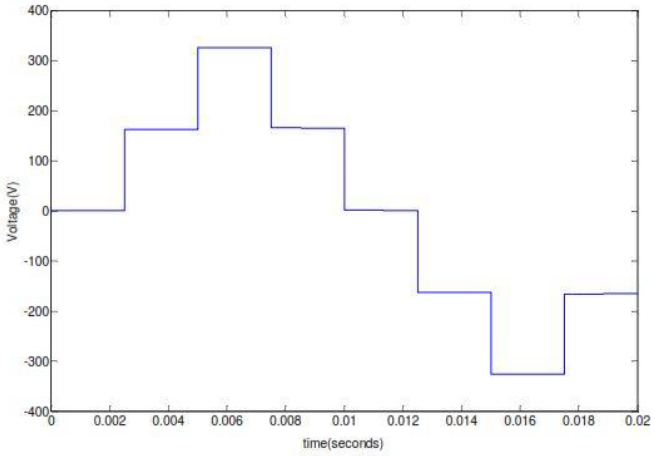

Fig 3.2 Theoretical output wave form (5 level)

3.2 flying capacitor MLI

- *This inverter consists three complementary switches (s1, s3), (s2, s4). Therefore, only three independent gate signals are required for each inverter.*
- *This inverter uses capacitors to limit the voltage of the power devices. The configuration of the flying capacitor multilevel inverter is like a diode clamped multilevel inverter except that capacitors are used to divide the input DC voltage. The voltage over each capacitor and each switch is Vdc.*

LIMITATIONS

• A large number of dc capacitors with separate pre-charge circuits.

• The inverter requires several banks of bulky dc capacitors.

3.2.1 5 level flying capacitor MLI

For a 5-level flying capacitor multilevel inverter: n=5

Therefore:

Number of switches=8

Number of capacitors= 10

- The switching states in this inverter are like in the diode clamped multilevel inverter. It means that for each output voltage level 4 switches should be on. Switching table shows the switching states for a 5-level flying capacitor clamped multilevel inverter.

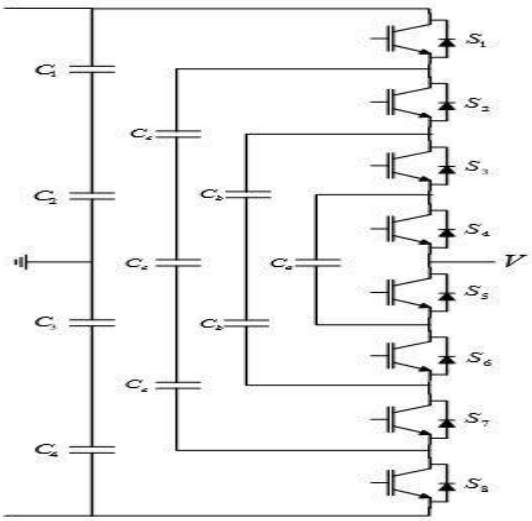

Fig 3.3 Theoretical Circuit diagram (5 level)

V_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-V_{dc}/4$	1	0	0	0	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

Table 3: Switching table (5 level)

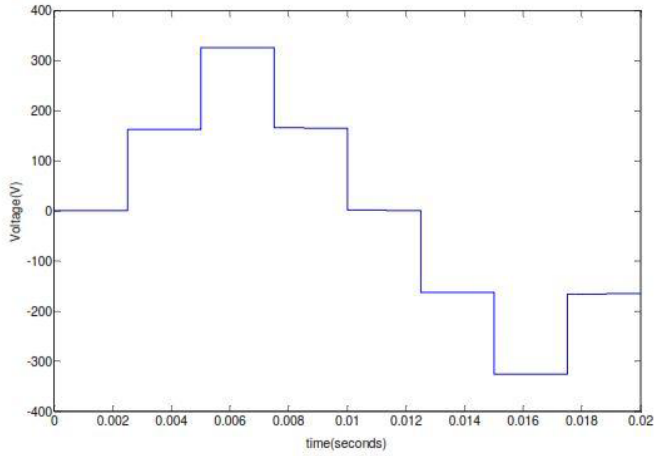

Fig 3.4 Theoretical wave form (5 level)

3.3 Cascaded H-bridge MLI

The most commonly efficient inverter is cascaded multilevel inverter. It provides higher output voltage and power levels. It is one of the methods used for drive application which meet the requirements such as high-power rating with reduced THD and switching losses. The Multilevel Inverter increases the number of levels in the output and reduces the number of input DC sources required. Mosfet is used as semiconductor switch for designing the inverter circuit. It has the high-power rating, less conduction loss and less switching loss.

3.3.1 5 level cascaded H-bridge MLI

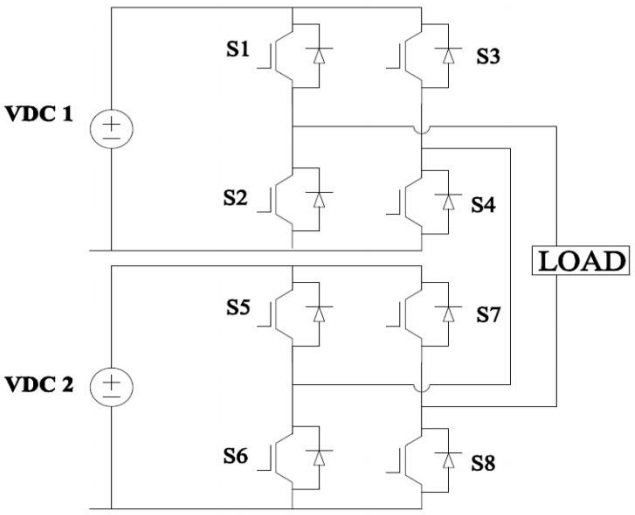

Fig 3.5 Theoretical Circuit diagram (5 level)

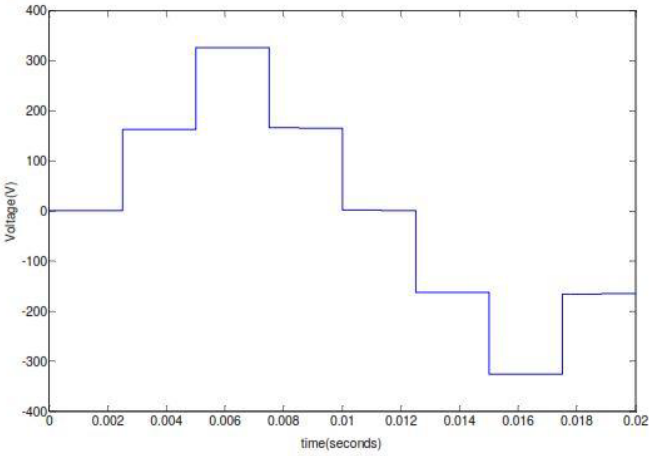

Fig 3.6 Theoretical wave form (5 level)

	S1	S2	S3	S4	S5	S6	S7	s8
2(Vdc)	1	0	0	1	1	0	0	1
Vdc	1	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
-Vdc	0	1	1	0	0	1	0	1
-2(Vdc)	0	1	1	0	0	1	1	0

Table 4: Switching table (5 level)

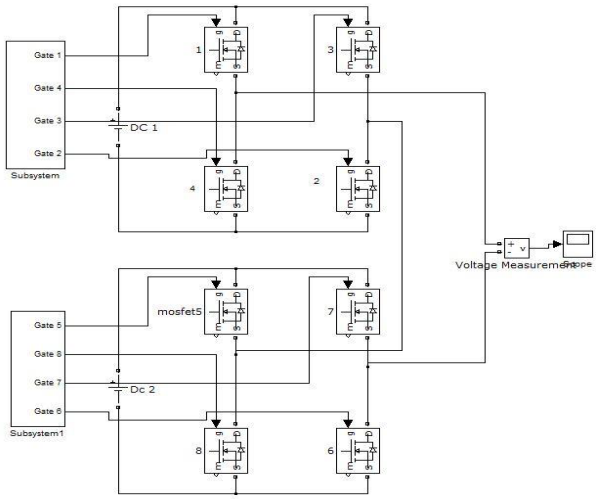

Fig 3.7 Practically circuit diagram (5 level)

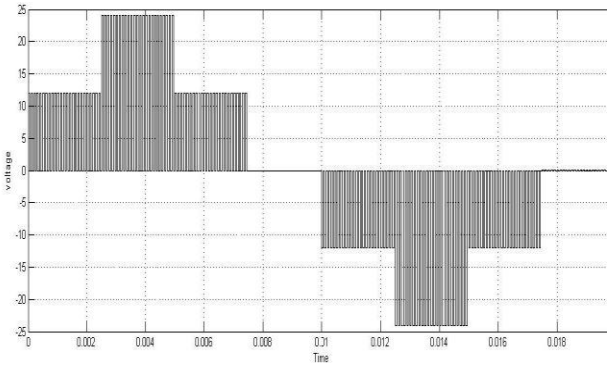

Fig 3.8 Practically Output waveform (5 level)

3.3.2 9 LEVEL CASCADED H-BRIDGE MLI

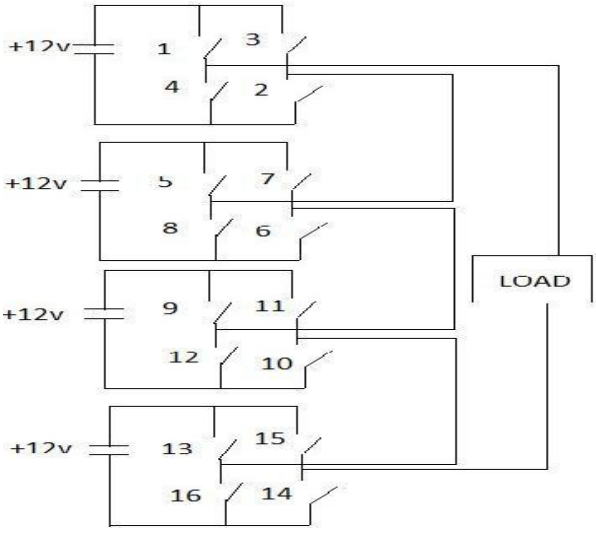

Fig 3.9 Theoretical circuit diagram (9 level)

OUTPUT(V) / SWITCHES	48V	36V	24V	12V	0V	-12V	-24V	-36V	-48V
S1	1	1	1	1	0	0	0	0	0
S2	1	1	1	1	1	0	0	0	0
S3	0	0	0	0	0	1	1	1	1
S4	0	0	0	0	1	1	1	1	1
S5	1	1	1	0	0	1	0	0	0
S6	1	1	1	1	1	0	0	0	0
S7	0	0	0	0	0	1	1	1	1
S8	0	0	0	1	1	0	1	1	1
S9	1	1	0	0	0	1	1	0	0
S10	1	1	1	1	1	0	0	0	0
S11	0	0	0	0	0	1	1	1	1
S12	0	0	1	1	1	0	0	1	1
S13	1	0	0	0	0	1	1	1	0
S14	1	1	1	1	1	0	0	0	0
S15	0	0	0	0	0	1	1	1	1
S16	0	1	1	1	1	0	0	0	1

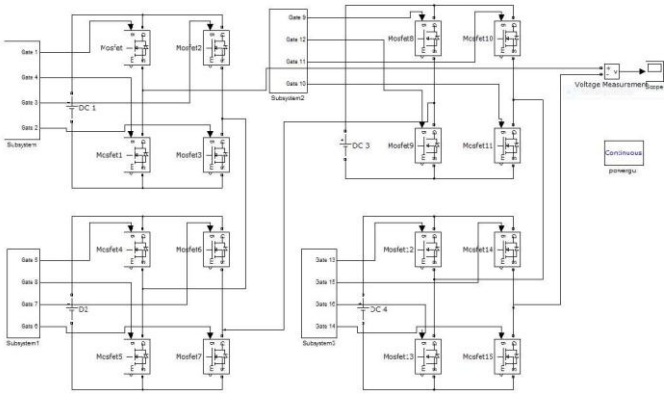

Fig 3.10 Practically circuit diagram (9 level)

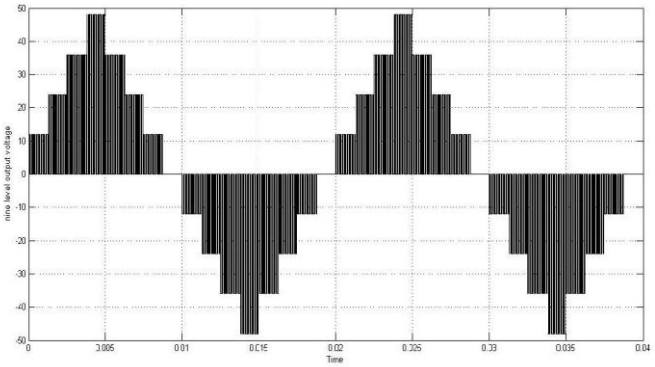

Fig 3.11 Practically Output waveform (9 level)

CHAPTER 4: HARDWARE COMPONENTS

1) MOSFET (IRFZ44N)

2) DC voltage source

3) Voltage regulator (IC 7812)

4) Microcontroller AT89C52

5) Diode (1N4007)

6) Diode (1N4148)

7) Opto-coupler

8) Power supply circuit for controller

9) Ac to 12V dc converter

10) MOSFET driver circuit

11)Misfit connection diagram

Chapter 5: CALCULATION OF MACHINE CYCLE

- *Crystal frequency Fc = 12MHz*
- *Machine cycle frequency Fm = Fc/12 = 1MHz*
- *Tm = 1/Fm = 1/1 M = 1micro second*
- *1 micro second = 1 Machine cycle*
- *(1111) micro second = (1111)10 = (0457)16*
- *FFFF – 0457 = (FBA8)16*
- *FB = TL0 & A8 = TH0*

LEVEL	8(P0.7)	7(P0.6)	6(P0.5)	5(P0.4)	4(P0.3)	3(P0.2)	2(P0.1)	1(P0.0)	CODE
1	0	1	0	1	1	1	0	0	5C
2	1	1	0	0	1	1	0	0	CC
3	1	1	0	0	1	1	0	0	CC
4	1	1	0	0	1	1	0	0	CC
3	1	1	0	0	1	1	0	0	CC
2	1	1	0	0	1	1	0	0	CC
1	0	1	0	1	1	1	0	0	5C
0	0	1	0	1	0	1	0	1	55
-1	0	1	0	1	0	0	1	1	53
-2	0	0	1	1	0	0	1	1	33
-3	0	0	1	1	0	0	1	1	33
-4	0	0	1	1	0	0	1	1	33
-3	0	0	1	1	0	0	1	1	33
-2	0	0	1	1	0	0	1	1	33
-1	0	1	0	1	0	0	1	1	53
0	0	1	0	1	0	1	0	1	55

Table 7: Timer coding for different levels

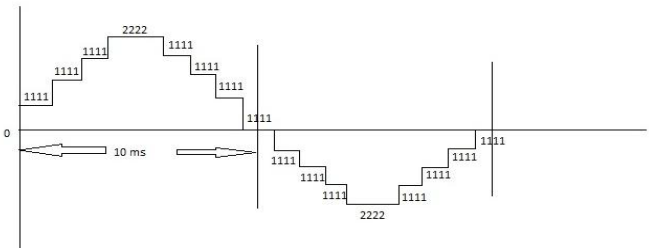

Fig 5.5: Delay for each level

LEVEL	16(P3.7)	15(P3.6)	14(P3.5)	13(P3.4)	12(P3.3)	11(P3.2)	10(P3.1)	9(P3.0)	CODE
1	0	1	0	1	0	1	0	1	55
2	0	1	0	1	0	1	0	1	55
3	0	1	0	1	1	1	0	0	5C
4	1	1	0	0	1	1	0	0	CC
3	0	1	0	1	1	1	0	0	5C
2	0	1	0	1	0	1	0	1	55
1	0	1	0	1	0	1	0	1	55
0	0	1	0	1	0	1	0	1	55
-1	0	1	0	1	0	1	0	1	55
-2	0	1	0	1	0	1	0	1	55
-3	0	1	0	1	0	0	1	1	53
-4	0	0	1	1	0	0	1	1	33
-3	0	1	0	1	0	0	1	1	53
-2	0	1	0	1	0	1	0	1	55
-1	0	1	0	1	0	1	0	1	55
0	0	1	0	1	0	1	0	1	55

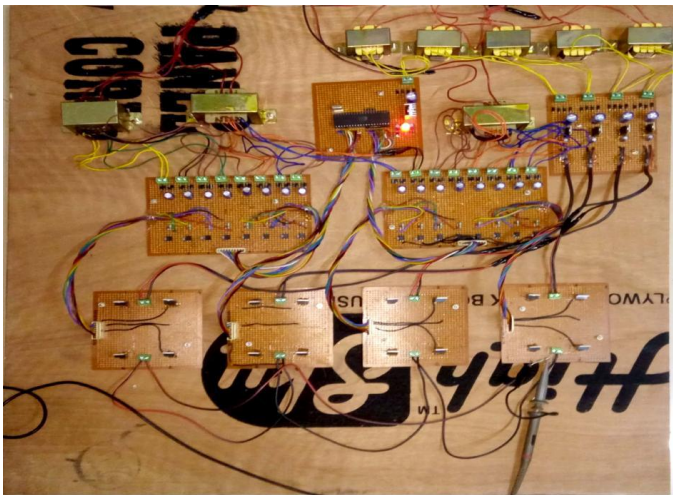

Fig 5.6: Hardware model

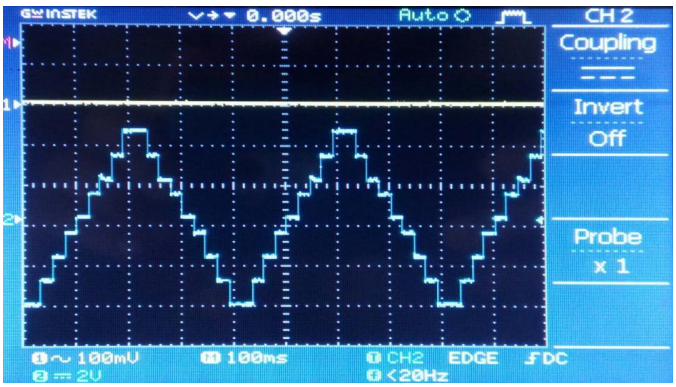

Fig 5.7: Nine level output waveform

CHAPTER 6: ADVANTAGES, DISADVANTAGES AND APPLICATIONS

Advantages

- *They are able to generate high output voltages with very low distortion and lower dv/dt.*
- *They are able to bring in input current with very low input distortion.*
- *Well suited for reactive power compensation.*

- *They can be functioned with a much lower switching frequency.*
- *Disadvantages*
- *It required huge number of switches.*
- *It requires isolated voltage source for a bank of series capacitor for voltage*
- *balancing.*

APPLICATIONS

This hardware may helpful in various applications like;

- *Interfacing with Renewable Energy sources*
- *Back to back Frequency Link System*
- *Power Factor Compensators*
- *DC Power Source Utilization*
- *Electric Vehicle drives*
- *Motor Drives & Active Filters*

CHAPTER 7: CONCLUSIONS

From this project we are known about different types of MLI, basic circuit diagrams, switching, and hardware circuits likes mosfet driver circuit, power supply for micro controller circuit, Ac to 12V Dc converter circuit and H-Bridge circuit.

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