A Novel High Speed Power Efficient Double Tail Comparator in 180nm CMOS Technology

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Abstract *- Comparator is one of the basic building blocks in most analog to digital converters. Many high speed analog to digital converters require high speed and low power comparators. This paper presents the idea of a new double tail comparator, which is more power efficient and high speed in operation. A model for the comparator is developed and its functionality is verified by showing a comparison of result between the proposed model and the existing models. Initially a study on the conventional comparator is performed. It is followed by the simulation of the circuit. Then the study and simulation of a single tail comparator is performed. The estimation of power and delay is also performed. Later the design and simulation of double tail comparator is performed. The core objective of designing a high speed and power efficient comparator is accomplished. The platform used to develop and analyze the models is cadence virtuoso tool.*

Keywords: comparator, schematic, simulation, DRC, LVS, layout.

1. INTRODUCTION

Comparator is one among the basic building blocks in most analog to digital converters. Comparators compares an analog signal with another analog signal and outputs a binary signal based on the comparison. The comparator can act as a decision-making circuit. The comparator is widely used for converting analog signals to digital signals. Comparators can be classified broadly into dynamic and static comparators depending upon whether its operation is controlled by clock signal. Static latched comparator suffers from high power con-sumption and slow regeneration process and thus is not suit-able for and low power and high-speed applications. Dynamic comparators were proposed to reduce power consumption and enhance comparison speed. It finds application in high-speed ADCs.

Many high speed analog to digital converters require high speed and low power comparators. CMOS evolution has reached a point where power is the crucial factor. A major issue is the decreasing supply voltage. The supply voltage has dropped from 5 V in the early nineties down to 1.8 V. Today the drop in supply voltages is expected to cause serious roadblocks for analog circuits, because the signal headroom becomes too small to design circuits with sufficient signal integrity at reasonable power consumption levels. The analog transistor properties are the same for identical bias conditions. But lower supply voltages require biasing at lower operating voltages which results in worse transistor properties, and hence yield circuits with lower performance. The second issue that occurs is the gate leakage. Gate leakage will increase extremely when migrating to newer technologies. When the gate oxide thickness is reduced to the equivalent of one atomic layer, the gate current increases by approximately one order of magnitude.

2. METHODOLOGY

This work aims at optimisation of power and delay for the double tail comparator using the different power reduction techniques. The delay and power of the conventional topologies are estimated. Then the analysis and comparison is performed for a better design. Since the proposal aims at power and delay optimisation, a study on existing power reduction techniques is required. The design of a high speed power efficient double tail comparator requires detailed analysis of power in the existing topologies. The detailed analysis and comparison of the different designs is to be performed.

2.1 SINGLE TAIL COMPARATOR

A single tail comparator is the conventional dynamic comparator with a tail transistor at its bottom end. The tail transistor present controls the circuit functioning. The clock provided improves the functionality of the circuit as it controls the transistors switching them ON and OFF. The working of the comparator circuit can be explained in two phases namely reset phase and evaluation phase. The operation of the comparator is as follows.

During the reset phase when CLK=0 and Mtail is off, reset transistors (M7,M8) pull both output nodes to VDD to define a start condition and to have a valid logical level during reset. During the comparison phase, when CLK=VDD, transistors M7 and M8 are off, and Mtail is on. Output voltage nodes, which had been pre-charged to VDD,

start discharging with different rates depending on the corresponding input voltage.

Assuming the case where IN1>IN2, Out1 discharges faster than Out2, the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Out2 pulls to VDD and Out1 discharges to ground. If IN1 <IN2, the circuits works vice versa.

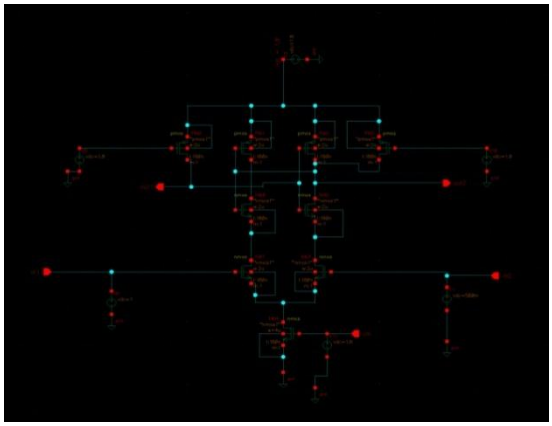

Fig. 1. Circuit diagram of a conventional Single tail comparator

2.2 DOUBLE TAIL COMPARATOR

The architecture of a Double tail dynamic comparator which is designed to operate at low voltages is shown in the figure. It can be observed from figure that the architecture contains separate input gain stage and output latch stage. This comparator architecture does not require too many transistors and are designed to operate at lower supply voltages when compared to conventional comparators.

The double tail architecture contains wider Mtail2 for fast latching and low current in the input stage due to small Mtail1. This small Mtail1 reduces offset and fast latching is found to be independent of the input common-mode voltage (Vcm). At the Reset phase, when CLK=0 both the tail transistors Mtail1 and Mtail2 are in OFF state ,while M3 and M4 transistors makes the fn and fp nodes to be charged to VDD denoting the start condition.

During the comparison phase, when CLK=VDD, the tail transistors becomes ON, while the p-mos transistors M3 and M4 turns OFF. Meanwhile voltages at fn and fp nodes start to discharge depending on the input voltages. The two cases depending on the input voltages are: If VINP>VINN, fn starts discharging at a rate faster than the node fp, which results more current in M2 than in M1. If VINN >VINP, fp starts discharging at a rate faster than the node fn.

The differential voltage builds up, is passed through the MR1 and MR2 transistors to the back to back cross coupled inverters and protects the circuit from the adverse effects of switching noise called kickback noise [3]. With less stacking, this type of architecture is suited for low supply voltages. But, during reset phase, fn and fp nodes have to be charged from ground to VDD, which increases power consumption.

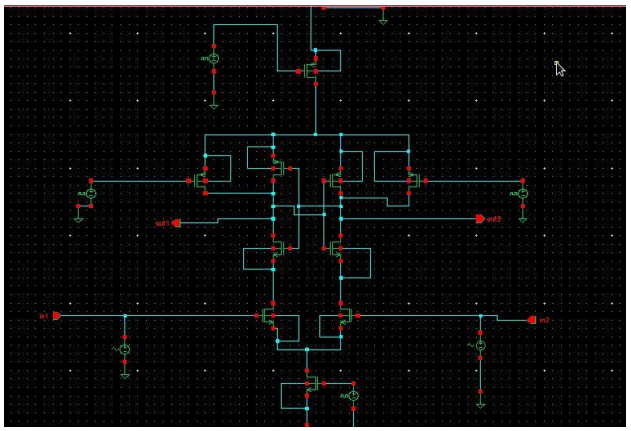

Fig. 2. Circuit diagram of conventional double tail comparator

2.3 DOUBLE TAIL COMPARATOR IN 16T CONFIGURATION

The configuration is named so due to the use of a total of 16 transistors in the circuit. It includes seven pmos and nine nmos transistors. The 16T configuration includes the use of two control transistors, two intermediate transistors and two nmos switches. The introduction of these additional transistors leads to reduction in the value of power and delay.

The control transistors in the double tail comparator with control transistors architecture form a direct current path from VDD to ground leads to static power consumption. During the reset phase, both the outputs which were precharged to VDD is grounded by the intermediate transistors. Another change in the circuit is the presence of two nmos switches. In order to minimize static power, two NMOS switches [Msw1 and Msw2] are added below the input transistors [IN1 and IN2].

At the beginning of the decision making process, both the switches are closed, since F1 and F2 nodes are charged to VDD.

While in evaluation phase nodes F1 and F2 start to reduce with different discharging rates. Switch in the F2 charging path is opened in this case, where F2 is pulling up to the VDD, meanwhile F1 should be discharged completely. This prevents current drawn from VDD to drop through the F2

path. The other switch in the path of F1 node is closed and allows F1 node to discharge.

3. SIMULATION RESULTS

The simulation results obtained using the cadence tool are incorporated below. The modified circuit of a double tail comparator is simulated. The transient response of the schematic is derived and the estimation of power and delay is performed. The performance is evaluated by comparing the values obtained.

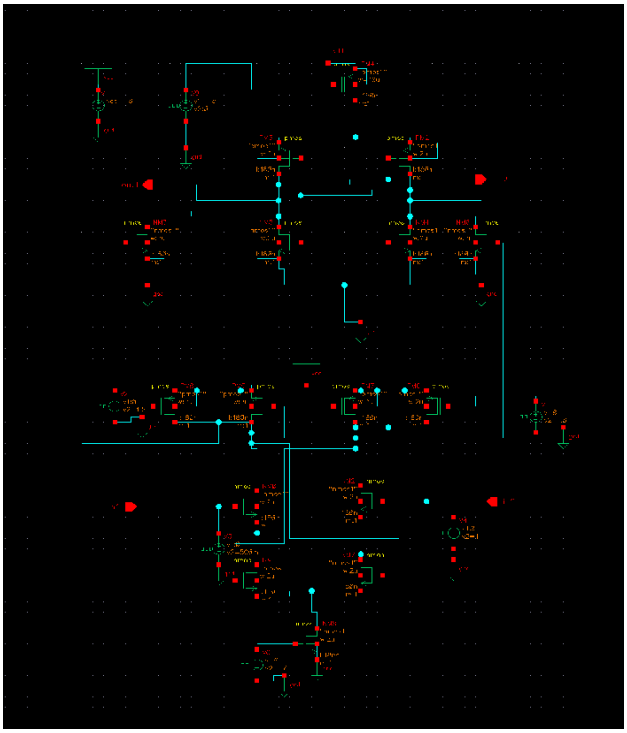

Fig. 3. Schematic diagram of comparator in 16t configuration

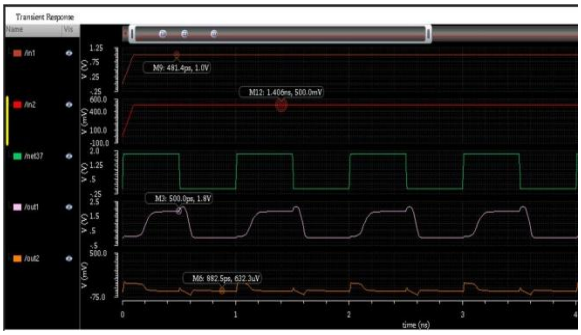

Fig. 4. Transient response of double tail comparator in 16t configuration

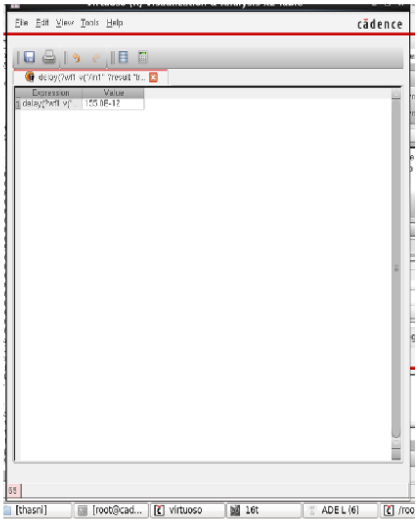

Fig. 4. Delay of comparator in 16t configuration

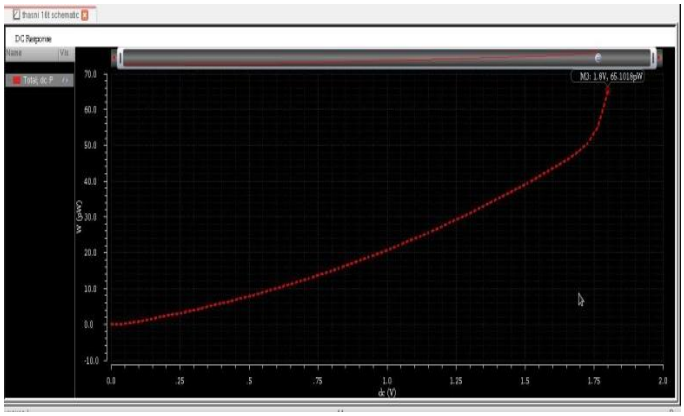

Fig. 5. Power of double tail comparator in 16t configuration

4. LAYOUT

An IC layout is ideally the representation of an integrated circuit in terms of geometric shapes in a plane which correspond to the arrangement of metal, oxide, or semiconductor layers that constitute the components of the integrated circuit.

The term integrated circuit layout is otherwise referred IC layout or IC mask layout. After the estimation of power and delay the layout of the optimised circuit in the 16T configuration is drawn using Assura. The layout is the actual plan of how the circuit is to be placed in an integrated circuit.

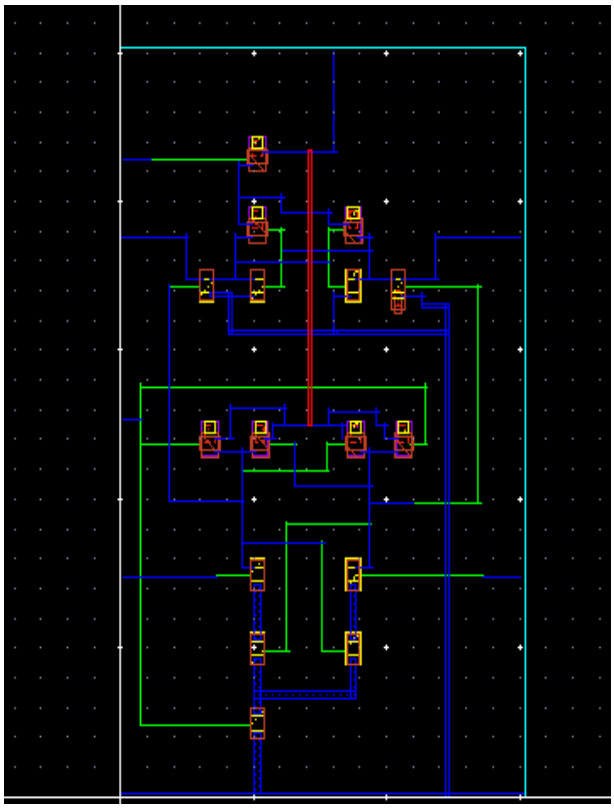

Fig. 7. Layout of double tail comparator in 16t configuration

5. PHYSICAL VERIFICATION

The process of Physical verification relies upon comparing and crosschecking an integrated circuit layout (IC layout) design via EDA software tools to ensure perfect electrical and logical functionality and feasibility. The steps of physical verification mainly consists of running a DRC and LVS in ASSURA.

A. Running a DRC

DRC is a design rule check constraint which check the physical checks of metal width, pitch and spacing requirement of different layers with respect to different manufacturing processes. Whenever we give physical connection to components we have to consider the DRC rules. Otherwise it will lead to failure of functionality of a system.

The main objective of design rule checking is to achieve a high overall yield and reliability for the design. If the design rules are violated the design will not function properly. To meet the goal of improving yields, DRC has evolved from simple measurement and boolean checks to more complex set of rules that modify existing features, insert new features, and check the entire design for process limitations such as layer density.

A completed layout consists not only of the geometric representation of the design but also data that provides support for the manufacturer of the design. While design rule check do not validate that the design will operate correctly, they are constructed to verify that the structure meets the process constraints for the given design.

Fig. 8. Result of DRC run

B. Running LVS

Layout Versus Schematic is the class of electronic design automation verification software that determines whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design. A successful DRC ensures that the layout conforms to the rules designed or required for faultless fabrication. However, it does not guarantee if it really represents the circuit you desire to fabricate. This is the case where an LVS check is used.

6. CONCLUSION

This paper proposes a power efficient and high speed double tail comparator in 180nm CMOS technology. Different power minimisation techniques are applied for a better design. The performance of different comparator architectures have been analyzed in terms of power and delay. . The comparator architectures are implemented and performance parameters are analyzed. It is observed that the performance of conventional comparator modified using various techniques by adding extra transistors is found to be better than the conventional structure. The simulation results obtained for modified comparators shows that the double tail comparator operate at low supply voltages, consumes less power and delay and also the power of the comparator architecture in 16T configuration is found to be lesser than other architectures

Fig. 9. Result of LVS run

CONFIGURATION	POWER (pW)	DELAY(ps)
SINGLE TAIL	52.19	196.4
DOUBLE TAIL	183.6	1150
USING 13T	201.4	117.1
USING 14T	486.2	98.44
USING 16T	65.1	155

Fig. 10. Tabulation of power and delay values obtained by simulation

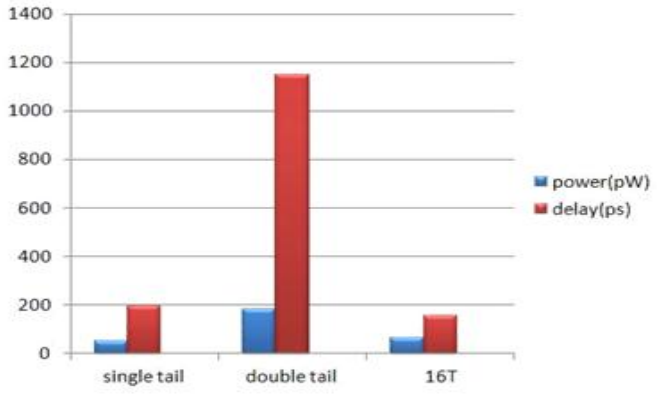

Fig. 11. Comparison of results obtained in simulation

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