

An Evaluation of the Performance Parameters of CMOS and CNTFET based Delay Line at 32nm Technology

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Abstract - In the current article a comparative study of various parameters of ring delay line were evaluated using the comparative technology of CMOS and CNT node. After the comparative study the outcomes exhibited that the CNT exhibit improved results as compared to the CMOS technology using the Spice tool. The various parameters evaluated were leakage power Consumption including the factors: preposition delay, leakage power, and leakage current and average power. After the evaluation parameters, the results concluded that the CNT transistor exhibited improved results and yield as collate to the CMOS technology as this have physical fundamental limits in near future. Along with this the demand of CNT 32 nm is enhancing each day. The power consumption diminished in delay line operates CNT. So, in this article CNT indicated improved evaluation and performance variables for delay line as compared to CMOS technology.

Keywords: Carbon nanotubes, CMOS, Delay line, Preposition delay, leakage current, leakage power.

1. Introduction

When a specified time constant is pre-recognized, which in itself introduces delay time to the signals; such devices are known as delay lines. The main characteristics of such type of devices are delay step and range and jitter performances. There is a difference amongst the delay line and delay step, the former is the maximum time by which the existing signal or the signal produced can be delayed where as the latter measures the minutest incremental step of time which can be produced by delay line. Jitter is referred to as uncertainty of the time in the signal which is delayed by output. This delayed output affects the small delay steps. This delay line it plays a considerable part in various sub systems of the TIM i.e. time interval measurement circuits being both ways, time tp digital convertors and digital to time convertors, i.e. TDCs and DTCs. One of the applications of delay line is in range imaging, in this the 3dimensional range images are captured using the delayed light pulse. For the data synchronization, regarding the moving, delay and storing of data on a definite time window is performed using TDL i.e. digitally tapped delay line. The applications of CMOS delay lines are in distribution of clock as well as the

recovery of clock data so that the requirements of the prescribed clock deskew are satisfied. They also exhibit application in controlling the debugging and testing of the digital VSLI circuits which perform on high speed and high performance using the accurate and exact pulse edge placement. Further, they are also utilized over measurements of time on-chips and synchronizing CPU along with the involvement of the interfaces [1].

Delay lines are basically of two types mainly based over the optical and the electronic technology. The resolution of the highest and the maximum delay step is determined via optical delay lines. They exhibit the delays of even the minutest picoseconds ranges with the increments which are linear. If the air aperture depth amongst input and output fiber optic transceiver is adjusted then also the signal is delayed. This illustrates that as the distance of a light travel is greater amongst the two points, the output signal will be delayed simultaneously. There is a limitation of the optical delay being the delay range which is just few 100ps. When there are extremely long delays, there are various optical delay lines which on maintaining their linearity and resolution extend the ranges. But, these are acquired on the basis of the complexity of the system as fiber optic cables are being used exhibiting an expensive, fragile and bulky setup. On comparing this system with the existing one there is a reduced system complexity and the costs too [2].

Continuous ascend of CMOS technology is the vital driving ingredient toward the exponential swelling in integrated circuit speed and density. Currently transistors are 20 times speedy and engage declined than 1% of the locality of those fabricated 20 years back. However, ascend of CMOS automation behind sub-nanometer scopes leads to numerous vital threats, such as improved short-channel effects, ex- potentially gaining leakage currents, better power densities, and diminished gate control [3]. On one hand, these threats have fabricated a bottleneck for sustained improvements of low power and better performance electronic gadgets. Diversely, these limitations have also initiated new vulnerabilities in security approaches, such as ciphers. Improved static leakage has been exploited to initiate power-side-channel attack on

ciphers [4]. As we progression into an age of nano-technology, components with maximum carrier mobility and appliances structures with better electrostatic fortunes are pretty promising alternatives to CMOS technology, such as nanotube, nanowires, CNTFET is ensuing favourable automation for future integrated circuits. Additionally, as the impart voltage is scaled diminished, the leading leakage power of CNTFET based logic gates expands linearly as compared to exponential enlarge of leakage power for CMOS based logic gates² [5].

CNTFET exhibits distinct advantage over MOSFET with regard to area, power and staging; however, another vital aspect to be examined is hardware security, and further precisely, side-channel attacks. Hardware execution of security-vital approaches i.e. ciphers, leak secret observation through covert necks, such as power consumption, electromagnetic emanation, or thermal variations. The strike that utilizes these covert channels to leak secret guidance of security-critical approaches is known as *side channel attack*. Conclusive sophisticated and lethal configuration of the side- channel strike is power-side-channel strike. Analysis in the previous tenner has exhibits that the CMOS technology is vulnerable to power-side-channel attacks [6] [7]. Therefore, CMOS circuit planner is deftly aware of these weakness and incorporate relevant countermeasures while executing security-vital applications. However, there is no certainty to be examined on CNTFET, which is an encouraging alternative to CMOS technology. There are a duplet of drawbacks associated in examine the power-side-channel strikes on CNTFET based circuits. Firstly, the automation is not usually convenient, and neither are CNTFET based ICs, which restriction us to simulation-based outcomes. Secondly, CNTFET based worth cell libraries are not convenient, preventing CNT based circuit simulations [8].

2. Literature Review

Abdul Razzak et.al in 2016 stated the CMOS delay line review, keeping the centre of attention over the high resolution delay step, which is one amongst the most frequently used technique. They further presented the specifications, circuit delays, the principles operating and the primary types. The described of delay circuits in the current articles are worn for delaying the digital inputs and the signals of the clock. They also investigated the topologies of the delay elements which were controlled digitally and were one of the commonest analog, their main attention was over the strategies of the delay tuning. Discussion regarding the IC variables mainly, supply voltage, temperature, sources of the noise and the process which usually effect the resolution of the delay via jitter

timing was also incorporated. The specifications of the designs for delay elements were compared with delay line circuits which were common. The main features which were investigated and derived in this paper were that the challenges which were being faced being techniques of the delay line with effective and efficient high resolution, trade off amongst CMOS delay lines which were designed incorporating either of the two being digitally controlled or the analog delay elements. Further, this article also considered about the drawbacks of the trade-off amid resolution and the scope of the delay and the solutions for the same were also provided. They also illustrated about the CMOS scaling technology which affects the CMOS delay line performance. Further, they also demonstrated the recent trends and all the efforts which was utilized for generating the output delayed signal with jitters which were low in the form of ranges of sub-picoseconds [1].

Jatinderpal et.al in 2014 stated that these CNT multi walled tubes are seeking attention and are one of the promising techniques regarding the applications of the nano-electronics in near future. They stated that they exhibited the replacement potential over the interconnects of the chip copper (Cu) as they have huge carrying capacities of current and conductivity. Amongst the integration circuits, one of the major constraints of designs is delay on the large scale platform of VSLI. They have investigated about the propagation delay and insertion repeaters effects on that delay for both the interconnects of MWCNT and Cu using the different nodes of the technology i.e. 32 nm and 22 nm respectively. The current research deals with voltage scaling effects in the repeaters for lengths of long interconnect in the circuits of VSLI regarding the propagation delay. The reduction in the propagation delay can be attained with enhancing in bias repeater voltage at several interconnects of various length and nodes of technology of 32 nm and 22 nm respectively [6].

3. Research Methodology

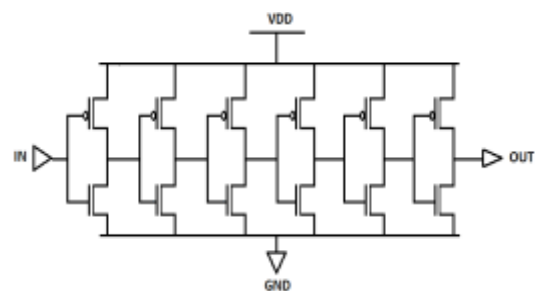


Figure 1: CMOS based Delay line circuit

The three stage delay line circuit as illustrate in figure 1. In this circuit to be used six inverter are connected in parallel of given circuit. All PMOS of given circuit is connected to

the impart voltage VDD and NMOS is connected to the GND of that circuit. The three stage delay line circuit is a closed loop circuit. CNTFET based three stage delay line circuit illustrate in figure 2.

In this circuit all NMOS and PMOS transistor should be replaced by CNT based transistor. CNTFET transistor is hollow spherical structure whose diameter should be range in nanometer scale.

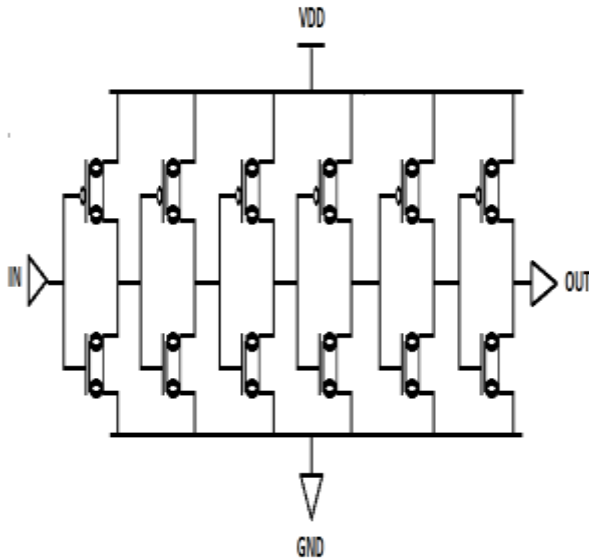


Figure 2: CNTFET based three stage delay line Circuit

The proposed research is evolved such that it can be examined that the CNT will designate a channel field under gate amid drain and source similar to CMOS. In these articles, during to initiation process the diameter of CNT will be established and the current limit is certain based on the number of CNTs worn. The characteristics of CNTFETs are initiated to be similar to MOSFETs and are considered as an absolute substitute to the MOSFET. Further, the operational characteristics of CNTFET and CMOS are initiates to be similar. However, from the proposed research it can be examined that a better current properties due to the substantial doping of source and drain is designate by the CNTFET compared to CMOS. The threshold voltage of CNTFET based channel which is illustrate as the deciding factor for CNTFET is determining using these equation (1)

$$V_T = \frac{E}{2e} = \frac{\sqrt{3}}{3} \frac{aV_\pi}{eD_{cnt}} \quad (1)$$

$$\Delta T = \Delta T_1 + \Delta T_2$$

Where, $a=2.49 \text{ \AA}$ is the carbon-to-carbon atom distance, $V_\pi=3.033\text{eV}$ is the π - π bond energy of carbon in the compact bonding bogus, e is the unit electron charge, and D_{cnt} is the CNT diameter.

4. Simulation Results and Discussion

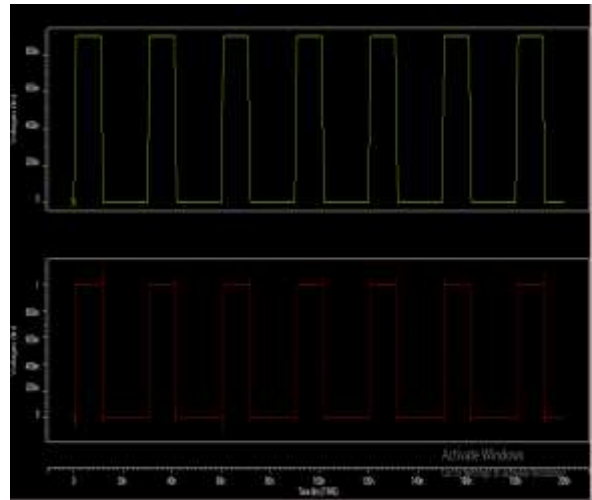


Figure 3: Waveform of three stage Delay line using CMOS

The proposed three stage delay line circuit were simulated using SPICE tools in 32nm technology and their transient analysis of given circuit waveform is acquired at 1v power supply. CMOS based three stage delay line circuit waveform as illustrate in figure 3. Simulated Waveform of three stages Delay line is operating CNT technology to provide noise immunity of signal should be improved and power consumption should be diminished in compare to CMOS technology as clearly seen in figure 4.

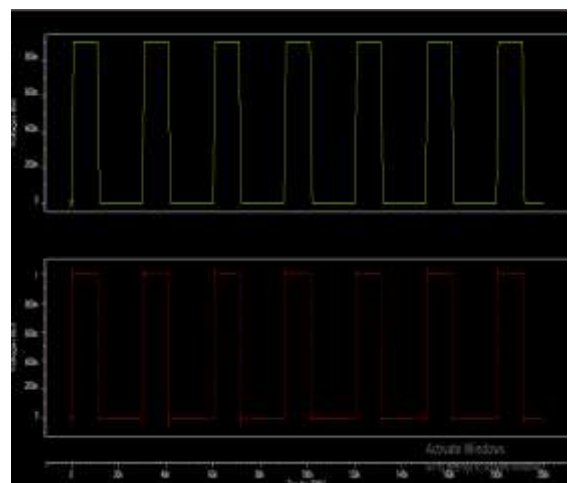


Figure 4: Waveform of three stage Delay line using CMOS

The propagation delay τ_p of a gate describes how speedy it greets to a reversal of its inputs; it indicates the delay affair through a signal when flowing through a gate. It is determined between the 50% transition ends of the input and output waveforms for an inverting gate. τ_{plh} Describes the reply time of the gate for a low to high output conversion, while τ_{phl} mention to a high to low conversion. The propagation delay describe the average of these two

$$\tau_p = \frac{\tau_{phl} + \tau_{plh}}{2}$$

Table.1 Comparison of MOSFET and CNTFET based three stage delay line as shown

Performance parameters	Delay line	
	CMOS	CNTFET
Technology	32nm	32nm
Supply Voltage	1V	1V
Leakage Power	1.5957nW	0.8439nW
Leakage Current	1.5957nA	0.8439nA
Average Power	19.67nW	10.88nW
Delay	10.9nS	10.8nS

Table:1

Table 1 illustrates the simulation results of three stage delay line. In CMOS based three stage delay line leakage power is 1.5957nW and delay is 10.9nS is to be determined with the help of SPICE simulation tools. CNTFET based three stage delay line leakage power was diminished to 0.8439nW and delay is reduced to 10.8nS at 1V power Supply.

Graphical representation of all Parameter was determined in both CMOS and CNTFET as shown in Figure 5.

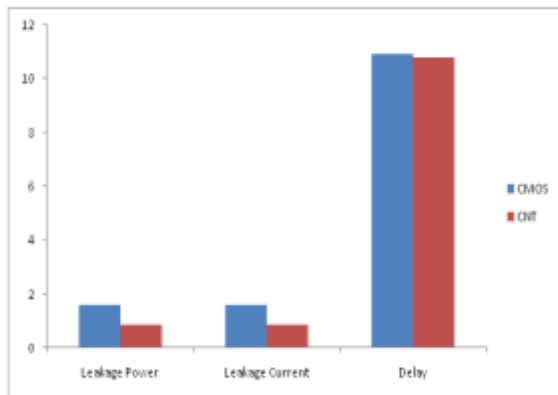


Figure 5: Graphical Representation of Various Parameter of Three Stage Delay Line

5. Conclusions

We barrier FETs, and fashion CMOS-like inverters and deception solution acquired CNT lattice bony feature. The on situation current and trans-conductance of the CNT thin-bony-based FETs are considerably enhanced by diminishing the barrier length, which strength be ascend to nanometric ambit whereas preserving a high current on/off quantitative relation.

These article is proposed such that it compares the traditional CMOS and CNTFET based Delay Line circuit for staging like rise time, fall time delay, power dissipation and transient analysis. This Delay Line circuit is simulated by SPICE tool at 32nm technology for CNTFET and CMOS apparatus as illustrate in Table1. From these articles it can be ascertained that the CNTFET based three Stage Delay line circuits describe better performance like faster output response, less consumption of power, and enhanced transient response in comparison to the traditional CMOS devices.

6. References

- [1] Bilal I. Abdulrazzaq, Izhal Abdul Halin, Shoji Kawahito, Roslina M. Sidek, Suhaidi Shafie, and Nurul Amziah Md. Yunus, A review on high-resolution CMOS delay lines: towards sub-picoseconds jitter performance, 10.1186/s40064-016-2090-z
- [2] Abas MA, Russell G, Kinniment DJ. Built-in time measurement circuits—a comparative design study. Comput Digit Tech IET. 2007;1(2):87–97. Doi: 10.1049/iet-cdt:20060111.
- [3] Melloni A, Canciamilla A, Ferrari C, Morichetti F, O’Faolain L, Krauss TF, De La Rue R, Samarelli A, Sorel M. Tunable delay lines in silicon photonics: coupled resonators and photonic crystals, a comparison. IEEE Photonics J. 2010;2(2):181–194. doi: 10.1109/JPHOT.2010.2044989.
- [4] Klepacki K, Pawłowski M, Szplet R. Low-jitter wide-range integrated time interval/delay generator based on combination of period counting and capacitor charging. Rev Sci Instrum. 2015;86(2):025111. doi: 10.1063/1.4908199.
- [5] Jatinderpal, Chakshu Goel, Karamjit Singh Sandha, Performance and Analysis of Voltage Scaled Repeaters for Multi-Walled Carbon Nanotubes as VLSI Interconnects, International Journal of Computer Applications (0975 – 8887) Volume 93 – No.8, May 2014, 18.
- [6] M.K. Majumder, N.D. Pandya, B.K. Kaushik and S.K. Manhas, Dynamic crosstalk effect in mixed CNT bundle interconnects, ELECTRONICS LETTERS 29th March 2012 Vol. 48 No. 7.