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IMPLEMENTATION OF MODIFIED H-BRIDGE MULTILEVEL INVERTER TOPOLOGY FOR SOLAR PHOTOVOLTAIC SYSTEM

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Abstract - *In this project, a new configuration of Multilevel Inverter (MLI) topology based on modified H-bridge seven level inverter is proposed, which can produce more voltage level with reduced number of switches when compared with cascaded H-bridge topology. In proposed MLI topology, only eight switches are required to generate seven level output, whereas twelve switches are required for conventional cascade H-bridge topology. Moreover, to resolve problems related to dc source fluctuations with Solar Photovoltaic, the Sinusoidal Pulse Width Modulation (SPWM) technique is developed. The switching losses, voltage stress on power devices and cost are reduced due to less number of switches. Further, Total Harmonic Distortion (THD) of load current less than 2% is achieved with small size low pass filter. Simulation results has been done in MATLAB and to validate the feasibility and performance of seven level Multilevel Inverter hardware setup has been developed. The PIC Microcontroller is used to produce gate signals based on SPWM technique for the gates of the MOSFET switches. The results are verified experimentally with seven level Multilevel Inverter circuit for 10 W Solar Panel with resistive load.*

***Key Words*: Low switching frequency, Modified H-bridge converter, SPWM technique and Single phase seven level inverter.**

1. INTRODUCTION

The multilevel inverter has been introduced since 1975 as alternative in high power and medium voltage situations. Various multilevel inverter topologies were proposed in the past decade, which have been extensively studied for renewable energy integration systems.The multilevel inverter generated the sinusoidal output voltage waveform, where power switches operated at low switching frequency. Fig 1 shows seven level multilevel inverter powered with solar photovoltaic. Which operates on seven voltage levels and inverts the direct current (DC) to alternating current (AC) with lower switching losses and reduced harmonic distortion. The AC load is connected to the inverter and inverter producing a sinusoidal output voltage.

Various topologies for multilevel inverter have been proposed over the years, aiming to construct a sinusoidal waveform for several DC-voltage levels, such as diode clamped multilevel inverter, flying capacitor multilevel inverter, cascaded H-bridge multilevel inverter, and modified H-bridge multilevel inverter. The proposed circuit is based on a resonant switched capacitor converter (RSCC), and voltage balancing of input capacitor technique. The main purpose of multilevel inverter topology for high power industrial applications and switching losses, voltage stress on power devices and costs are reduced due to less number of switches.

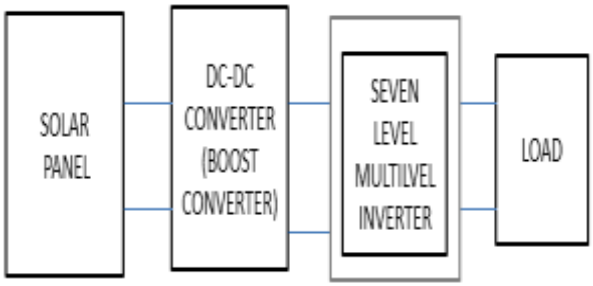

Fig- 1: Seven level multilevel inverter

2. TOPOLOGY OF MODIFIED H-BRIDGE INVERTER

H-bridge is an electronic circuit that enables a voltage to be applied across a load in either direction. These circuits are used for robotics and other applications to allow DC motors to run forwards and backwards. Most DC-to-AC converters (power inverters), most AC-to-AC converters, the DC-to-DC push–pull converter, most motor controllers, and many other kinds of power electronics use H bridges. In particular, a bipolar stepper motor is almost invariably driven by a motor controller containing Two H Bridges. Three-phase configuration can be easily implemented by three single-phase structures. Soft switching techniques can be used to reduce switching losses and device stresses. The advantages are; (1) switching at (or nearly) the fundamental frequency, drastically reduces switching losses. (2) elimination of the transformer in providing required voltage levels. (3) easier packaging due to the simplicity of its structure and its low component count.

2.1. Proposed Multilevel Inverter Topology

The structure of the Modified H-bridge multilevel inverter is shown in Fig 2. This inverter consists of H-bridge, single voltage source, eight controlled switches and four diodes.

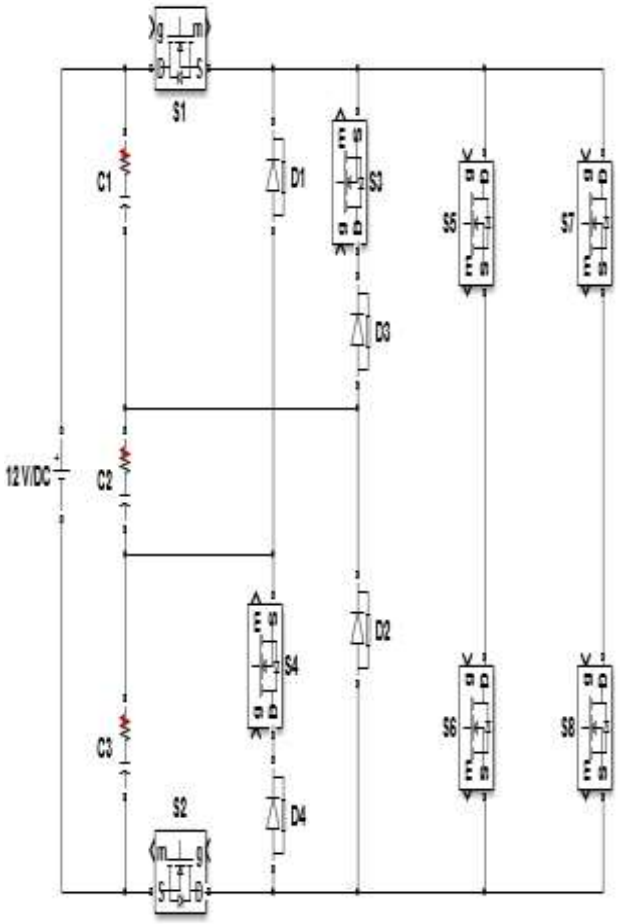

Fig- 2: Proposed seven level inverter model

An input voltage divider comprises four series capacitors C_1, C_2, and C_3. The divided voltage is transmitted to H-bridge by four MOSFET switches, and four diodes. The proposed multilevel inverter generates seven-level AC output voltage with the appropriate gate signals.

Table-1: Switching Combinations at Different Voltage Levels

Voltage Level	Switching ON-State
1/3 Vdc	S1,S5,S8,D2
2/3 Vdc	S1,S5,S8,S4,D4
Vdc	S1,S5,S8,S2
-2/3 Vdc	S7,S6,S2,D3,S3
Vdc	S7,S6,S2,S1
0	S7,S5

2.2 Topology Comparision

Table 2 presents the number of components required to implement a seven level inverter using the proposed topology and previous one that can be considered as the standard multilevel configurations, the cascaded multi-cell inverter

Table-2: Comparison between Proposed and Existing Seven Level Inverter Model

Device	Existing Model	Proposed Model
Power Switch	12	8
Input Source	3	1
Input Capacitor	-	3
Diode	-	4

3. RESULTS AND DISCUSSION

The major feature of the proposed topology is the reduction of power components. The Sinusoidal Pulse Width Modulation is used to control the circuit. The proposed Seven Level Multilevel is implemented in MATLAB/Simulink.

3.1 Simulation Result

Table 3 shows the components and their ratings considered simulation. The figure 4 shows the circuit of subsystem producing positive half cycle.

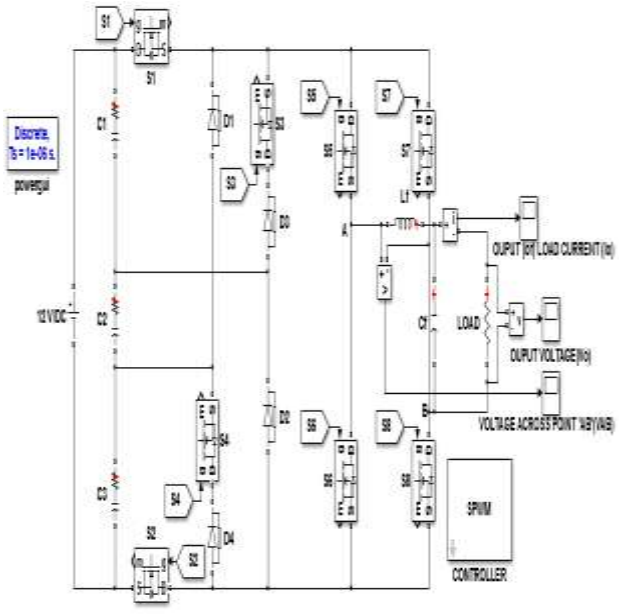

Fig-3: Proposed Seven Level Inverter-Simulink model

Table-3: Components and its Ratings in Simulation

Component	Value
Input Voltage	12V/DC
Capacitor C1 TO C3	1000 µF
Inductive Filter	1 mH
Capacitive Filter	10 µF
Resistive Load	25 Ω
Switching Frequency	18 kHz

Which is present in the main simulation circuit. This circuit shows seven level inverter. This capability simplifies the creation and management of designs that share components, as one model can represent a family of designs. Conditionally executed subsystems let it change system dynamics by enabling or disabling specific sections of design via controlling logic signals.

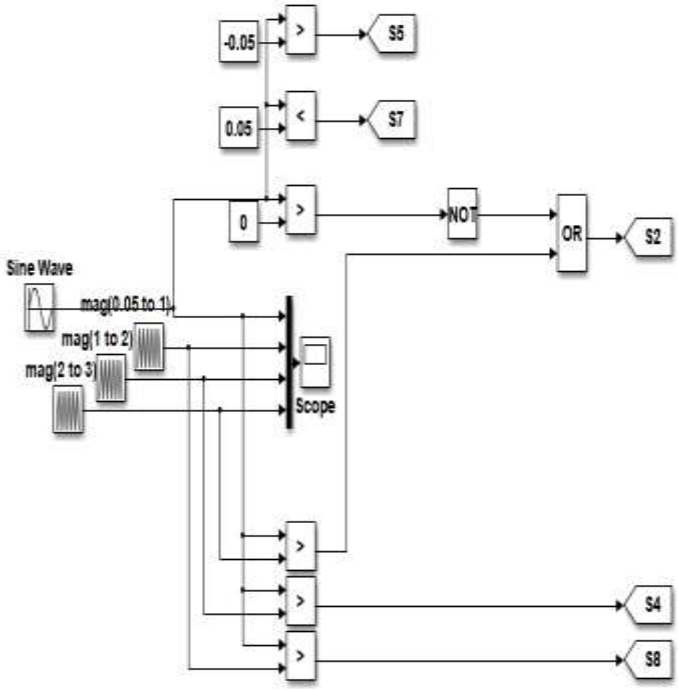

Fig- 4: Positive half cycle generation.

Simulink lets it create control signals that can enable or trigger the execution of the subsystem based on specific time or events. This include blocks for creating simulation tests. For example, the Signal Builder block lets us to graphically create waveforms to exercise models. Using the Signal & Scope Manager, we can inject signals into the model, as well as log and view signals, without adding blocks. Simulink also provides model verification blocks to check that block outputs conform to our design requirements

The positive half cycle generating switches are S2, S4, S8, S5, S7. This switches are compared with four carrier signals (triangular wave) magnitude of each carrier signal is (0.05 to 1), (1to 2), and (2 to 3) these are positive side ON switches. So, all magnitude values are positive. The reference signal is the pure sine wave and it is also called as modulation signal. The amplitude of the reference signal is 3.8 meters. Initially, the switches S5 and S7 producing a zero level and it is start conducting from +0.05 seconds to -0.05 second and other switches are when reference signals are greater than the carrier ($V_{sin} > V_{tri}$)the switches starts to conducting. The switch S2 will conduct ON both ($V_{sin} < 0$ and $V_{sin} > V_{tri2}$) for producing negative cycle.

The Fig 5 shows the individual switches are conducting in positive half cycle.

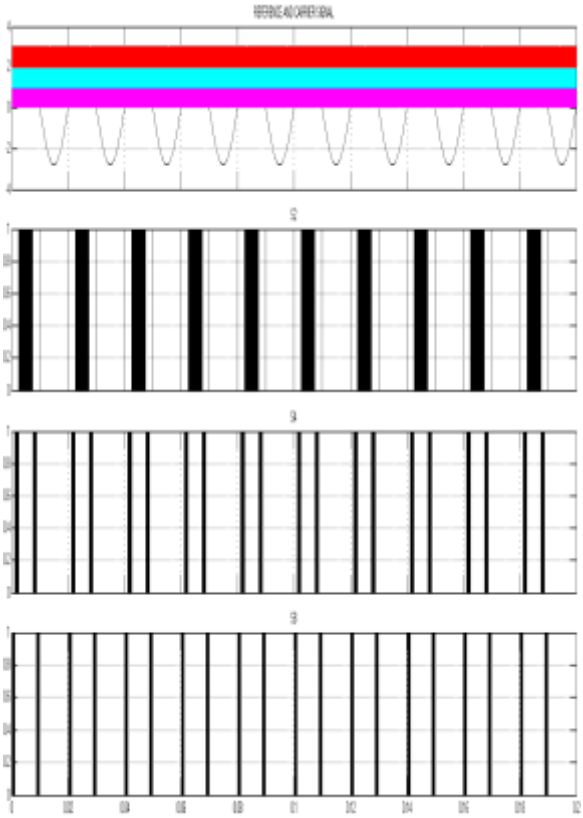

Fig-5: Positive Half Cycle ON Switches

The negative half cycle generating switches are S1, S3, S6 shows the Fig 6.This switches are compared with four carrier signals (triangular wave) magnitude of each carrier signal is (-0.05 to -1), (-1 to -2), and (-2 to -3) these are negative side ON switches. So, all magnitude values are negative. The amplitude of the reference signal is 3.8 meters. When the switches are greater than or less than the carrier and sine wave ($V_{sin} > V_{tri}$) or ($V_{sin} < V_{tri}$) the switches starts to conducting. The switch S1 will ON both ($V_{sin} > 0$ and $V_{sin} < V_{tri1}$) for producing positive cycle.

The Fig 7 shows the individually conducting the S1, S3, S6 switches in the negative half cycle generation. These switches are only negative side conducting Switches.

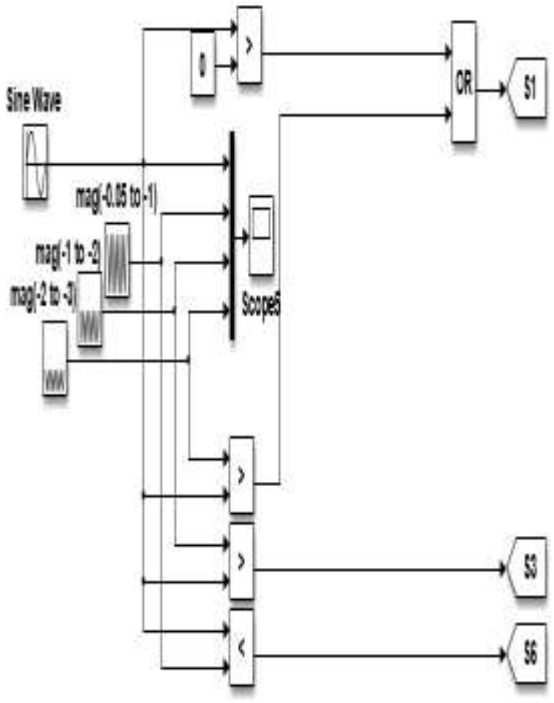

Fig- 6: Negative half cycle generation

Fig-7: Negative Half Cycle ON Switches

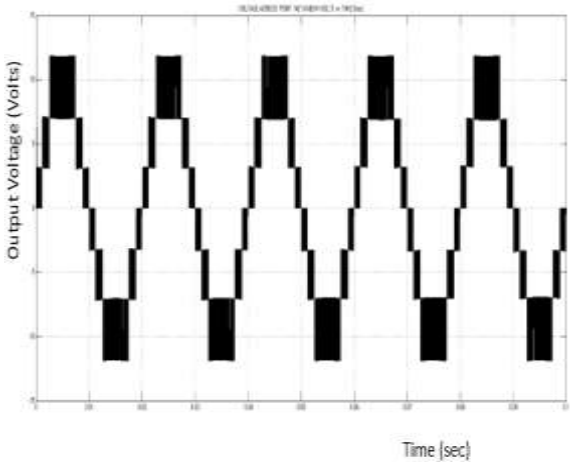

Fig-8: Output Voltage across Vab

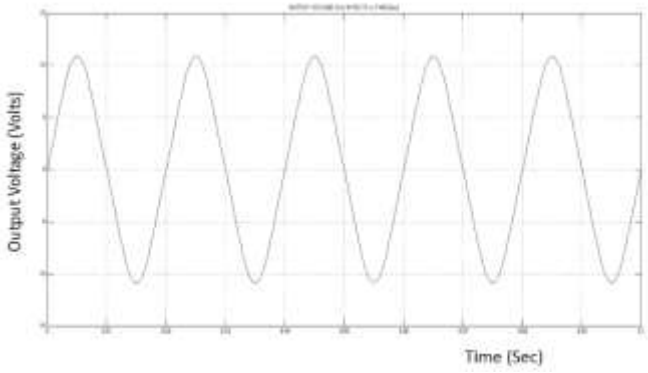

Fig-9: Output Voltage (Vo) after filter

The Fig 8 shows the seven level stepped output voltage waveform Vab with using filter. The Fig 9 shows the output voltage waveform of proposed topology after including low pass filter (L=1 milli Henry, C=10 micro Farad) across resistive load. It shown that the output voltage waveform is almost sinusoidal. The output load current is shown in Fig 10.

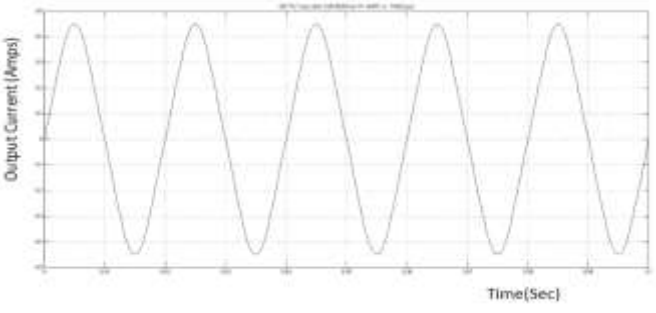

Fig-10: Output Current (Io) after filter

The Fig 11 shows the output voltage waveform with filter. It is a sinusoidal waveform which gives the efficient output voltage and it produces a very less harmonics in the circuit.

Which is achieved by using small size of low pass filter. The minimal Total Harmonic Distortion (THD) of 4.83% is achieved which is less than IEEE 519 standard.

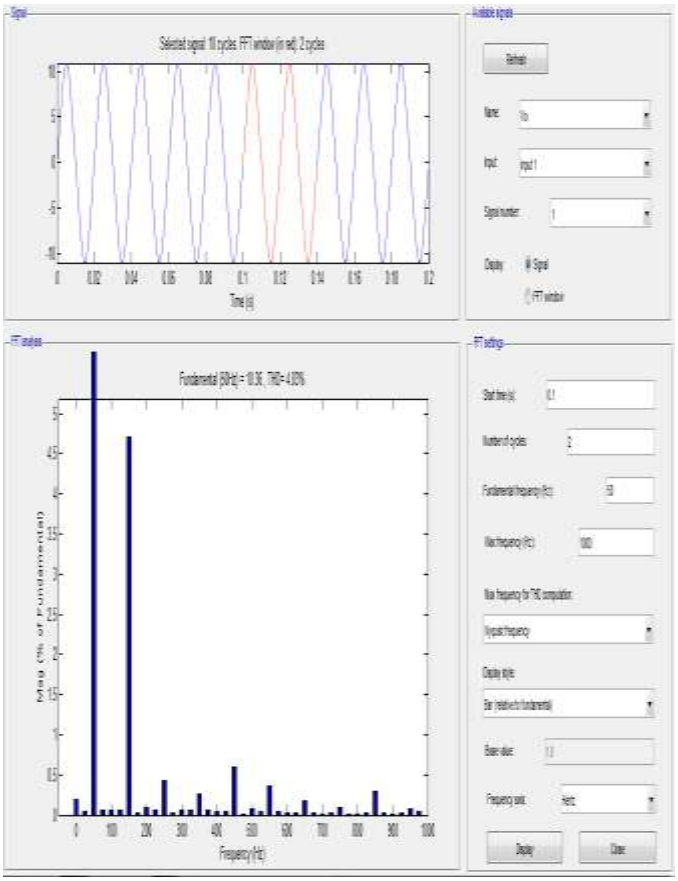

Fig-11: Harmonics level with filter

3.2 EXPERIMENT RESULT

The hardware setup for modified h-bridge multilevel inverter topology output is fed to the load. The input of circuit solar or battery. The solar panel rating 12V, 10W or give up battery as input which would be charge around 12V.The AC voltage of 230V is step down to 12V from step-down transformer and 12V AC input is rectified into 12V pulsating DC with the help of full bridge rectifier circuit. The ripples in the pulsating DC are removed and pure DC is obtained by using a capacitor filter. The positive terminal of the capacitor is connected to the input pin of the 7812 regulator for voltage regulation. An output voltage of 12V obtained from the output pin of 7812 is fed as the supply to the pulse amplifier. An output voltage of 5V obtained from the output pin of 7805 is fed as the supply to the micro controller. From the same output pin of the 7805, a LED is connected in series with the resistor to indicate that the power is ON. First block is controller block, which has PIC16F876A microcontroller is used to generate triggering pulse for MOSFETs. The current gain of PIC Microcontroller are very less and then added to the buffer amplifies the current gain. The PIC microcontroller is programmed using assembly language and it generate the gate signal for boost converter and seven level multilevel inverter switches. Which are used totally eight MOSFET switches (IRF840), three capacitors, four diodes. The isolation for these four MOSFET (H-bridge) for gate driving circuit (FAN7392N). There are one gate driver circuit for two MOSFET and hence two set of gate driver circuit. In this block part of four MOSFET for seven level inverter and one MOSFET part of boost converter and hence five MOSFET switches. In this block providing isolation for these MOSFET and optocoupler in second block are each MOSFET for one optocoupler and hence five optocoupler. The operating voltage of optocoupler (TLP250H) are 12V that is given by power supply circuit. Each optocopuler has to be given individual power supply 12V.One transformer for pic controller circuit and five transformer for optocoupler power supply circuit. The Fig 12 shows the seven level stepped output voltage waveform hardware setup without using filter.

Table 4 shows the parameters value for 10 Watt solar panel 12V dc and Table 5 shows the hardware components use to implement the proposed seven level inverter

Table -4: Parameter Value of Solar Panel

Parameter	Value
Peak Power (Pmp)	10 W
Open Circuit Voltage (Voc)	22.96 V
Short Circuit Current(Isc)	0.74 A
Peak Power Voltage (Vmp)	19.45 V
Peak Power Current(Imp)	0.65A

Table- 5: Hardware components use to implement the proposed seven level inverter

Parameter	Value
Solar panel	12 V
MOSFET(IRF840)	500 V,8 A
Diode(IN4007) D1 TO D4	100 V, 1 A
Capacitor C1 TO C3	1000 µF
Boost converter	L=10 mH, C=22 µF, Diode(IN4007),MOSFET(IRF84), Resistive load (100 kΩ)
LED	12 V,2.4 W,O.2 A
Resistive load	100 kΩ

Fig-12: Hardware Setup for Seven Level inverter

The solar panel is kept on sun for long time we can get output voltage 30V across the boost converter. The input voltage of 12V are boosted to 30V.The probes are connected to DSO across the resistive load and verify the seven level inverter stepped output voltage waveform. The Fig13 shows the stepped output voltage waveform for seven level multilevel inverter.

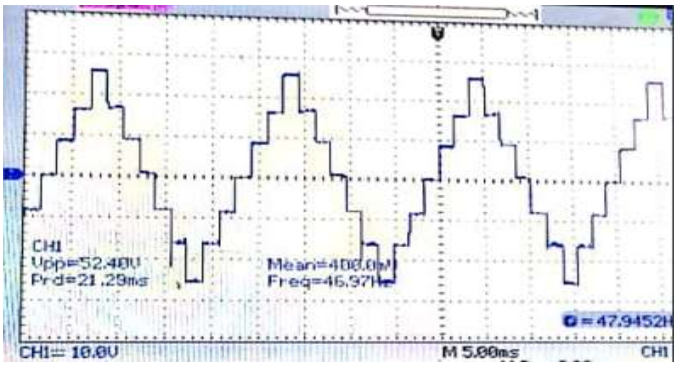

Fig-11: Stepped output voltage waveform for seven level multilevel inverter

4. CONCLUSION

A new topology of Modified H-bridge Multilevel Inverter has been proposed in this work. When comparisons with the CHB and cascaded half -bridge topologies show that the proposed MLI topology, only eight switches are required to generate seven level output waveform. As result, the installation cost and space of multilevel inverter are reduced. Simulation results demonstrate that, by applying Sinusoidal Pulse Width Modulation (SPWM) technique of the staircase-like voltage waveforms are obtained and PIC microcontroller is used to produce the gate pulse in hardware setup of this project. The pulses are generated by the gate driver circuit and it is given to the switches of the multilevel inverter. Thus the hardware is implemented with output voltage waveform of the multilevel inverter is a stepped wave with seven levels. The result demonstrates that the proposed topology can be substituted to control the seven level multilevel inverter suitable for medium-voltage renewable energy integration with improved control performance.

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