Simulation of High \( k \) dielectric MOS with Hfo\(_2\) as a gate dielectric

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**Abstract**- Conventional MOS over 40 years has been fabricated using Silicon substrate with polysilicon in gate material. As scaling of SiO\(_2\) increases, a serious issue in terms of tunneling current and oxide breakdown raises. To overcome these problems, silicon based MOS with High-\( k \) dielectric material in gate is becoming a strong alternative for replacing the conventional SiO\(_2\) dielectrics gates MOSFETs. High-\( k \) oxides provide a solution to leakage problems and improve performance such types of MOS can be used in both application of high performance and low power consumption. In this paper, HFO\(_2\) based high \( k \) dielectric gate is used for the formation of device because HFO\(_2\) is having high dielectric constant value and improves the performance of the device. On the basis of some electrical parameters, a comparative study in between conventional MOS and High \( k \) dielectric MOS is also presented.

**Keywords:** High \( k \) material, Hfo\(_2\), Leakage current, power consumption, output resistance, gate oxide.

**1. Introduction:**

The National Technology Roadmap of semiconductor (NTRS) and ITRS having scaling prediction from 100 components per IC in 1965 to 15 billion in the current state. There are less gain in device performance i.e. power Consumption, short channel effects and parasitic capacitance as scaling goes further below sub-100 nm. In 2007, the use of high-\( k \) dielectrics [6] is first time introduced, to show gate leakage issues.

High \( K \) dielectric devices have applications in low power dissipation, low leakage current and high performance over conventional MOS. Basic difference in structure of conventional MOS over high \( k \) dielectric device is gate material. The materials used for the conventional MOS is SiO\(_2\) but in high \( k \) dielectric based device gate material can be HFO\(_2\), Al\(_2\)O\(_3\), Y\(_2\)O\(_3\), La\(_2\)O\(_3\), Sc\(_2\)O\(_3\) [7]. For further downward scaling, dielectric having a higher dielectric constant will be the solution for achieving the same transistor performance while maintaining a relatively thick physical thickness [6].

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**Table 1** Electrical properties of high \( k \) material [5-6].

<table>
<thead>
<tr>
<th>Gate dielectric Material</th>
<th>Dielectric constant ( (k) )</th>
<th>Energy band gap Eg ( (eV) )</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO(_2)</td>
<td>3.9</td>
<td>9</td>
<td>Passivation</td>
</tr>
<tr>
<td>Al(_2)O(_3)</td>
<td>8</td>
<td>8.8</td>
<td>High channel mobility</td>
</tr>
<tr>
<td>TiO(_2)</td>
<td>80</td>
<td>3.5</td>
<td>Low leakage current up to 1 nA/ cm(^2)</td>
</tr>
<tr>
<td>ZrO(_2)</td>
<td>25</td>
<td>5.8</td>
<td>high-permittivity</td>
</tr>
<tr>
<td>Hfo(_2)</td>
<td>35</td>
<td>5.7</td>
<td>Higher Breakdown voltage</td>
</tr>
<tr>
<td>Ta(_2)O(_5)</td>
<td>25</td>
<td>6</td>
<td>high durability and stability to heat</td>
</tr>
<tr>
<td>Y(_2)O(_3)</td>
<td>13</td>
<td>6</td>
<td>effective mobility</td>
</tr>
</tbody>
</table>

As from above table, it can be seen that Hfo\(_2\) is having higher dielectric constant value and it is widely used material for the simulation of MOS device. In the below figure the schematic of high \( k \) dielectric based gate oxide is shown.
The used of high k-dielectric based material providing improvement in the performance of the device. Among the three main terminals of the MOS transistor – gate stack (Scaling of the gate stack is a key to enhancing the performance of complementary metal-oxide-semiconductor (CMOS), field-effect transistors (FETs) of past technology generations). Source/drain, and channel length; gate stack is most sophisticated and sensitive part for performance, yield and reliability [1]. Many alternate of high-k gate dielectrics have been studied to replace SiO₂. Among them, Hf-based oxides has been recently highlighted as the most suitable dielectric materials because of its comprehensive performance.

2. Evolution & Device Development:

1. The industry has employed oxy-nitride gate dielectrics since the 1990s, but in conventional silicon oxide dielectric is infused with the help of small amount of nitrogen. [2].

2. In early 2007, Intel has announced the deployment of hafnium-based high-k dielectrics with a metallic gate for components worked one the technology of 45 nanometer and has been used it in the 2007 processor series. [5]

3. In 2007, IBM also announced the transition to high-k materials, also hafnium-based, for some products in 2008.

4. NEC Electronics has also announced the use of an HfSiON dielectric in their 55 nm.

5. The 2006 ITRS roadmap predicted that the implementation of high-k materials to be commonplace in the industry by 2010 [6].

3. Modeling and Simulation of HfO₂ based MOSFET:

Fabrication process flow is:

1. Define silicon substrate.

2. Deposition of high k dielectric HfO₂ in gate.

3. Partially etch out the high k material (HfO₂).

4. Formation of drain and source using ion implantation having phosphorous impurity.

5. Deposition of electrodes using aluminum material.

6. Deposition of tungsten material on HfO₂ layer for the formation of gate.

7. Deposition of low resistance material (aluminum) on the tungsten layer.

Step: 1 For <100> boron is used to doped silicon wafer, choose ADD region from Region menu and from right side window click on silicon material and select set base impurity.
Step: 2 HFO₂ is thermally grown from the region menu, then from the Right window select material HFO₂.

Step: 3 HFO₂ is etched out first and etching of silicon substrate, for this chooses the region which will etch out and click on apply button.

Step: 4 Drain and source is created using phosphorus impurity.

Step: 5 Aluminum materials are used for the formation of electrodes.

Step: 6 Gate is placed on the high k material using tungsten material.
Step: 7 High k devices are ready by applying the low resistance metal layer on the gate.

**Fig.7 High k-dielectric based device.**

IV. Software details:

Dr. Ivan Pasic founded Silvaco in 1984. Silvaco is an interactive tool. It has different parts such as Deck build, Tony plot, Maskview. Silvaco is used to provide analog semiconductor process, device and design automation solutions in CMOS. Among these interactive tools, Devedit is a tool of silvaco which is used for simulation of device, it will be used to either create a device by remesh or edit an existing device. It helps to create standard silvaco structure which can be easily integrated into 2D or 3D simulators of silvaco tool.

V. Conclusion:

When decreasing size of MOS technology it required the replacement of the SiO$_2$ with gate dielectrics material that have a high dielectric constant value (high-k). When the thickness of SiO$_2$ is decreased below 1.4 nm then electron tunneling effects and high leakage currents will occur which causes a serious obstacles for device reliability. Therefore, MOSFET structure with high k dielectric is useful to improve electrical performance of the design.

VI. References:


