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Modified Low Power Single Bit-line Static Random-Access Memory Cell Architecture

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Abstract - *The most disquieting disputes related to our electronics industry are speed and power. SRAM modules promise speedier data access than DRAMs and SRAMs own the ability to work without episodic refreshing of memory module. Since SRAM is one of the exceptional circuits in low power VLSI industry, study about SRAM is relevant in our day today life. The divergent variety of SRAM architectures are put forward by many researchers around the world, all are not proven efficient in case of power and stability. Out of various logics, SRAM with adiabatically operated word line consumes less power and is more stable compared to others. A modified SRAM architecture with low power consumption than the existing is proposed in this paper.*

Key Words: Adiabatic logic, MLV circuits, 6T SRAM cell, Single bit-line SRAM, Flash RAMs

1. INTRODUCTION

A reliable device consumes less power. The researchers possess an urge to develop more less power consuming devices in VLSI technology. Thus far CMOS devices are famous for low power consumption. For minimizing the power consumption of a circuit board or a memory system, CMOS devices may use less power than equivalent devices from other technologies those it may not help thus much. Low power design has become an important issue in VLSI design now a day, especially for high speed systems that we use in day today life. Generally dynamic power consumption leads more the power dissipation in most digital systems. Dynamic power dissipation usually depends upon the switching frequency, the output voltage swing and the supply voltage. Reduction in the supply voltage is more effective to decrease dynamic power dissipation. But lowering supply voltage affects badly the performance dramatically. Lowering the supply voltage also decreases the threshold voltage which will increase the sub-threshold current or leakage current and the static power dissipation increases as a result. Controlling the output voltage swing is an another way to reduce dynamic power and delay efficiently. Various approaches can be implemented for reducing the voltage swing during the read and write switching activities during SRAM operation. Charge Sharing Technique is one of them which is proven efficient. In this method, the charge sharing means to reduce the bit line voltage during the operation. Another technique known as half swing pulse mode technique [3] is also proposed to reduce the dynamic power. Another scheme as, hierarchically distributed bit-line tactic, during switching activity is proven in effect for dropping the active power in SRAMs by reducing the value of bit-line capacitance. Multiple valued techniques (MLV) [5] is also proven as a very hopeful and useful method for reducing the voltage swing of the output. MLV circuits are designed with both voltage mode and current mode. The memory array plays an imperative role in various circuits such as the system-on-chips (SoCs), microprocessors and microcontrollers and the overall memory system also consumes a major chip area. These memory elements consume almost 60% of the total power of the IC. When the number of transistors increases from thousands to millions, the leakage power also increases dramatically. This becomes an important challenge to be tackled during the designing of an SRAM cell structure. There are several techniques discussed in the literature for reducing power dissipation in memory systems. One of the such effective technique is to reduce the supply voltage of the circuit and however, this technique is not so efficient, due to the fact that the reduction in the source voltage leads to degradation in the performance of the SRAM. Reducing the device (transistor) size also helps in the reduction of power consumption. In addition to the above methods, one more efficient way in reducing power dissipation is the use of adiabatic logic technique. Adiabatic control of word line voltage helps in improving the read noise margin of SRAM cell, which determines the stability of the SRAM cell. Static random-access memory is one of the noteworthy circuits engaged in low power VLSI. A modified single bit line SRAM cell using adiabatically operated word line is described in this paper. Talking about the design, single bit line SRAM cells are more stable than dual bit line SRAM cells. Since adiabatic logic circuits consumes less power, conserves energy and reutilizes the charge from circuit nodes, SRAM cell employed with this logic seems more stable and less energy consuming. Microwind and Dsch are used to simulate the above architectures in this paper.

2. EXISTING SINGLE BIT-LINE SRAM CELL WITH ADIABATICALLY OPERATED WORD LINE

In any SRAM cell, after the write operation is completed, the node voltages should be maintained for efficient read operation to be carried out on the cell. For a 6T SRAM [2, 4] the voltage at node1 decreases because of the flow of the leakage current through the transistor nmos1, when the

voltage at the node1 goes low, transistor pmos2 turns on. This affects the voltage at node2, since the pmos2 is turned on, and there happens to be a direct path creation between the source and node2. Due to the reasons it is always possible that the node voltage may change after the write operation. This problem can be solved if we have better control over the leakage paths through which the transistor leakage current flows to reduce power consumption. Fig -1, shows the SRAM cell structure. In this configuration of the SRAM cell, 10 transistors are used. Transistors nmos1, nmos2, nmos3, nmos4, pmos1 and pmos2 are used for write operation and transistors nmos4, nmos5, nmos6 and nmos7 are used for read operation. In this cell structure, only one bit-line [6] is used for the read operation and so the bit-line capacitance is reduced. While the read operation, the transistors nmos7 and nmos8 are turned on. In the 6T SRAM cell, there is a possibility that the pre-charge voltage of bit-line gets discharged. However, because of the presence of the transistor nmos5 in the proposed SRAM cell discharging of bit-line voltage does not happen and the enhanced difference in voltage between the bit-line and the bit complement line are realized. This small difference is sensed and amplified using the sense amplifier. Then it can be taken into consideration that this SRAM cell can provide better performance in terms of read noise margin, and stability characteristics even as compared to the orthodox 6T SRAM cell structure.

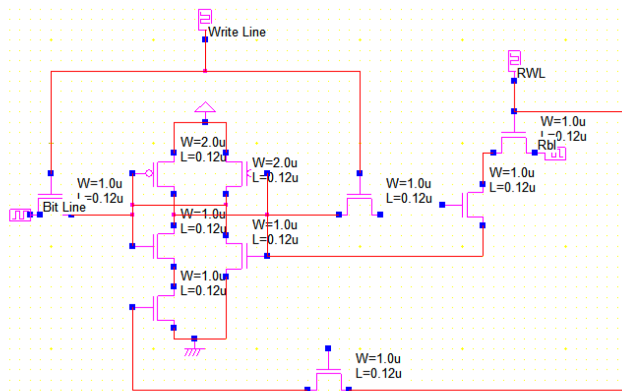

Fig -1: Single bit-line SRAM cell with adiabatically operated word line

Generally, most of the quasi-adiabatic circuits [1] use a four-phase power clock as demonstrated in Fig -2. As shown in Fig -2, the power clock progress from 0V to V_{DD} during the evaluation phase (E).and the power clock returns to 0 during the recovery phase (R) and during the hold (H) phase, the signal in the output nodes are held, so that the output of the present stage is measured as the input to the next stage in the adiabatic pipeline. This is made possible by having the power clock lag behind the input adiabatic signal by one quadrant so as to consume less power to make it more conservation of energy.

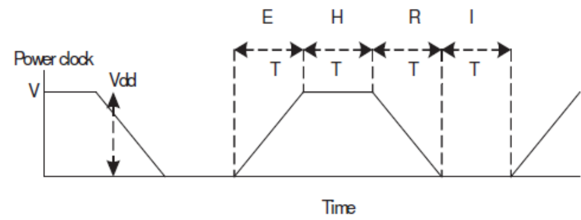

Fig -2: Adiabatic power clock

3. MODIFIED LOW POWER SINGLE BIT LINE SRAM CELL WITH ADIABATICALLY OPERATED WORD LINE

In this work, we propose a modified SRAM architecture which consumes less power than the present adiabatic SRAM with minimum modification. The proposed structure is shown below in Fig -3 and the transistor nmos6 from the existing structure Fig -1 is eliminated to reduce power consumption. The elimination of the above-mentioned transistor does not affect too much of the efficient working of the SRAM cell and the leading power consumption is a great compliment achieved by this elimination.

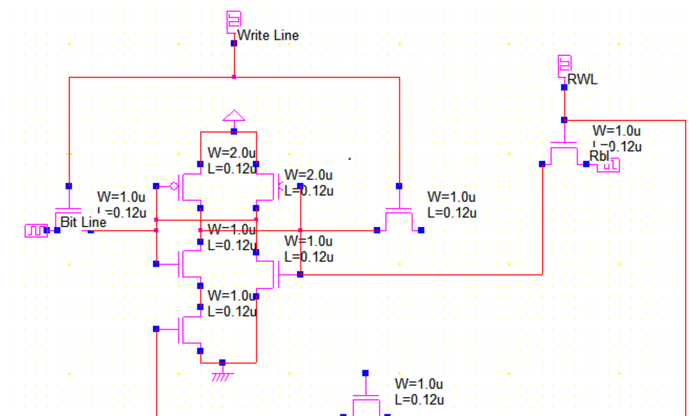

Fig -3: Modified low power single bit-line SRAM cell with adiabatically operated word line

The power consumed by the single bit line SRAM cell in Figure 3.3.A is 0.498mW and the proposed SRAM cell structure in Figure 4.1.A consumes a power of 0.350mW. That means a reduction in 0.148mW power is observed. The stability and the SNM are not affected too much by the change and that lead us to a conclusion that the modified SRAM architecture can be used for the same applications those are used for single bit line SRAM with adiabatically operated word line. And the reduction in power consumption is a great achievement that we could save some more energy than with the adiabatic logic. Maximum I_{dd} current, threshold voltage for low leakage, high speed and high voltage applications stay same for both architectures by using parametric analysis and MOS characteristics analysis, we can find out the values of the above-mentioned

parameters and check it, the values are compare to the existing adiabatic SRAM cell architecture for the verification.

4. SIMULATION RESULTS

The Microwind 3.8 is used to implement and simulate the single bit line SRAM cell with adiabatically operated word line and the power consumption obtained value is 0.498 micro Watts. The waveforms observed are pasted below in Fig -4.

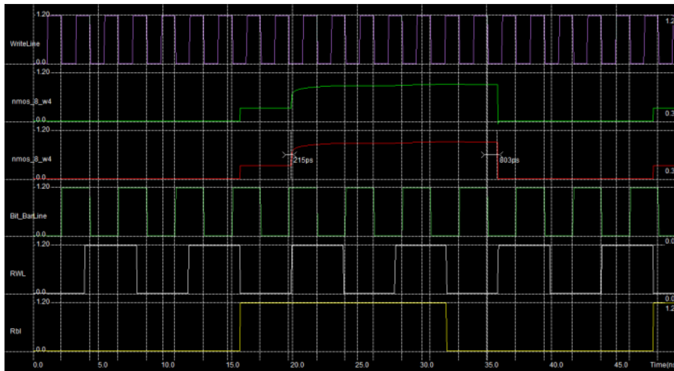

Fig -4: Simulation results of single bit-line SRAM cell with adiabatically operated word line

The proposed system has to be simulated so that to prove the power consumption is reduced from the existing system. The power consumed by the proposed SRAM cell structure is 0.350 micro Watts and a reduction of 0.148 micro Watts power is observed. Refer Fig -5 for simulation results.

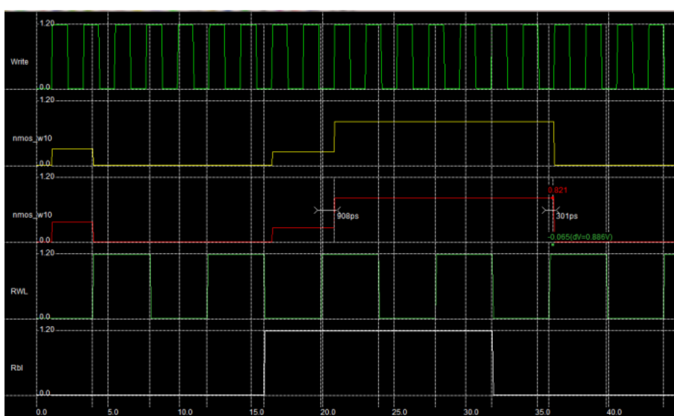

Fig -5: Simulation results of modified low power single bit-line SRAM cell

5. CONCLUSIONS

The power consumed by the proposed SRAM cell structure is 0.350 micro Watts and a reduction of 0.148 micro Watts power is observed. From the parametric analysis, for a supply voltage rise of 0 V to 2V, the maximum I_{dd} current for both the existing single bit line SRAM cell with adiabatically operated word line and the proposed low power SRAM cell, the value can be plotted below 2mA. They both possess same MOS characteristics analysis parameters for low leakage (for V_b = 1V, the value of V_t = 6.5V), high speed (for V_b = 1V, V_t = 5.5V) and high voltage (for V_b = 1V, V_t = 9.5V). Elimination of a transistor also offers 5-8% overall area reduction.

As electronics designers cram more and more components onto each chip, current technologies for erecting random-access memory (RAM) are surfacing day by day. European researchers possess a great place in a new technology known as resistive RAM (RRAM) that may be soon replacing flash RAM in USB drives and other portable gadgets. The Semiconductor Road Map possess a lot of technologies, but even though the researches are like in a state of near end of road. Future electronics may be in need of memory chips that are smaller, faster and cheaper than those of existing today. In this category, low power memory chips will be most needed so that to save energy and to save nature from power dissipated problems. If we could save a somewhat energy by any means through our work, it will be a good achievement to the electronics industry.

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