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Calibration Techniques for Pipelined ADCs

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Abstract - Development and design of advanced pipelined ADC has increasing scope in recent times. This is due to the fact that circuitry is able to get smaller and smaller with rise and betterment of fabrication of nano circuitry which has a comparatively smaller footprint. This means in order to achieve this we need high performance pipelined ADCs that are able to rectify analog non – idealities with respect to digital calibration circuits.

Digital calibration is a better option rather than changing the analog circuitry in the deep submicron processes. In deep sun-micron, a large field across a thin oxide causes a trap generation randomly distributed in the oxide layer which leads to the stress induced oxide or gate leakage and leads to degradation of the MOSFET performance. Discussion on some of the techniques of advanced pipelining of ADCs have been done in this paper. Technology scaling at a constant rate has caused supply voltages to decrease in size and circuitry to work at higher speeds. A closer view on SNDR, SFDR, DNL and INL of pipelined ADCs with different calibration techniques is made in this paper. A comparison is made with intention of getting a perspective towards speed, power, and efficiency improvement and function of ADCs.

Key Words: **pipelined ADCs, calibration techniques, SFDR, SNDR, INL, DNL**

I. INTRODUCTION

There a variety of applications of pipelined ADCs. A few key ones to name are video imaging systems, military, HDTV cameras, cellular base stations. The pipelined ADCs have multistage architecture and hence deal with solutions for low power, high resolution, high speed, and chip area. Various power reduction techniques can be used for low resolutions of 8-10 bits [1-3]. Speed of ADCs achieving beyond 100MS/s with resolution beyond 12 bits is difficult to achieve without the calibration techniques. Hardware complexity increases with increase in the resolution of the ADC. Various errors like op-amp non-linearity, capacitor sizing error, and op-amp finite gain errors may be incurred due to switched capacitor circuits used in MDAC of pipelined ADCs.

There is difficulty in fabrication of amplifiers with high gain due to the scaling down in the CMOS technologies. Degradation in performance of the ADC occurs due to capacitor sizing issues. Many techniques are available to minimize these errors [4-10]. These techniques have their own advantages, disadvantages and limitations. A comparison of these techniques for digital calibration isnt available in literature till date.

Analysis and comparison of different digital calibration techniques along with their advantages that have been developed and used in different applications is the objective of this paper. Detailed discussion on some important calibration techniques like nested background calibration, least mean square method, SPLIT, variable amplitude dithering, two-way interleaved interpolation based non-linear calibration, inter-stage scaling is done in this paper. There are five sections in this paper. Section II outlines pipelined ADCs with different. Section III lays emphasis on different categories of calibration techniques. Section IV is discussion on available techniques for digital calibration for pipelined ADCs and their comparative analysis.

1.1 Sub Heading 1

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II. PIPELINED ADC ARCHITECTURE AND DIFFERENT ERRORS

n number of individual ADCs are cascaded in pipelined ADCs [11-18]. The building blocks of each stage are sample and hold (S/H) circuit, Sub-DAC (Digital to Analog Converter), Sub-ADC (Analog to Digital converter), analog subtractor and gain amplifier [16-17]. The switched capacitor circuits in CMOS technology implements the transfer function ($V_{res}=2V_{in}-V_{adc}$) of a pipelined ADC and figure 1 shows the block diagram of one stage of a pipelined ADC.

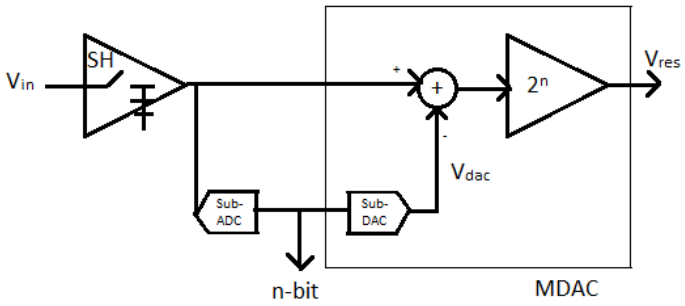

Figure 1: Block diagram of pipelined ADC stage

Correction Logic:

At clock cycle, the sample and hold block samples the input voltage (V_{in}) and holds the sampled value, to produce a low-resolution digital output. A new output voltage is produced known as the residue of that stage which is produced by subtraction of the DAC converted analog voltage and the input voltage. Literature of a 10-bit pipelined ADC which includes 1.5 bit/stage as a single stage architecture is widely available. Immunity of the stage to the comparator offset within $\pm\frac{V_{ref}}{4}$ is one of the advantages a 1.5 bit/stage architecture offers where V_{ref} is the reference voltage of the ADC. This is achieved by the use of Digital Error Correction Logic (DECL), consisting of adders as shown in figure 2 [16-17].

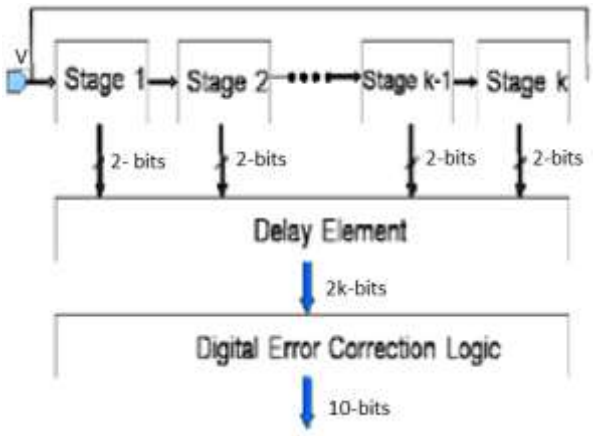

Figure 2: Digital Error Correction Logic

Delay units are used to synchronize the digital outputs of different stages in each stage. For a 10-bit pipelined ADC, there will be a latency of 10 clock pulses [16-17].

Different errors:

Multiplication of the DAC is the cause of different errors:

- Capacitor mismatch error
- Comparator offset
- Finite DC gain of the op-Amp

Comparator offset:

An internal offset voltage may add to the difference produced by the comparator voltage. Wrong output is produced as the output of the comparator propagates through the other stages. Figure 3 shows the comparator offset error on the residue and

ADC output as a function of input voltage. The dotted line shows the desired output and solid line shows the actual output [16-17].

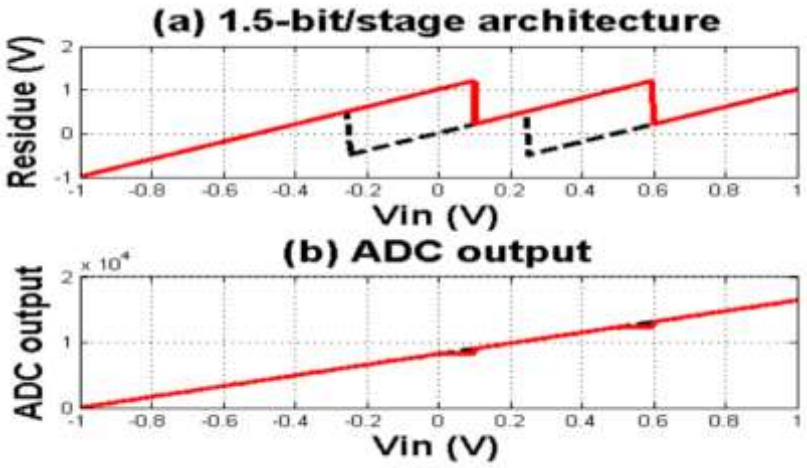

Figure 3: Comparator offset error

Capacitor mismatch error:

The gain of the Switched capacitor MDAC is decided by the capacitor ratio C_s/C_f. The output may change with change in the values of C_s and C_f. An accurate capacitor matching is required for a better resolution pipelined ADC. Capacitor mismatch may be caused due to the fabrication issues, over-etching and oxide thickness gradient. The effect of the capacitor mismatch error on the residue and ADC output as shown in figure 4.

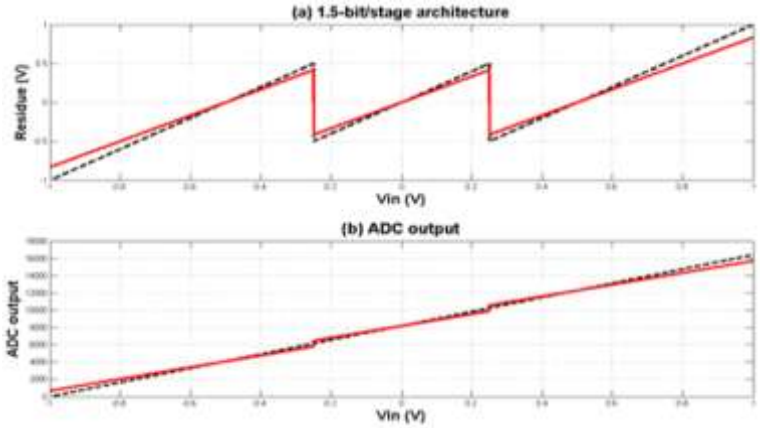

Figure 4: Capacitor mismatch error

The dotted line is graph of an ideal transfer function and the solid red line is the output with the capacitor mismatch error [16-17].

Op-Amps finite open loop gain:

Since an op-amp plays an important role in switched capacitor circuit [6] it is essential to show the effects of non-idealities of op-amps. Figure 5 shows a switched capacitor implementation.

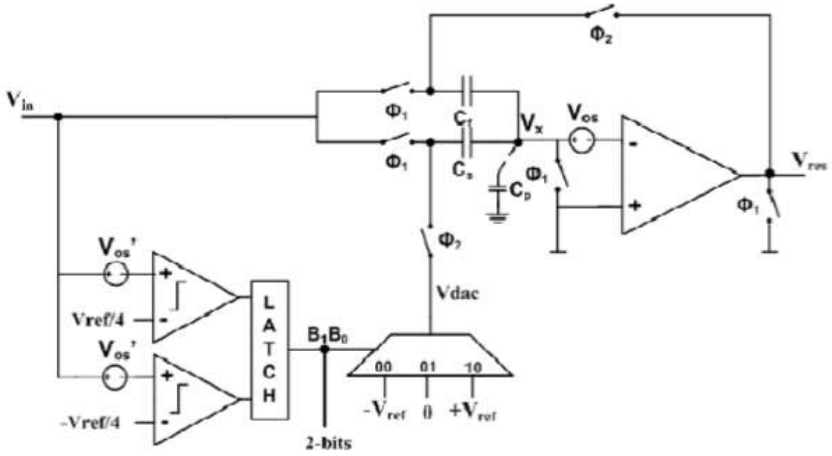

Figure 5: 1.5-bit per stage SC implementation

C_P is the input parasitic capacitance and A is the open loop DC gain of the op-amp.

Motivation: less than 11 bits resolution can be achieved by the non-calibrated pipeline ADCs and the calibrated ones can improve this to more than 14 bits. The motivation of calibration is to improve bot the static and the dynamic behavior of ADCs which include full scale error, offset error, signal to noise and distortion ratio, spurious free dynamic range, effective number of bits, total harmonic distortion, differential non-linearity error, integral non-linearity errors etc. Calibration can correct all these different types of errors. Monitoring of the ADC output, identification of errors and rectification of the output requires additional circuitry. Accuracy, speed and application of the ADC determine the choice of calibration. Foreground and background calibration are two different categories of calibration [5-7].

Factory calibration: Onetime events like capacitor trimming can be rectified easily using the factory calibration. To improve the linearity of the ADC, trimming of the capacitors is done in order to match them and this could happen before packaging the ADC, which is easily achieved by factory calibration.

Foreground calibration: Recalibration is allowed at power up but at the time of calibration the converter is required to be offline. Due to this characteristic of the need for the ADC to be offline at the time of the calibration the operation of the ADC gets disrupted, and hence requires extra clock cycles to inject the calibration signal which results in slow response [12]. But this scheme is non-transparent to all the ADCs.

Continuous calibration: the best feature of this type of calibration is to perform the calibration of the ADC in the background while all the processes are still running and no disruption in the flow of signal to the ADC. Two types of continuous calibration exist: Analog and Digital.

Analog: the extra cycles that are required for calibration, slow response, and increased power dissipation are drawbacks of analog precision techniques. The process isnt transparent to all ADCs. Difficulty in using the analog calibration scheme is apparent as the down scaling continues in process technologies.

Digital: Since the converter remains in the normal mode of operation while calibration occurs it is a popular type of calibration. Digital background calibration is best for deep submicron technologies. It provides robustness and economy for the high performance and complex processing. Modifications are easier to implement as they are in the digital domain. Accuracy and speed of pipelined ADCs is relaxed using the digital calibration techniques. Few techniques introduced are: Least mean square method, variable amplitude dithering, split method etc.

III Comparison of calibration techniques

1. **Nested background calibration:** It is very difficult to achieve both speed and accuracy together in the ADCs. Low speed ADCs are more accurate than high speed ones. In nested calibration scheme [6], the architecture used for the ADCs is accurate but slow, which is cautiously calibrating an ADC which is fast but inaccurate. The calibration is nested because slow-but-accurate ADC, which has been already calibrated in foreground, is used here as a reference ADC to calibrate inaccurate pipelined ADC. Least mean square governs this type of calibration. Calibrated output generated using digital signal processing unit is shown in figure 6:

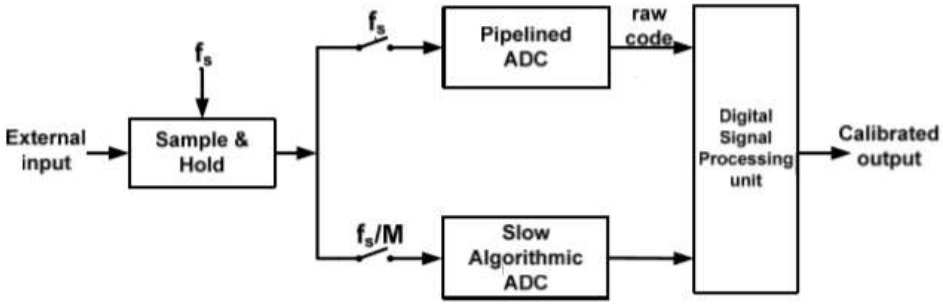

Fig 6: Nested back ground calibration [6]

Both the sample and hold amplifier and the pipelined ADC operate at the same sampling rate of 20MSamples/s. The gain error information, about the pipelined ADC, saves in the form of raw code and it have to be taken out in the digital error estimation block (DEE). The uncalibrated output is combined with the DEE block to produce calibrated output. The pipelined and algorithmic outputs are subtracted to obtain the errors. Adders in the DEE block and negative feedback in association is used to reduce the MSE, so the calibrated output lines optimize the output of the slow algorithmic ADC in steady state. High gain op-amps are not required and circuit non idealities because of capacitor mismatch is also removed. Different problems may occur with this calibration scheme such as area overhead. The reference ADC may have a complicated circuit of the type folding interpolating architecture resulting in increased power consumption.

2. **Calibration using Least-Mean Square method:** The new method assumes component errors from conversion results, which uses digital post processing on results to correct those errors by adjusting the analog component values to attain linearity. This scheme resembles the channel equalization problem, which occurs in digital communication system. Here, using a slow but accurate ADC, the code domain adaptive finite impulse response (FIR) filter is used to remove the effect of component errors [7]. This scheme is able to remove errors like op-amp offset error, capacitor mismatch; sampling switch induced offset and finite op-amp gain, which is not dependent on signal. The block diagram utilizing this algorithm, running in the background, which is digital, fully adaptive and data driven is shown in figure 7.

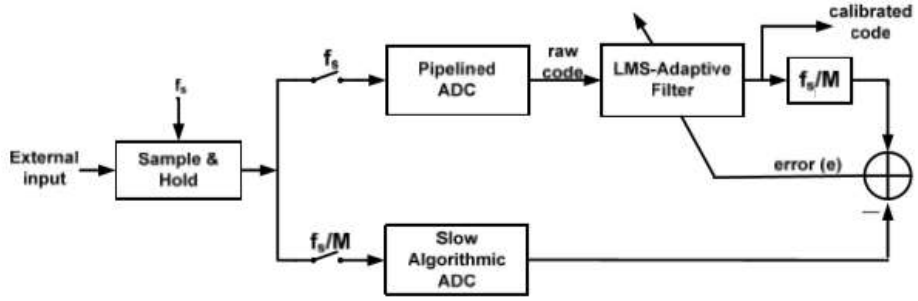

Fig 7: code-domain LMS adaptive LE as digital correction system

The benefit of this scheme is relaxing from the requirement of precision of analog components and is able to continue CMOS device scaling approach [8]. FIR filter removes all the component errors from all the stages. This is able to correct errors caused by finite op-amp gain, capacitor mismatch, various input-referred offsets etc. The analog signal path is intact completely to maintain conversion speed as maximum permitted by device technology used for designing purpose. A Pipelined ADC has been implemented in 0.35-μm double-poly triple-metal CMOS process [21]. Also, it is able to achieve 14-b accuracy without calibration or dithering but it is required to work at high input voltage and it dissipates large power. A combination of techniques is used to improve accuracy, such as amplifiers with gain boosting, domain extended digital error corrections, communicated feedback capacitor switching (CFCS) and low noise dynamic comparators [22]. Also, front-end stage uses a sample and hold amplifier (SHA) – less front-end stage.

3. **Calibration using SPLIT:** In this technique, a single ADC is split into two ADC, where individual converter is converting the same input signal. Two outputs from two ADCs is averaged to produce calibrated digital signal as shown in Figure 8[9].

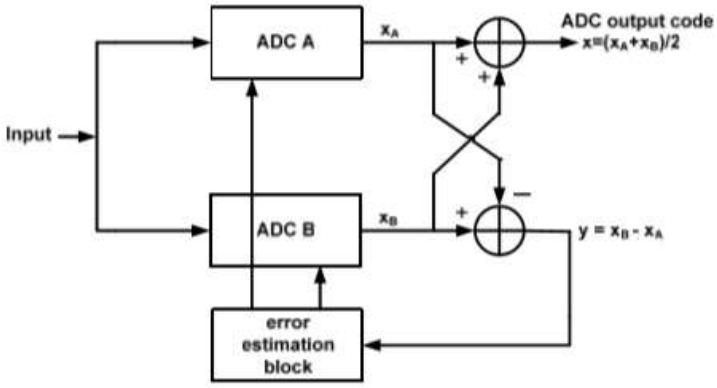

Fig 8: Split based ADC calibration technique [9]

The final ADC output is achieved by averaging the two different outputs from two different ADCs. The difference of outputs of both ADCs is equal to zero with the same input, indicates ADCs are well calibrated. The difference with non-zero value indicates calibration is required and the value decides the amount by which it should be calibrated. As analog circuit broke up into 2, so total analog area remains same. As we know bandwidth is proportional to gm/C, power is proportional to gm and noise is proportional to √kT/C, splitting by two parts and having capacitance of C/2 by each half, bandwidth remains same and so power. The overall noise remains unchanged as the results are getting by averaging of two [9]. For a 10-bit, 1 MS/s algorithmic ADC, Self-calibration is used with around 10000 conversions. By using the concept of split ADC, the analog area of single ADC essentially splits into two, so it makes insignificant effect on analog complexity when consider its power, overall area, noise performance and bandwidth [23]. But the concept of split ADC only, is not enough for the estimation of errors. For example, if both A and B sides have the same error and comparators outputs also same, it would be unable to rectify the error [15]. But this problem could be rectified if we force the two sides to take different decisions and it can be realized by multiple residue mode cyclic amplifier [9]. This amplifier will be the combination of dual residue approach and the 1.5 bit/stage amplifier. Which comparator output will be used for digital output has been decided by 2-bit path address? The best possible residue among four residue modes, this technique helps for digital output selection without interacting the analog circuit. But it requires an additional comparator. It will impact minimal on overall area and power. Due to multiple residue mode, a wide variety of decision paths are available, so it is easy to extract the calibration information even for a DC input.

4. **Calibration using variable amplitude dithering:** The pseudo-random noise dither (PN dither) method is majorly used for digital calibration, to measure domain-extended Pipelined ADC gain errors. By using redundancy bits, the digital error correction technique has been applied to rectify the comparator offset error. But there are some disadvantages with these two techniques like decrease in amplitude of the transmitting, slow convergence speed and deduction of the redundancy space [2427]. To overcome these disadvantages, instead of using the pseudorandom noise dither, the variable-amplitude dithering has been used for a digital calibration algorithm for domain-extended pipelined ADCs [10]. This circuit works well even in worst conditions like the signal stays at high level all the time. The redundancy space plus the total amplitude of the signal and the dither has been restricted by the quantify range. Both static and dynamic performances have improved after the calibration with much higher convergence speed without any circuit complexity. The amplitude of the dither varies with the signal level. Because the amplitude of the dither can be increased without any loss of the amplitude of the signal, the convergence speed remains high. Further over, in the domain-extended architecture, due to the existence of more redundancy space it allows the comparator offsets to be corrected that is within a certain range.

   In this case the values of the threshold voltages have changed to $\pm\frac{3}{4}Vref, \pm\frac{1}{4}Vref$ where the input range is from $\frac{5}{4}Vref\ to \frac{5}{4}Vref$ which is same as the output range. The value of Vref is usually half that of the supply voltage Vdd. In variable amplitude dithering three more components and a capacitor is added in which the capacitor is split into 4 parts with each part having a value of $\frac{Cf}{4}$. Switches have been used to control the dither injections which depends on output of the encoder and the PN value. The amplitude of the dithers varies from $-\frac{3}{4}Vref\ to -\frac{1}{4}Vref$ in all sub levels of the main level.

Table 1: Amplitude of the dithers

V_{in}		Amplitude of dithers	
Main level	**Sub-levels**	**PN=-1**	**PN=1**
$-\frac{3}{4}V_{ref}\sim-\frac{1}{4}V_{ref}$	$-\frac{3}{4}V_{ref}\sim-\frac{5}{4}V_{ref}$	$\frac{5}{4}V_{ref}$	$-\frac{1}{2}V_{ref}$
	$-\frac{5}{8}V_{ref}\sim-\frac{1}{2}V_{ref}$	V_{ref}	$-\frac{3}{4}V_{ref}$
	$-\frac{1}{2}V_{ref}\sim-\frac{3}{8}V_{ref}$	$\frac{3}{4}V_{ref}$	$-V_{ref}$
	$-\frac{3}{8}V_{ref}\sim-\frac{1}{4}V_{ref}$	$\frac{1}{2}V_{ref}$	$-\frac{5}{4}V_{ref}$

5) Equalization based digital calibration

Generally, the calibration signals are normally used to measure using the above technique. While considering the deep submicron technologies the precision of the signals is very important. Various techniques are available [32-34]. Certain errors like amplifier non-linearity, capacitors mismatch and the residue gain error are measured in advance and corrected later using the technique of equalization based digital calibration. This method can be used either by calibrating foreground or background. having four ground estimation into consideration, the error estimation has done with non-pressure precision calibration signals and to convert it to background scheme, and adaptive linear prediction structure has been used. For estimating the error coefficients which had no requirement for higher accuracy signals for calibration, LMS algorithm has been used and CNFA MDAC topology has been used to design the 1.5 bit/stage pipelined ADC [11]. The calibration works recessively in opposite direction by pipelined stages as shown in figure 9.

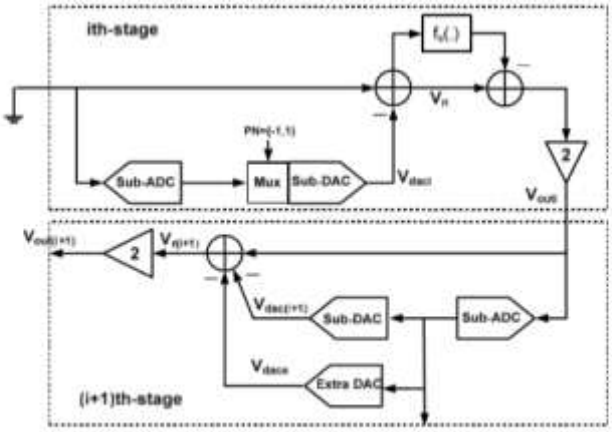

Fig 9: Calibration of ith stage implemented in CNFA MDAC structure [11].

This technique does not require any accurate calibration signal. The adaptive LMS algorithm has been used to approximate the errors.

(6) Inter-stage scaling for low power pipelined ADC

Using deep submicron technology, pipelined ADC implementation has been done. Consists of a sample and hold circuits (S/H), 8 cascading 1.5-bit stage and 2-bit flash ADC in [12]. To correct the offset of comparator, a block of current generator, non-overlapping dock, reference generator and digital error logic (DEL) is required as shown in figure 10.

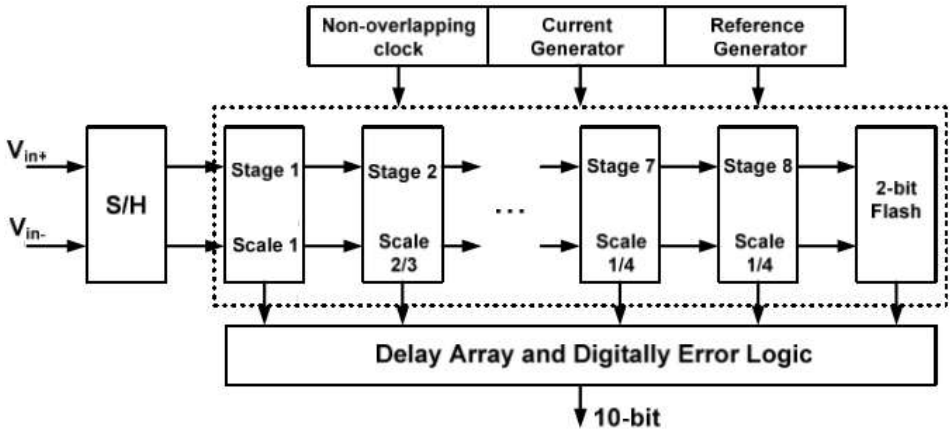

Fig 10: Block diagram of Pipelined ADC [12]

To minimize the distortion, the switch in SHA is bootstrapped. Sub-ADC has switched -capacitor comparator. MDAC uses 2X game in each stage. Design of the first stage involves specific considerations to noise, distortion and incomplete settling. High bias currents and high sampling capacitors are used. The second stage in was a downscaling factor of 2/3 and 1/4 for the further stages. To achieve a sampling rate of 50 megahertz with 1.6 pf load to minimize the settling time coma specifically designed OTA is used scale factor is 2/3 in the stage 2, C1 [sampling capacitor]and C2 [feedback capacitor] can be reduced to about 2/3 when compared with C1 and C2 in stage 1. In [28], the multi-bit architecture having an op-amp count of 3 for the complete ADC is used. By using the same unary cell implementation, an inter-stage scaling has been applied effectively to all the stages of pipelined ADC. The cell has been used multiple times at higher stages. The power and area consumption decrease with no compromise in performance of the pipeline stages. There are limitations faced with this calibration scheme like the sampling frequency cannot go high as required in some applications. In [29], the implementation of 1.5-b/stage. Pipelined ADC core using an amplifier sharing technique, the capacitor matching layout and swing-improved telescopic OTA is shown. To satisfy the special condition of working at high input voltage and least power dissipation with excellent static and dynamic performance, the Analog to Digital converter has been designed.

(7) Two-way time-interleaved Pipelined ADC occupying less Area:

With this adaptive power/ground architecture eradicates the headroom boundaries due to low power requirement. While considering the signal swing, this technique gives a flat transition between the MDAC stages and the last flash stage. A single-stage amplifier structure has been used in the SHA and MDACs to attain good phase margin, wide bandwidth and low noise is chosen. A telescopic cascade structure has been used to achieve high amplifier gain to get 12-bit linearity. To improve the bandwidth, all input devices are implemented with thin gate device only of a gain-boosting circuit. For CMOS Switch, in the amplifier design, a 2.5V supply is used. The disadvantage of thick-oxide devices is to make it slow and normally thin-oxide devices are more reliable in terms of fast transition, low on-resistance and very less power consumption. A 6-level Flash ADC is used to generate a 2.5-bit digital output in each MDAC and the final residue is digitized by a 6-bit Flash ADC. In [30], to generate the extra reference voltage taps, a reference voltage extrapolation method is used here. From the inner taps of the reference ladder, three-input dummy pre-amplifiers at the edges generate the over ranging voltages by analog addition. In both 6-bit Flash ADC and the 2.5-bit Flash ADCs, MDACs and the folded preamplifiers are used. In [31], an 11-bit time-interleaved ADC with 800MS/S has been implemented for a 10GBase-T application in a 90nm CMOS process. To achieve high resolution and conversion rate, a single open-loop T/H circuit using a cascade source follower has been used.

Interpolation based non - linear calibration: In high resolution pipelined ADCs, the utmost requirement is high gain OP-AMP and large capacitors. But these are the main cause of large ADC power. The linearity of ADC is also limited by the finite operational amplifier (OPAMP) gain and capacitor mismatch in MDAC. In [14], interpolation based digital self-calibration architecture for pipelined ADC has been introduced. The 0.78 pJ/step figure-of-merit (FOM) is low for designs in 0.35 µm CMOS processes. Here a precise Cal ADC is used to measure the MDAC error and it runs in two modes as calibration mode and recovery mode.

Calibration Mode: It enables Cal ADC to measure any internal node in the pipeline, so that MDAC transfer function can be measured directly. A set of input voltages is supplied to the pipeline ADC. Cal ADC switches are used to measure the MDAC transfer function. Switches will turn on successively, while complimentary switches turn off at the same time. Every time, every MDAC on which calibration is going on, a sample on its transfer function is recorded every time ($X_{j,i}$,$Y_{j,i}$), where $X_{j,i}$ is the input voltage of the i-th sample and $Y_{j,i}$ is the output voltage of the i-th sample.

Recovery Mode: In this mode, all switches go off and Cal ADC is held away from the pipelined ADC. The 14-bit raw codes are digitized from input signal by pipeline ADC, converted into 12-bit code by a digital decoder. In this design, the pipeline is to generate 13-bit raw data and the extra 1-bit is for design redundancy. From the end of the pipeline, the recovery process is started and moves in order to the front in this process, MDAC input voltage is calculated using the residue voltage and its quantization code. At the end of the pipeline, for MDACs, there is no requirement of calibration, as they considered linear. As this architecture is not using backend ADC to measure MDACs, it is free from the measurement error, which results in more accurate calibration. Because of the slow settling of the first pipeline stage, SNDR of the calibrated ADC drips to 8 dB at the Nyquist frequency. Also, the power consumption is high. Table 2 shows, all the performance parameters of different calibration techniques, which are most popular for Pipelined ADCs.

Table 2: Comparison of the performance of Pipelined ADCs having different calibration techniques

Reference No.	Resolution (bit)	VDD (V)	Area used (mm2)	Technology used	THD (dB)	Sampling freq	SNDR (dB)	SFDR(dB)	INL(LSB)	DNL(LSB)	Power diss.(mw)
[6]	12	3.3	7.5	0.35 µm 2P4M	–92.9	20 MS/s	70.8	93.3	0.47 (max)	0.41(max)	254
[8]	12	3	7.9	0.35 µm	76(1 mHz) 74(40 MHz)	75 MS/s	-	80(1 MHz) 76 (40 MHz)	-0.9,+0.6	-0.5,+0.5	290
[9]	16	2.5	1.16 mmX 1.38 mm	0.25 µm 1P4M		1 MS/s	-	-	+2.1/-4.8	+0.66/-0.47	105
[10]	12	-	-	-	86.2	100 MS/s	87.7	-	-0.5~0.4	-0.4~0.5	V. high
[11]	12	-	-	90 nm	-	100 MS/s	68	83	2.2	0.9	48
[12]	10	2.5	0.6	0.3µm	-	50 MHz	-	68	-0.63/+0.63	-0.27/+0.21	50
[13]	12	2.5	0.4	40 nm		3GS/s	58	-	+03/-03	+0.5/-0.5	500
[14]	12	3.3	4.8mmX 4.3 mm	0.35 µm	-79.8	20 MS/s	72.5	84.4	0.2	0.27	56.3
[32]	12	2.5	-	0.25 µm	-	80 MS/s	72.6	84.5	+0.24	+0.09	340
[33]	12	1.2	-	90 nm	-	200 MS/s	62	-	+1.3	+0.59	348
[34]	10	1.2	-	90 nm	-	500 MS/s	56	-	1	0.4	55

IV. CONCLUSION

The requirement of digital calibration techniques in the pipelining of the ADCs in recent times and summary of different advantages and disadvantages that appear during operation are discussed in this paper. Drift towards smaller ADC structures and use of digital circuits for error correction is a favorable model. Control of the requirement of low power dissipation of modern processes and enhancement of resolution and static/dynamic performance of pipelined ADC circuits is achieved by

using digitally assisted ADCs. A general comment can be made saying, some improvements are still awaited to be permutation of features that involve improved system implanting with reduction in analog sub-circuit complexity and a precision system with cheap Digital signal processing resources.

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REFERENCES

[1] A. Panigada and I. Galton, "Digital background correction of harmonic distortion in pipelined ADCs," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 53, no. 9, pp. 1885–1895, Sep. 2006.

[2] A. Gharbiya, T.C. Caldwell, and D.A. Johns, "High speed oversampling analog-to-digital converters," International journal of high-speed Electronics and systems, Vol. 15, No. 2, pp. 297-317, 2005.

[3] N. Sasidhar , Y. Kook , S. Takeuchi , K. Hamashita , K. Takasuka , P. Hanumolu and U. Moon "A 1.8 V 36-mW 11-bit 80 MS/s pipelined ADC using capacitor and opamp sharing", IEEE Asian Solid-State Circuits Conf. 2007, ASSCC\'07, pp.240 -243 2007 .

[4] Wu, P.Y., Cheung, V.S.-L. ; Luong, H.C. "A 1-V 100-MS/s 8-bit CMOS Switched-Opamp Pipelined ADC Using Loading-Free Architecture" IEEE Journal of Solid-State Circuits, Volume 42 , Issue 4, April 2007.

[5] Li, J. ; Un-Ku Moon "Background calibration techniques for multistage pipelined ADCs with digital redundancy" IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Volume:50 , Issue: 9 , Sep 2003

[6] X.Wang,P.J.Hurst, S.H.Lewis, "A 12-bit 20-Msample/s Pipelined Analog-to-Digital Converter with Nested Digital background Calibration", IEEE Journal of Solid-State Circuits, vol.39, No.11, Nov. 2004.

[7] Yun Chiu, Cheong yuen W. Tsang, Borivoje Nikolic and Paul R. Gray, "Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters "IEEE Transactions On Circuits And Systems—I Vol. 51, No. 1, January 2004.

[8] Boris Murmann, Student Member, IEEE, and Bernhard E. Boser, Fellow, "A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification" IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, December 2003.

[9] John McNeill, Michael C. W. Coln and Brian J. Larivee,"Split ADC" Architecture for Deterministic Digital Background Calibration of a 16-bit 1-MS/s ADC "IEEE Journal Of Solid-State Circuits, Vol. 40, No. 12, December 2005

[10] Ting Li and Chao You "A Digital Calibration Algorithm With Variable-Amplitude Dithering For Domain-Extended Pipeline Adcs" International Journal of VLSI design & Communication Systems (VLSICS) Vol.5, No.1, February 2014

[11] BehzadZeinali, TohidMoosazadeh, Mohammad Yavari and Angel Rodriguez-Vazquez, "Equalization-Based Digital Background Calibration Technique for Pipelined ADCs "IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 2, February 2014

[12] Zhzo-Xin Xiong and Min Cai "A 10-Bit 50-Ms/S Low-Power Pipeline ADC For Wimax/Lte" Journal of Theoretical and Applied Information Technology, May 2013. Vol. 51 No.3

[13] Chun-Ying Chen, Jiangfeng Wu, Juo-Jung Hung, Tianwei Li, Wenbo Liu and Wei-Ta Shih "A 12-Bit 3 GS/s Pipeline ADC With 0.4 mm and 500 mW in 40 nm Digital CMOS" IEEE JOURNALOFSOLID-STATECIRCUITS, VOL.47, NO.4, APRIL 2012

[14] JieYuan,Sheung Wai Fung, Kai Yin Chan and Ruoyu Xu "A 12-bit 20 MS/s 56.3 mW Pipelined ADC With Interpolation-Based Nonlinear Calibration" IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 59, No. 3, March 2012

[15] John A. McNeill, "Digital Background-Calibration Algorithm for "Split ADC" Architecture", IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 56, No. 2, February 2009.

[16] SwinaNarula , Sujata Pandey " A Methodology for Behavioral modeling of 10 bit Pipelined ADCs with modified Digital Error Correction Logic" Fifth international Conference on Advanced Computing and Communication Technologies, Jan 2015

[17] SwinaNarula, Sujata Pandey "High Performance 14-Bit Pipelined RSD ADC." inJournal of Semiconductors (IOP Science), Vol. 37, No.3, pp. , 2016.

[18] Moon, Un-Ku. Song, Bang-Sup. "Background digital calibration techniques for pipelined ADCs", IEEE Transactions on Circuits and Systems II- Vol. 44, No. 2, Feb 1997, pp 102.

[19] Gustavsson, M., J. J. Wikner, and N. N. Tan, "CMOS Data Converters for Communications" Kluwer Academic Publishers, 2000.

[20] X. Wang, P. J. Hurst, and S. H. Lewis, "A 12-bit 20-MS/s pipelined ADC with nested digital background calibration," in Proc. IEEE Custom Integrated Circuits Conf., Sept. 2003, pp. 409–412.

[21] W. Yang, D. Kelly, I. Mehr, M. T. Sayuk, and L. Singer, "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," IEEE J. Solid-State Circuits, vol. 36, pp. 1931–1936, Dec. 2001.

[22] Ting Li, Chao You "A 3-V 14-bit 75-MS/s CMOS pipeline analog-to-digital converter with 93.72-dB spurious-free dynamic range" International Journal of Electrical, Electronics and Computer Systems, March 2014.

[23] J. McNeill, M. Coln, and B. Larivee, ""Split-ADC" architecture for deterministic digital background calibration of a 16b 1MS/s ADC," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2005, pp. 276–278.

[24] E. Siragusa and I. Galton, "Gain error correction technique for pipelined analog-to-digital converters," Electron. Letter, vol. 36, pp. 617–618, Mar. 2000.

[25] E. Siragursa and I. Galton, "A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC," IEEE Journal of Solid-State Circuits, vol. 39, no. 12, pp. 2126–2138, Dec. 2004.

[26] A. Panigada, I. Galton. "Digital background correction of harmonic distortion in pipelined ADCs," IEEE Trans. on Circuits and Systems I: Regular Papers, vol. 53, pp. 1885–1895, 2006.

[27] A. Meruva, and B. Jalali, "Digital background calibration of higher order nonlinearities in pipelined ADCs," IEEE International Symposium on Circuits and Systems, pp. 1233–1236, 2007.

[28] P. Bogner, "A 28mW 10b 80MS/s Pipelined ADC in 0.13 μm CMOS", Proc. of the ISCAS 2004 Conf., pp. 17–20, 2004.

[29] Nan Wang, Ping Zhou, "A 10-bit 100-MS/s CMOS IP With Emphasis on layout Matching" , IEEE Asian Conference of Solid-State Circuits, vol. 12, pp.335-358, Nov 2006.

[30] S.Gupta, M.Choi, M.Inerfield, and J.Wang,"A 1GS/s11b time-interleaved ADC in 0.13/spl mu/m CMOS," IEEE ISSCC Dig.Tech.Papers , 2006, pp. 2360–2369

[31] C.-C.Hsu, F.C.Huang, C.Y.Shih, C.C.Huang, Y.H.Lin, C.C.Lee, and B. Razavi, "An 11b 800 MS/s time-interleaved ADC with digital back ground calibration," in IEEE ISSCC Dig. Tech. Papers, 2007, pp. 464–465.

[32] C. R. Grace, P. J. Hurst, and S. H. Lewis, "A 12-bit 80-MSample/s pipelined ADC with bootstrapped digital calibration," IEEE J. Solid State Circuits, vol. 40, no. 5, pp. 1038–1046, May 2005.

[33] B. D. Sahoo and B. Razavi, "A 12-bit 200-MHz CMOS ADC," IEEE J. Solid-State Circuits, vol. 44, no. 9, pp. 2366–2380, Sep. 2009.

[34] A. Verma and B. Razavi, "A 10-bit 500-MS/s 55-mW CMOS ADC," IEEE J. Solid-State Circuits, vol. 44, no. 11, pp. 3039–3050, Nov. 2009.