

Review on Generation of IRNSS Standard Positioning Signal

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Abstract - The two types of services given by the IRNSS (Indian Regional Navigational Satellite System) satellites are Standard Positioning Service (SPS) and the Restricted Service (RS). Both of the services will be in two frequencies of L5 (1164.5 MHz) and S (2472.5 MHz) band. In this paper a study is made on the Generation of IRNSS Standard Positioning Signal. This paper additionally shows the IRNSS Master Frame. The Navigational data and the PRN code produced by the IRNSS is X-ORed, the X-ORed output is modulated by BPSK with Local oscillator and then it is passed through up converter to get IRNSS SPS. In demodulation Phase, the signal is passed through Down Converter and it is demodulated by using BPSK with a Local Oscillator and then the output is X-ORed with IRNSS code to get Navigational Data. The output obtained is implemented using XILINX Software.

Key Words: MATLAB, FPGA Hardware and ISE Simulator.

I. INTRODUCTION

IRNSS Refers to an Indian Regional Navigation Satellite Systems and it is developed by INDIA, with an Operational name of NAVIC. Satellite is an artificial object that rotates around the earth in order collect the information and for the communication. The IRNSS is covers INDIA and it extended up to 1500km from its boundary of an INDIA. The IRNSS provides an accurate real-time positioning and also for timing services. Navigation Satellites are very useful in today's date.

If the India has an IRNSS, in this case would not have to ask anyone else. It would also get Indian scientists a lot of experience in fields they have never ventured before, which can be used for a lot of other projects. The IRNSS gives the services. These services are standard positioning services and restricted services.

This Paper only deals with the generation and analysis of IRNSS SPS signal. Both the services will be provide at two types of frequencies, that is L5 (1164.5 MHz) and S (2472.5 MHz) band. This paper will produce and analyze the IRNSS SPS signal by using

MATLAB and implemented through FPGA KIT and also analyze the frame structure which is received from satellite. The IRNSS Signals are modulated by using three signals. The modulation scheme for IRNSS is BPSK, BOC and Pilot channel BOC. These signals are combined and form a composite signal and analyze the spectrum. The modulation schemes are,

BPSK Modulation: The BPSK refers as Binary Phase Shift Keying and it is digital modulation technique. Here the binary one and binary zero are represented by the different phases each carrier is around 180 degree apart. The BPSK scheme is used 2 phases to represent the two binary digits and is known as binary phase-shift keying.

The result of the transmitted singles is for one bit time, that represented by S (t)

$S(t) = A \cos(2\pi f_c t)$ it is for binary 1

$S(t) = A \cos(2\pi f_c t + \pi)$ it is for binary 0.

BOC Modulation: The idea of the BOC modulation is to reduce the interferences by using BPSK-modulated signal and it has sinc function shaped spectrum. Therefore, BPSK-modulated signals such as C/A codes have most of their spectral energy concentrated around the carrier frequency, while BOC-modulated signals have low energy around the carrier frequency and two main spectral lobes further away from the carrier.

Pilot channel: the pilot channel is used to providing the greatest possible benefit to signal tracking.

II. RELATED WORK

The generation of GPS signals using FPGA based Xilinx System Generator 9.2. The Consideration of L1 frequency band is mainly used for commercial, civil aviation and also for other purposes. Once GPS signals are generated in the simulated laboratory environment then test the proper working of multichannel GPS receiver which is an extension of this paper. After

obtaining an accurate laboratory results, go with the real GPS signals [1]

The implementation VLSI for the correlator/demodulator chip suitable for direct sequence, spread spectrum operation is presented by Zimmermann and Neeracher. This design integrates the code correlation and data demodulation of a RAKE receiver into a single package. It allows the use of either BPSK and/or QPSK encoding, with the PN code lengths of between the 15 to 1023 chips, at a clock rate of up to 16 MHz [2]

This paper present's two ASIC designs for a spread spectrum wireless local area network. The first implements the matched filter, the performing square root raised cosine filtering, while the second calculates complex correlations and coherent BPSK/QPSK demodulation. The PN code rate of 20 Mchips/s is cited as being typical, with the resulting bit rate from 16 kb/s to 2 Mb/s. Both devices are clocked at 65 MHz [3].

The single ASIC CDMA digital receiver for space applications is proposed in [4]. It is has assumed that the receiver is used by a low earth orbit satellite and also for Doppler effects are taken into account during the acquisition phase. The QPSK modulation is used with the Gold code and also maximal length sequences operating ranges from 250 bps to 300 kbps.

The design for a code phase shift keying spread spectrum receiver is presented in this paper. The FPGA is used to implement a baseband code PSK, M-ary decoder using the double threshold detection schemes. An analog IF and demodulator stage are constructed using discrete components and an interfaced to the FPGA, with carrier recovery being performed by a Costas loop. This section looks at the effects of introducing Additive White Gaussian Noise (AWGN) into the communications channel. This can be used to simulate quiet atmospheric interference, as well as the effects of other co-channel users who are using properly correlated PN codes [5].

The Gold code also known as Gold sequence it is a type of binary sequence and used in telecommunication (CDMA). The Pseudo noise (PN) sequences are widely used in digital communications. Pseudo-random Noise (PN) generators are at the heart of every spread spectrum system PN generators are based upon Linear Feedback Shift Registers (LFSRs). The set of Gold codes can be generated by using two steps. That is Pick two maximum length sequences of the same length $2n - 1$

such that their absolute cross-correlation is less than or equal to $2(n+2)/2$, where n is the size of the LFSR used to generate the maximum length sequence [6].

The LFSR based on PN Sequence Generator technique is used for various cryptography applications, designing encoder and for decoder in different communication channel. It's more important to test and verify by an implementing any hardware for getting the better efficient result. The FPGAs is used for implementation of any logical functions for faster prototype development.

It is necessary to implement the existing designs of LFSR on FPGA to test and verify the simulated & synthesis result between different lengths. The total number of random state generated on LFSR depends on the feedback polynomial. It is simple counter so it can count maximum of $2^n - 1$ by using maximum feedback polynomial. Here in this paper implemented 8, 16 and 32-bit LFSR on FPGA by using VHDL to study the performance and an analysis the behavior of randomness[7].

III. PROPOSED METHODOLOGY

Figure one shows the Block Diagram of IRNSS Standard Positioning Signal

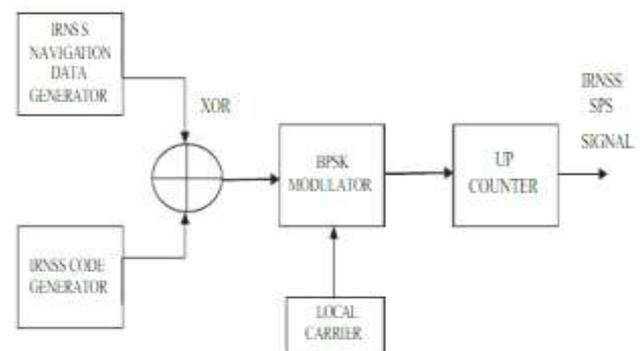


Fig 1: Generation of IRNSS SPS Signal

The Navigational data and the PRN code produced by the IRNSS is X-ORed, the X-ORed output is modulated by BPSK with Local oscillator and then it is passed through up converter to get IRNSS SPS. Figure 2 shows the Demodulation of IRNSS Standard Positioning Signal

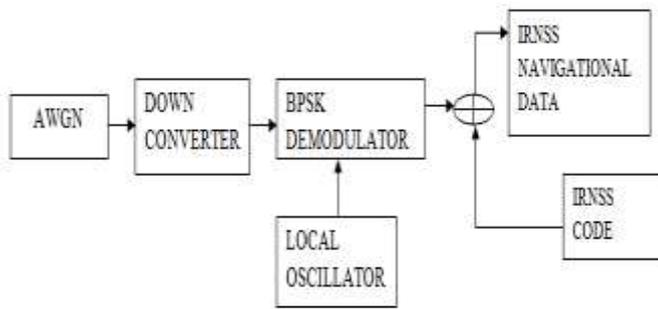


FIG 2: Demodulation of IRNSS SPS Signal

In demodulation Phase, the signal is passed through Down Converter and it is demodulated by using BPSK with a Local Oscillator and then the output is X-ORed with IRNSS code to get Navigational Data. The output obtained is implemented using XILINX Software.

V. RELATED CODES FOR IRNSS SPS

➤ PN SEQUENCE

A pseudorandom noise (PN) sequence is the progression of ones and zeros that does not have any definite pattern and also comprises the deterministic sequence of a pulse that will rehashed after the period and which is the most extreme length sequence. In this legitimate random of a sequence, the bit pattern is never rehashes. The pseudo random, a binary sequence is the semi-random sequence as its seems arbitrary inside of a sequence length, The satisfying the needs of the randomness and the whole sequence rehashes uncertainly.

This PN sequence generation is normally a Linear Feedback Shift Register (LFSR). It has creates the maximal length sequence of length $N = 2n - 1$ components. In view of the great autocorrelation two comparable PN sequences can without much of a stretch to be staged synchronized and the notwithstanding when one of them is debased by noise.

➤ Gold Sequence

The Gold sequence is developed by XOR of a favoured pair of m-sequences with the same timing. They have very much characterized of cross-correlation properties and just for the straightforward of hardware and it is an expected to create vast number of one of the kind codes. In this gold sequence of the length can be denoted as, $L = 2n - 1$, one uses the two LFSRs and each of the length consist $2n - 1$. On the off chance that

Linear Feedback Shift Register (LFSR) is the picked appropriately and gold sequences has better cross correlation properties.

The upside of gold code is the producing bigger number of codes size. The Gold and Kasami are demonstrated that for a certain well-picked m-sequences and the cross-relationship just takes three conceivable values such as $\{-1, -t(n) \text{ or } t(n) - 2\}$. A cross correlation is between the codes of uniform and limited.

$$t(n) = 1 + 2^{n+1/2} \text{ for } n = \text{odd}$$

$$t(n) = 1 + 2^{n+2/2} \text{ for } n = \text{even}$$

Here $t(n)$ depends an exclusively on the length of the LFSR utilized. The fact is that, for an LFSR with “n” memory components and gold code family is estimate $M = 2n + 1$, $n =$ shift register stages. The code size increments with an expanding the quality of the phase register.

VI. CONCLUSION

The research motivation for this paper is to develop an IRNSS SPS signal and also implement the output in FPGA Kit, analyze the Frame Structure which is briefly explained in the introduction part.

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