A NOVEL SOFT SWITCHING PWM DC-DC CONVERTER

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Abstract: This paper presents the design of a soft-switching boost dc-dc converter. Passive soft-switching is employed due to its advantages over the active soft-switching and its ability to reduce switching losses. A Laplace transform-based analysis of the converter circuit is carried out to obtain design information. Experimental results obtained from the prototype agree closely with the predicted results and demonstrate the feasibility of the system.

Key words: Boost Converter, Active, Passive, Laplace transform, Pulse width modulation.

1. INTRODUCTION

Semiconductor device switching at high frequency is a major contributor to power loss in converters. Switching devices absorb power when they turn on or off if they go through a transition when both voltage and current are non-zero. As the switching frequency increases, these transitions occur more often and the power loss in the device increases. High switching frequencies are otherwise desirable because of the reduced size of filter components and transformers which reduce the size and weight of the converter circuits.

In resonant switching circuits, switching takes place when the switching device voltage and/or current are/is zero, thus avoiding simultaneous transitions of voltage and current and thereby eliminating switching losses. This type of switching is called “soft” switching. Resonant converters include resonant switch-mode converters, load resonant converters, and resonant dc link converters [1]. A successful soft-switching scheme should be able to reduce the switching losses, diode reverse recovery losses, and switching voltage and current stresses on converter components. Any of the two main soft switching approaches which include the zero-current switching and the zero-voltage switching may be employed depending on the semiconductor device technology that will be used. For example, MOSFETs present better performance under zero-voltage switching (ZVS). This is because under zero-current switching the capacitive turn-on losses increase the switching losses and the electromagnetic interference (EMI). On the other hand, insulated gate bipolar transistor (IGBTs) and bipolar junction transistors (BJTs) present better results under zero-current switching (ZCS) which can avoid the turn-off losses caused by the tail current [2].

Furthermore, the last twenty years have witnessed an intensive research with the sole aim of achieving lossless switching of semiconductor devices. Lossless switching increases circuit efficiency and makes high frequency operation possible thereby reducing the size and weight of circuit components. Several dc-dc converter configurations aimed at achieving a percentage degree of this goal have been proposed [3,4,5,6,7,8,9]. Each of these proposed circuit topologies has at least one of the following limitations:

(a) Too many circuit components, thus degrading circuit reliability,
(b) High current/voltage stresses on the circuit components,
(c) Complex control circuitry which may include switching current/voltage level detection circuits,
(d) Parasitic capacitor turn-on loss of some of the circuit switches,
(e) Limitation of the output voltage control range to allow for switching transients.

In this paper, a detailed study of the single stage dc-dc employing a versatile and efficient soft-switching circuit cell is presented. In the presented converter, the turn-off and the turn-on of the main active switch and the corresponding freewheeling diode take place under zero-current and/or zero-voltage switching. Also, the turn-on and the turn-off of the circuit cell semiconductor devices take place under zero-current and/or zero-voltage switching.

![Fig. (1) Block diagram of conventional soft-switched dc-dc converter.](image)

A lossless switching is achieved under the above scheme while the voltage and current stresses are drastically reduced to the barest minimum through clamping techniques. Figure 1 shows a schematic block diagram of a conventional dc-dc converter. In this paper, the performance analysis and design of the soft-switched dc-dc converter is given. Predicted results from the analysis are verified with experimental prototype.
2. ACTIVE/PASSIVE SOFT SWITCHING

Higher switching frequencies allow reduction of the magnetic component sizes with pulse width modulated (PWM) switching converters. Unfortunately, increased switching frequencies cause higher switching losses and greater electro-magnetic interference (EMI). The switching loss mechanisms include the current and voltage overlap loss during the switching interval and the capacitance loss during turn-on. The diode reverse recovery also causes an additional conduction loss and further contributes to the current and voltage overlap loss. Soft switched pulse width modulated converters can either be passively soft switched or actively soft switched. Active or passive soft-switching methods have been used to reduce these switching losses.

Recently, passive soft switching has received renewed inspection as a better alternative to active methods. Passive methods do not require an extra switch or additional control circuitry. They are less expensive, have higher reliability and have been reported to achieve higher performance/price ratios than active methods [10, 11]. For PWM converters, passive soft switching reduces switching losses by lowering the active switch’s di/dt and dv/dt to achieve zero-current turn-on and zero-voltage turn off. Furthermore, by controlling the di/dt of the active switch, the reverse recovery currents of the diodes are also controlled. The only loss mechanism not recovered with the passive techniques is the energy in the internal capacitance of the switch. However, this loss is much smaller than the other switching losses and may be smaller than the loss incurred by using an auxiliary switch in an active method [10, 11]. Historically, passive soft switching techniques were used to reduce spikes in the switching circuits and were lossy by dissipating the recovered switching energy in resistors [12]. But more recently, many lossless and partially lossless techniques have been proposed [10, 13].

The two necessary components that must be added to the circuit to achieve passive zero-current turn on and zero-voltage turn off are a small inductor $L_r$ and a capacitor $C_o$. The inductor provides zero-current turn on of the active switch and limits the recovery current of the diodes while the capacitor provides zero-voltage turn off of the active switch. However, the topological rules that describe where these components must be placed in the circuit have not been proposed in the literature. Typically the inductor and capacitor have been placed in series and parallel respectively with the active switch. But many other locations are possible and can lower the component count and reduce switch stress. Also additional circuitry accompanying the capacitor and inductor is used to recover their energy to either the load or the input. There are many different proposed circuits to accomplish this. Furthermore, circuitry cells can be constructed that simplify the creation of new soft switching circuits.

The description and analysis of the proposed soft-switched converter, implemented with boost converter is hereby presented. A model of the circuit cell of passively soft-switched pulse width modulated converters can be represented as follows:

![Diagram of passive soft switching circuit cell]

3. BOOST CONVERTER CONFIGURATIONS

There are different possible configurations of the passively soft switching boost converter but the analysis given below is with reference to the configuration shown below:

Definitions: $Z_{os} = W_{os}L_r$; $W_{os}^2 = 1$

![Diagram of Configuration A]

$L_rC_o$:

$$Z_{ot} = W_{ot}L_r; \quad W_{ot}^2 = 1/L_rC_o; \quad W_0 = 1/L_rC_o; \quad C_T = \frac{C_rC_s}{C_r+C_s}$$

The main inductor current at time $t_0$ has a value of $I_1$ whereas the resonant capacitor voltage $(v_{cr})$ has an initial value at time $t_0$ of $V_0$. Also the resonant inductor current $I_r$ and the snubber capacitor voltage $v_{cs}$ at time $t_0$ have values of zero each:

$$i_{lm}(t_0) = I_1; \quad v_{cr}(t_0) = V_0 \quad \text{......... (3.1)}$$

$$v_{cs}(t_0) = 0; \quad i_{lr}(t_0) = 0 \quad \text{......... (3.2)}$$
**Stage 1: \( t_0 \leq t \leq t_1 \)**

This stage lasts between time \( t_0 \) and \( t_1 \). Here \( S_M \) is turned on at zero current switching, the output voltage \( V_0 \) is across the resonant inductor \( L_r \) and the resonant inductor current \( i_{lr} \) rises to \( I_1 \) after \( D_m \) recovers from conduction. That is,

\[
I_{lm}(t_1) = I_1; \quad V_{cr}(t_1) = V_0 \quad \text{............... (3.3)}
\]

\[
V_{cs}(t_1) = 0; \quad i_{lr}(t_1) = I_1 \quad \text{............... (3.4)}
\]

It is worthy to note that here \( S_m \) turns on at zero-current and \( D_m \) turns off at zero-voltage because of the resonant inductor connected in series to \( S_m \) and snubber capacitor \( C_s \) connected across \( D_m \). The circuit operation under this stage is shown below;

![Stage 1 Diagram](image)

At the end of mode 1 when time becomes \( t_1 \) the resonant inductor current is \( I_1 \). That is,

\[
I_1 = -\frac{V_{32}}{L_r}(t_1 - t_0) = \frac{V_0}{L_r}(t_1 - t_0) \quad \text{....... (3.5)}
\]

Hence, at \( t = t_1 \), when \( i_{lr} = 1 \) mode 1 stops, therefore, the interval of mode 1 becomes

\[
t_1 - t_0 = -\frac{L_r I_1}{V_{32}} = \frac{L_r I_1}{V_0} \quad \text{....... (3.6)}
\]

**Stage 2: \( t_1 \leq t \leq t_2 \)**

This stage has a time gap between \( t_1 \) and \( t_2 \). Due to the resonant capacitor, oscillation will take place in the loop \( C_r \rightarrow D_{s2} \rightarrow C_s \rightarrow L_r \rightarrow S_m \) as depicted in the figure below. This oscillation will continue until the resonant capacitor voltage discharges to zero (i.e. \( V_{cr} = 0 \)) and its voltage is clamped to zero by \( D_{s1} \) conducting. At the end of stage two we have,

\[
V_{cr}(t_2) = 0; \quad V_{cs}(t_2) = -V_{cs2} \quad \text{....... (3.7)}
\]

\[
i_{lr}(t_2) = I_1 + i_{cs2} \quad \text{....... ... (3.8)}
\]

From the circuit of second stage of operation, three equations can be derived with regard to resonant capacitor voltage, resonant inductor current and snubber capacitor voltage as follows;

\[
Cr\frac{dV_{cr}}{dt} = i_{lr} - I_1
\]

\[
=> Cr[SV_{cr(s)} - V_{32}] = I_{lr(s)} - I_{1/S}
\]

\[
V_{cr(s)} = \frac{I_{lr(s)} - I_{1/S} + V_{cs2}Cr}{Scr} \quad \text{....... (3.9)}
\]

Also,

\[
V_{lr} = L_r \frac{di_{lr}}{dt} = -V_{cs}
\]

\[
L_r[Sf_{lr(s)} - I_1] = -V_{cs(s)} + L_r I_1 \quad \text{....... (3.10)}
\]

Again,

\[
C_s \frac{dV_{cs}}{dt} = i_{lr} - I_1
\]

\[
=> C_s[SV_{cs(s)} - 0] = I_{lr(s)} - I_{1/S}
\]

\[
V_{cs(s)} = \frac{I_{lr(s)} - I_{1/S}}{Scs} \quad \text{....... (3.11)}
\]

Putting (3.9) and (3.11) into (3.10), we have after simplification

\[
i_{lr(t)} = I_1 + \frac{V_0}{Z_{ot}} \sin W_{ot}(t - t_1) \quad \text{....... (3.12)}
\]
The resonant capacitor voltage can also be derived.

Substituting (3.11) into (3.9), we have after simplification

\[ V_{cr}(t) = -V_0 \left[ \cos W_{ot}(t - t_1) + \frac{W_{os}^2}{W_{ot}^2} \cos W_{ot}(t - t_1) \right] \] ...

(3.13)

Also, from equation (3.10),

\[ V_{cr}(t) = L_r i_1 - V_{cs}(t) - S L_r I_{Lr}(t) \]

Combining this with equation (3.9), we have

\[ \frac{I_{Lr}(t)}{SCr} - \frac{I_1}{S^2 Cr} + \frac{V_{32}}{SCr} = L_r i_1 - V_{cs}(t) - S L_r I_{Lr}(t) \]

\[ I_{Lr}(t) \left[ S L_r + \frac{1}{SCr} \right] = \frac{I_1}{S^2 Cr} + L_r i_1 - V_{cs}(t) - \frac{V_{32}}{S} \]

But from equation (3.11) we have

\[ I_{Lr}(t) = SCr V_{cs}(t) + \frac{I_1}{S} \]

Then substituting equation (3.11) we have after simplification

\[ V_{cs}(t) = \frac{V_0 W_{os}^2}{W_{ot}^2} - \frac{V_0 W_{os}^2}{W_{ot}^2} \cos W_{ot}(t - t_1) \] ...

(3.14)

**STAGE 3; t_2 \leq t \leq t_3**

The circuit operation for this stage is shown below;

The resonant capacitor voltage is still clamped at zero as a result of \( D_{s1} \) and \( D_{s2} \) conducting. The resonant inductor current \( i_{Lr} \) continues to oscillate about its steady state value in the loop; \( L_r \rightarrow D_{s1} \rightarrow D_{s2} \rightarrow C_s \rightarrow L_r \). At the end of stage three, time \( t_3 \), the oscillator component of the resonant inductor current \( i_{Lr} \) dies down [i.e., \( i_{Lr} (t_3) = 0 \)] and the operation takes the normal form of \( S_m \) conducting and \( D_m \) off. Also the snubber capacitor voltage \( V_{cs} \) reaches a value of \(-V_{cs3}\). That is,

\[ V_{cs}(t_3) = -V_{cs3}; V_{cr}(t_3) = 0 \]

Initial conditions

\[ i_{Lr} = i_{Lr}(t_2) \]

\[ V_{cr} = V_{cr}(t_2) = 0 \]

\[ V_{cs} = V_{cs}(t_2) \]

Here there are two equations that describe the path of the excess current:

\[ \frac{C_s dV_{cs}}{dt} = i_{Lr} - I_1 \]

\[ \therefore C_s \left[ SV_{cs}(t) - V_{cs}(t_2) \right] = i_{Lr}(t) - I_1/S \]

\[ \Rightarrow SCr V_{cs}(t) - C_s V_{cs}(t_2) = I_{Lr}(t) - I_1/S \] ...

(3.15)

Also, \( L_r \frac{di_{Lr}}{dt} + V_{cs} = 0 \)

\[ \Rightarrow L_r \left( S L_r i_{Lr}(t) - i_{Lr}(t_2) \right) + V_{cs}(t) = 0 \]

\[ \therefore V_{cs}(t) = -L_r \left( S L_r i_{Lr}(t) - i_{Lr}(t_2) \right) \] ...

(3.16)

Substituting (3.16) into (3.15) we have after simplification

\[ i_{Lr}(t) = I_1 \left[ 1 - \cos W_{os}(t - t_2) \right] + i_{Lr}(t_2) \cos W_{os}(t - t_2) - \frac{V_{cs}(t)}{z_{os}} \sin W_{os}(t - t_2) \] ...

(3.17)

Also, from equation (3.15) we have

\[ I_{Lr}(t) = SCr V_{cs}(t) - C_s V_{cs}(t_2) + I_1/S \] ...

(3.18)

From equation (3.16) we have

\[ I_{Lr}(t) = \frac{L_r i_{Lr}(t_2) - V_{cs}(t)}{z_{os}} \] ...

(3.19)

Combining (3.18) and (3.19) we have after simplification

\[ V_{cs}(t) = \frac{Z_{os} i_{Lr}(t_2) \sin W_{os}(t - t_2) + V_{cs}(t_2) \cos W_{os}(t - t_2) - Z_{os} I_1 \sin W_{os}(t - t_2)}{z_{os}} \] ...

(3.20)

**STAGE 4; t_3 \leq t \leq t_4**

The resonant inductor current remains constant at a value of \( I_2 \) in the loop \( V_s \rightarrow L_m \rightarrow L_r \rightarrow S_m \rightarrow V_s \).

That is,

\[ i_{Lm}(t_4) = I_2; V_{cr}(t_4) = 0; V_{cs}(t_4) = -V_{cs3} \]

The circuit operation for stage four is as shown below;

Initial conditions are,

\[ V_{cr} = V_{cr}(t_3) = 0 \]

\[ i_{Lr} = i_{Lr}(t_3) = I_2 \]

\[ V_{cs} = V_{cs}(t_3) \]
Here, only one equation applies,
\[
(L_m + L_r) \frac{di_r}{dt} = V_s
\]
\[
\therefore i_r = \frac{\int_{t_3}^{t} V_s \, dt}{L_m + L_r} = \frac{V_s}{L_m + L_r} (t - t_3) + i_1
\]
This mode ends at \( t_4 \) and the resonant inductor current is \( i_2 \).
\[
\therefore i_2 = \frac{V_s}{L_m + L_r} (t_4 - t_3) + i_1
\]
This gives the interval of mode 4 as
\[
(t_4 - t_3) = \frac{(L_m + L_r)(i_2 - i_1)}{V_s} \quad \ldots (3.21)
\]

**STAGE 5: \( t_4 \leq t \leq t_5 \)**

At time \( t_4 \), the main active switch \( S_m \) is opened at zero voltage switching and the resonant capacitor \( C_r \) is charged by the current \( i_2 \). Stage five ends when \( D_{s3} \) is forward biased by taking the loop \( V_s \rightarrow L_m \rightarrow C_s \rightarrow D_{s3} \rightarrow V_0 \rightarrow V_s \).

Under this condition,
\[
V_{cr} - V_{cs} = V_0
\]
\[
i.e, \ V_{cr} + V_{cs3} = V_0
\]
\[
V_{cr}(t_5) = V_0 - V_{cs3}
\]

Since \( V_{cs}(t_5) = -V_{cs3} \)

**STAGE 6: \( t_5 \leq t \leq t_6 \)**

At \( t_5 \) which marks the beginning of this stage the resonant capacitor has charged up to a certain value given by equation (3.22). This causes the resonant inductor current to split into two. One part which tends to discharge \( C_s \) flows through \( C_s \rightarrow D_{s1} \rightarrow V_0 \rightarrow V_s \rightarrow L_m \) the other part flows through \( L_r \rightarrow D_{s1} \rightarrow C_r \rightarrow V_s \rightarrow L_m \) as shown in the circuit below. This continues up to time \( t_6 \) when the resonant capacitor voltage becomes \( V_0 \) causing \( D_{s2} \) to conduct. That is,
\[
V_{cr}(t_6) = V_0; \ V_{cs}(t_6) = -V_{cs6}
\]
These two voltage values remain \( V_0 \) and \( -V_{cs6} \) respectively at the end of stage six. It is necessary to note that \( -V_{cs6} \) is smaller than \( -V_{cs3} \) in magnitude.

At \( t_5 \), \( V_{cr} + V_{cs} = V_0 \) and \( D_{s3} \) starts conducting and there are two parallel paths for current.

**Initial conditions**
\[
V_{cr} = V_{cr}(t_5)
\]
\[
V_{cs} = V_{cs}(t_5)
\]
\[
i_{lr} = i_{lr}(t_5) = I_2 \quad \ldots \ldots \ldots (3.23)
\]

Here, three equations apply,
\[
C_r \frac{dV_{cr}}{dt} = i_{lr}
\]
\[
i.e, \ C_r [SV_{cr}(s) - V_{cr}(t_5)] = I_{lr}(s)
\]
\[
\Rightarrow SC_r V_{cr}(s) - C_r V_{cr}(t_5) = I_{lr}(s)
\]
\[
hhhhhhhhhhhhhhhhhhhV_{cr}(s) = \frac{I_{lr}(s) + C_r V_{cr}(t_5)}{SC_r} \quad \ldots \ldots \ldots (3.24)
\]

Also \( C_s \frac{dV_{cs}}{dt} + i_{lr} = I_2 \)
\[
\Rightarrow C_s \frac{dV_{cs}}{dt} = I_2 - i_{lr}
\]
\[
C_s [SV_{cs}(s) - V_{cs}(t_5)] = I_2/S - I_{lr}(s)
\]
\[
SC_s V_{cs}(s) - C_s V_{cs}(t_5) = I_2/S - I_{lr}(s)
\]
Again, combining (3.24), (3.25) and (3.26), we have after simplification

\[ \dot{V}_{cs(t)} = \frac{I_2}{S} - I_{Lr(s)} + \frac{C_s V_{cs(t)}}{Sc} \ldots \ldots (3.25) \]

Also, the resonant capacitor voltage can be derived. Substituting (3.25) into (3.27) we have

\[ \dot{V}_{cr(t)} = \frac{I_2 W_{os}^2}{W_{ot}^2} + I_2 \cos W_{ot}(t - t_s) - \frac{I_2 W_{os}^2}{W_{ot}^2} \cos W_{ot}(t - t_s) + \frac{V_T}{W_{ot}^2} \sin W_{ot}(t - t_s) \ldots \ldots (3.27) \]

STAGE 7: \[ t_6 \leq t \leq t_7 \]

This stage starts from time \( t_6 \). At this time, \( D_{s2} \) is conducting as well as \( D_{s1} \) and \( D_{s3} \). This clamps the resonant capacitor voltage at \( V_0 \) and also \( V_{cs} = -V_{cs6} \) is placed across the resonant inductor.

\[ \Rightarrow V_{cs(t)} = V_{cs(t)} - \frac{V_0 W_{os}^2}{W_{ot}^2} + \frac{V_0 W_{os}^2}{W_{ot}^2} \cos W_{ot}(t - t_s) + \frac{I_2}{C_s} (t - t_s) \]

\[ - \frac{I_2}{C_s} W_{os}^2 \sin W_{ot}(t - t_s) \ldots \ldots (3.31) \]

Thus the resonant inductor current is further decreased until it becomes zero at \( t_7 \), thus causing the whole of \( I_2 \) to flow through \( C_s \). That is,

\[ I_{Lr}(t_7) = 0;\quad i_{cs}(t_7) = I_2 \]

\[ V_{cs} = -V_{cs7} \]

Initial conditions are

\[ V_{cr(t_6)} = V_0 \]

\[ V_{cs(t_6)} = V_{cs6} \]

\[ i_{Lr(t_6)} = I_{Lr6} \]

Two equations apply in this case:

\[ \frac{C_s V_{cs}}{dt} = I_2 - i_{Lr} \]

\[ C_s [S V_{cs(t)} - V_{cs(t_6)}] - \frac{I_2}{S} - I_{Lr(s)} \]

\[ \Rightarrow V_{cs(t)} = \frac{I_2}{S} - I_{Lr(s)} + \frac{C_s V_{cs(t)}}{Sc} \ldots \ldots (3.32) \]

Also,

\[ \frac{L_r}{dL_r}{dt} = V_{cs} \]

\[ L_r [S L_{r(s)} - L_{r(t_6)}] = V_{cs(s)} \]

\[ \Rightarrow I_{Lr(s)} = \frac{V_{cs}(s)}{L_r} + I_{Lr6} \ldots \ldots (3.33) \]

Combining equation (3.32) and (3.33) we shall have after simplification
\[ I_{Lr(t)} = I_2\left[1 - \cos W_{os}(t - t_6)\right] + \frac{V_{cs}(t_6)}{Z_{os}} S_i W_{os}(t - t_6) + I_{fr(t_6)} \cos W_{os}(t - t_6) \ldots \ldots \ldots (3.34) \]

Also, if we substitute (3.33) into (3.32) we have after simplification

\[ V_{cs(t)} = I_2 Z_{os} S_i W_{os}(t - t_6) - I_{fr(t_6)} Z_{os} S_i W_{os}(t - t_6) + V_{cs(t_6)} \cos W_{os}(t - t_6) \ldots \ldots \ldots (3.35) \]

STAGE 8: \( t_7 \leq t \leq t_8 \)

The soft switching capacitor with \( i_{cs(t_7)} = I_2 \) which is constant till \( t_8 \), discharges till the soft switching capacitor voltage \( V_{cs} \) becomes zero at \( t_8 \). At this point in time the voltage becomes clamped to zero and the charging current \( I_2 \) is transferred to \( D_m \) for conduction so as to discharge the energy in \( L_m \) to the load.

At \( t_8 \) mode of conduction becomes as assumed before \( t_0 \) and this condition will continue till \( t_9 \) when \( S_m \) is turned on again to start a new circuit cycle.

Initial conditions are,

\[ i_{Lr} = i_{fr(t_7)} = 0 \quad i_{cs} = i_{cs(t_7)} = I_2 \]
\[ V_{cr} = V_{cr(t_7)} = V_o \quad V_{cs} = V_{cs(t_7)} \]

But only the snubber capacitor is involved.

\[ C_s dV_{cs} = I_2 \]
\[ C_s \left[ S V_{cs(t)} - V_{cs(t_7)} \right] = \frac{I_2}{S} \]
\[ hhhhhhhhhhhhh \quad V_{cs(t)} = \frac{I_2}{S} + C_s V_{cs(t_7)} \ldots \ldots \ldots (3.36) \]

STAGE 9: \( t_8 \leq t \leq t_9 \)

The main diode \( D_m \) is now conducting current and \( i_{bm} = i_{Lm} \) which falls from \( i_{Lm} = I_2 \) at \( t_8 \) to \( i_{Lm} = I_1 \) at \( t_9 \) when the main active switch \( S_m \) is turned on again to restart the switching cycle. Diagram for \( t_8 \leq t \leq t_9 \) is the same as for the initial stage [see fig (3.3a)]

Initial conditions are

\[ i_{Lm} = i_{Lm(t_8)} = I_2; \quad V_{cr} = V_{cr(t_8)} = V_o \quad V_{cs} = V_{cs(t_8)} = 0 \]

One equation applies to this mode:

\[ \frac{L_m d i_{Lm}}{dt} = V_o - V_o \]
\[ L_m\left[ S i_{Lm(t)} - I_2 \right] = \frac{(V_o - V_o)}{S} \]
\[ i_{Lm(t)} = \frac{(V_o - V_o) + I_2}{S^2 L_m} \]
\[ \therefore i_{Lm(t)} = \frac{(V_o - V_o) + I_2}{L_m (t - t_8)} \ldots \ldots \ldots (3.37) \]

4. CONCLUSION

It is necessary to state here that \( V_s - V_o \) gives a negative value since in a boost converter the output voltage is always greater than the supply voltage. In fact, from the prototype a supply voltage of 48 volts was used to light a bulb of 230 volts. As time progresses from \( t_8 \) the main inductor current which at \( t_8 \) is \( I_2 \), falls gradually to \( I_1 \) which is the value at the beginning of mode 1. The graph below is a measure of the voltage across the load \( R \) from the constructed prototype.

\[ \text{Fig. (13) Voltage across the load } R \]

5. REFERENCES


