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Analysis of 3-Phase Induction Motor with High Step-up PWM DC-DC Converter Using Matlab/Simulink

Naga Sivasankar vangapati[1], M.Venkatesan[2]

[1,2] *Dept of Electrical and Electronics Engineering, Vignan's Lara Institute of Technology & Science, Vadlamudi, Guntur District, Andhra Pradesh, India*

Abstract: *In this paper high step-up pulse width modulation dc–dc converter combining both coupled-inductor and switched capacitor (SC) techniques for Induction motor drive application is presented. The proposed converter consists of a Boost unit, multiple coupled-inductor-SC units, 3-level multilevel inverter and induction motor drive. The proposed converters have increasing the ultra high voltage gain. In this converter for high voltage gain by increasing the multiple CLSC unit or turns ratio of coupled inductor. In this converter the diodes operating soft switching mode and also using drop inductance of coupled inductor. In this proposed converter using low voltage rated transistors and improved efficiency of the converter and also reduced main switch voltage stress. The a novel high step-up pulse width modulation dc–dc converter integrating coupled-inductor and switched capacitor (SC) techniques is fed to a induction motor drive and the implementation of the motor drive is summarized by using MATLAB/SIMULINK R2012b software.*

KEY WORDS- dc–dc converter, Coupled-inductor, switched-capacitor, soft-switching, Multilevel Inverter, Induction Motor.

I.INTRODUCTION

Now a day's high gain DC/DC converter are the main part of renewable energy systems. The high step-up DC-dc converters are mainly using because of renewable energy sources are increased recently. Designers and customers are required low cost and high reliability. In recent years the renewable energy applications need high step-up DC-DC converters with high voltage gain, low output voltage ripple and input current, having high current conduct capability and more efficiency. In recent years of the conventional coupled inductor and switched capacitor based converters have high step-up gain because the turns ratio of the coupled inductor can be increased to boost the voltage gain. At low power grid connected PV system, the transformer less configuration has become a widespread tendency because its higher efficiency, smaller size, lighter weight, and lower cost compared with the isolated transformers. However, the transformer less configuration, the multilevel inverters have adopted with sinusoidal pulse width modulation (SPWM) techniques and the common mode (CM) ground leakage current may appear between DC source and the ground and this brings the safety issue and increase the efficiency of the inverter. Some of the boost converters are not suitable applications for large step up conversion applications, because the boost converters have high duty cycle and high step-up conversion ratio is extremely large, which results give high switching losses, high current ripple and insufficient turn-off period. A lot of coupled inductor and switched capacitor based converters are promulgated, In order to get enormous voltage conversion ratio. The high step-up conversion ratio is increased and the voltage stress of the converters is decreased by using coupled inductor and switched capacitor methods.

The PV panels, low voltage DC sources and energy storage devices, like super capacitors, battery and fuel cells are generally needed to be boost to high voltage level for industrial and commercial applications. This boosted voltage is directly connected to multilevel inverters for AC voltage level. Another choice is first boost the low voltage and directly connected to the bridge inverters. Due to the normal structure the large step-up dc-dc converters used flyback and forward converters. In recent years, many new high step-up dc–dc converters were developed by utilizing some following techniques: switched-capacitor (SC), switched inductor, tapped inductor, and coupled inductor. In this paper, high step-up zero-current switching (ZCS) converters implemented by using resonant SC methods. Among all new techniques, for excessive step-up voltage gain the combination of CLSC is largely adapted. In this proposed converter is used pulse width modulation technique to get large voltage conversion ratio, less magnetic components and active switches are employed. Only two active switches, one coupled inductor and one CLSC unit is used in this proposed converter

This paper proposes high step up DC-DC converter based 3-phase induction motor. To get the analysis of induction motor, 3-level diode clamped multilevel inverter, 5.36HP, 4KW induction motor is used in this proposed converter. The simulation results are verified using

MATLAB/SIMULINK R2012b. The proposed converter simulation results are provided in section IV and concluded in section V.

II. PROPOSED STEP-UP DC-DC CONVERTER

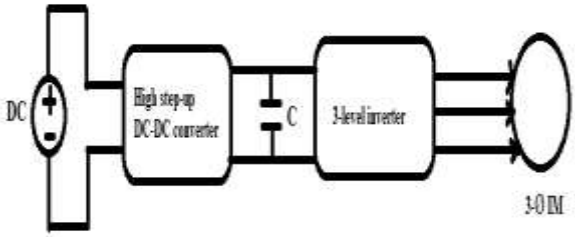


Figure.1 block diagram of the proposed converter

Fig.1 shows the block diagram of the proposed converter. This proposed converter consist of low level DC input voltage, high step up DC-DC converter, diode clamped multilevel inverter and 3-phase induction motor drive. The high step up DC-DC converter is used to get high output voltage from low input voltage and this high step up output voltage is given to the diode clamped multilevel inverter. This inverter is converted the high step up DC voltage into 3-phase AC voltages and given to the 3-phase induction motor drive.

It indicates that the converter is capable of providing ultra high voltage conversion ratio by employing multiple CLSC units or setting a larger turns ratio of the coupled inductor or increasing the duty ratio. For a specific proposed converter, the turn's ratio and the number of CLSC units are fixed, output voltage is controlled by changing the duty ratio in PWM mode to withstand the load and input voltage fluctuations. The duty ratio of the converter cannot be too great and it is usually below 0.8. The turn's ratio is usually not less than 1 for step-up applications. For instance, if the duty ratio is set to 0.5 and the turns ratio is 2, the proposed converter gets the output voltage is 489V from input voltage 60 V. To get the proper operation of the proposed converter, two assumptions is needed i.e. 1) the primary side winding of the coupled inductor is ideal, i.e., no leakage inductance and parasitic resistance, and 2) the input voltage source Vin is ideal, i.e., constant and no series impedance, the proposed converter with one CLSC unit, is shown in Fig.2, wherein L_k is the leakage inductance of the secondary side winding of the coupled inductor and R is the total parasitic resistance of the components including one transistor S1,2, one diode D1,2, one capacitor C1,2 and the secondary side winding of the coupled inductor.

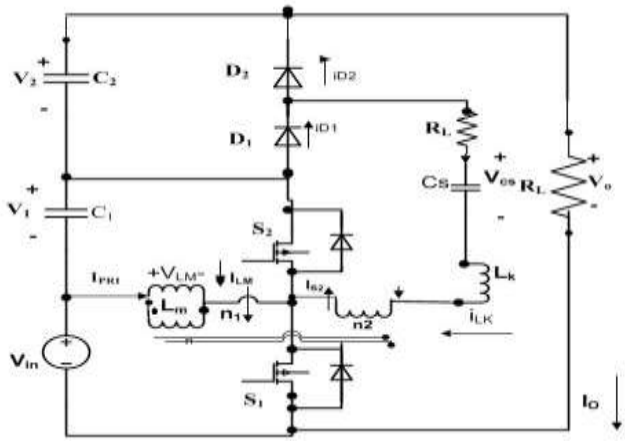


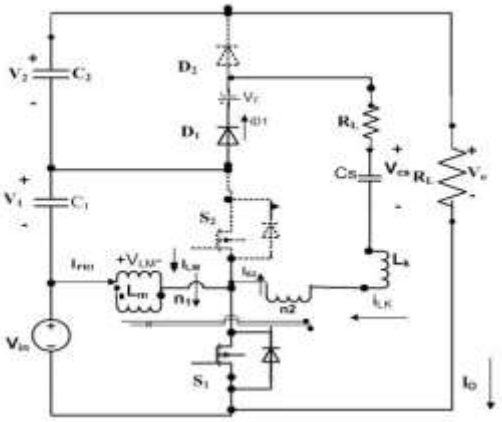
Figure.2 power circuit of the proposed converter.

III.OPERATION PRINCIPLE

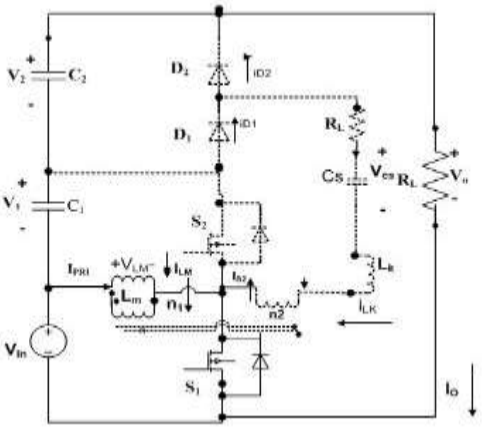
In this proposed converter, transistors S1 and S2 operate in a complementary manner. Based on the assumption that the Q factor of the R - L_k - C_S tank is greater than 0.5, i.e., Q = L_k/C_S /R > 0.5, there are four working modes in one period of a switching cycle. Fig. 3 shows the four-state circuits, where $i_{S1,2}$ and $i_{D1,2}$ are the currents flowing through the two transistors and the two diodes; I_{Lm} and I_{pri} are the excitation current and the current flowing through the primary side winding of the coupled inductor, respectively; i_{Lk} is the current flowing through the R - L_k - C_S tank as well as the secondary side winding of the coupled inductor; V_F is the forward voltage drop of the diode D1,2 . The capacitors C_1 and C_2 are assumed to be much larger than C_S and both their voltages V_1 and V_2 can be seen as constant.

MODE I [t0 < t < t1]: This mode starts by turning S1ON while S2 is OFF. The input voltage V_{in} is directly across the primary side winding of the coupled inductor so that the excitation current I_{Lm} rises linearly from its minimum value I_{min}. At the same time, a higher voltage (n + 1)V_{in} + V_1 – V_F is developed across the R - L_k - C_S tank resulting in the resonant current i_{Lk} increase from zero in under damping resonant mode. The diode D1 is therefore turned ON under ZCS and this mode can be also mathematically described as

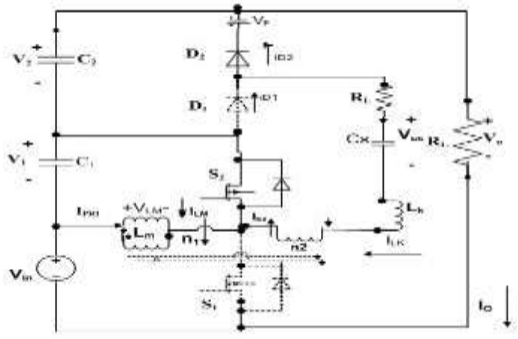
$$\begin{cases} i_{Lk}(t) = \frac{(n+1)V_{in}+V_1-V_F-V_{Cmin}}{\omega_r L_k} e^{-\beta(t-t_0)} \sin\omega_r(t-t_0) \\ V_{C_s}(t) = V_{Cmin} + \frac{1}{C_s}\int_{t_0}^{t} i_{Lk}(\tau)d\tau \end{cases} \quad (1)$$



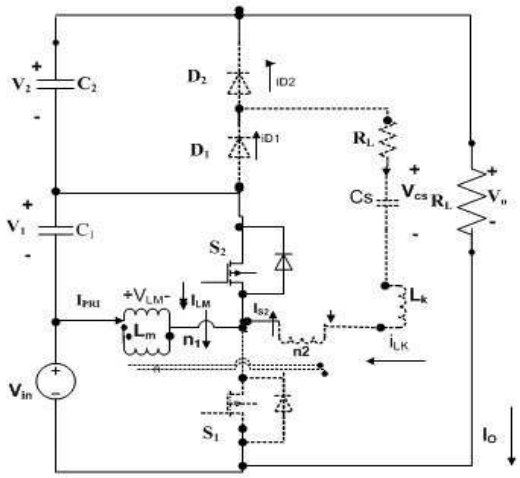
(a)Mode I S1 ON S2 OFF



(b) Mode II S1 ON D1 OFF



(c) Mode III S1 OFF S2 ON



(d) Mode IV S2 ON D2 OFF

Figure.3 Operation mode circuits. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV

$$\begin{cases} I_{Lm}(t) = I_{min} + \frac{V_{in}}{L_m}(t - t_0) \\ I_{pri}(t) = I_{Lm}(t) + n \times i_{Lk}(t) \\ i_{S1}(t) = I_{Lm}(t) + (n+1) \times i_{Lk}(t) \\ i_{D1}(t) = I_{Lk}(t) \end{cases} \quad (2)$$

Where V_{Cmin} is the initial voltage across the capacitor C_S.

MODE II [t1 < t < t2]: Based on the assumption that the conduction duration of the transistor S1 is longer than half of a period of the resonant frequency, i.e., $d \times T_S \geq \pi/\omega r$, here T_S is the switching cycle, $\beta = R/(2L_k)$. The resonant current iLk changes back to zero after half a period of the resonant frequency, and the diode D1 is therefore OFF naturally. The capacitor voltage V_{Cs} reaches to its maximum value $V_{C\,max}$ and this value will be maintained until the next operation mode. The excitation current continues to increase linearly and this mode is mathematically described as

$$V_{Cmax} = (n+1)V_{in} + V_1 - V_F + [(n+1)V_{in} + V_1 - V_F - V_{Cmin}]e^{\frac{-\beta\pi}{\omega r}} \quad (3)$$

$$i_{S1}(t) = I_{pri}(t) = I_{Lm}(t) = I_{min} + \frac{V_{in}}{L_m}(t - t_0) \quad (4)$$

At the end of this mode, the excitation current reaches to its maximum value *I*max, i.e.,

$$I_{max} = I_{min} + \frac{V_{in}}{L_m}D \quad (5)$$

Where again *d* is the duty ratio of the transistor S1 and T_S is the switching cycle.

MODE III [t2 < t < t3]:

This mode starts by turning S1 OFF while S2 is ON. The capacitor voltage V_1 is inversely across the primary side winding of the coupled inductor resulting in the excitation current I_{Lm} fall linearly from its maximum value I_{max}. At the same time, a lower voltage $V_2 + V_F - nV_1$ is developed across the R - L_k - C_S tank so that the resonant current i_{Lk} increases from zero in reverse direction. The diode D2 is therefore turned ON under ZCS and this mode can be mathematically described as

$$\begin{cases} i_{Lk}(t) = \frac{V_2+V_F-nV_1-V_{Cmax}}{\omega_r L_k} e^{-\beta(t-t_2)} \sin\omega_r(t-t_2) \\ V_{CS}(t) = V_{Cmax} + \frac{1}{C_S}\int_{t_2}^{t} i_{Lk}(\tau)d\tau \end{cases} \quad (6)$$

$$\begin{aligned} I_{Lm}(t) &= I_{max} - \frac{V_1}{L_m}(t-t_2) \\ I_{pri}(t) &= I_{Lm}(t) + n \times i_{Lk}(t) \\ i_{S2}(t) &= I_{Lm}(t) + (n+1) \times i_{Lk}(t) \\ i_{D2}(t) &= -I_{Lk}(t) \end{aligned} \quad (7)$$

MODE IV [t3<t<t4]:

Based on the assumption that the conduction duration of the transistor S2 is longer than half of a period of the resonant frequency, i.e., (1 - d) × $T_S \geq \pi/\omega r$, the resonant current i_{Lk} changes back to zero again after half a period of the resonant frequency, and the diode D2 is OFF naturally. The capacitor voltage V_{Cs} reaches to its minimum value V_{Cmin} and this value will be maintained until when the transistor S1 is turned ON while S2 is OFF. Because of this stage, the excitation current continues to decrease linearly. And this mode is mathematically described as

$$V_{Cmin} = V_2 + V_F - nV_1 - [V_{Cmax} - (V_2 + V_F - nV_1)]e^{\frac{-\beta\pi}{\omega_r}} \quad (8)$$

$$i_{S2}(t) = I_{pri}(t) = I_{Lm}(t) = I_{max} - \frac{V_1}{L_m}(t-t_2) \quad (9)$$

When all components are ideal, the voltage gain is V_O / V_{in} = (n + 2)/(1 - d).

TABLE I SPECIFICATION AND COMPONENTS OF THE PROPOSED CONVERTER

Switching frequency, f_s	50 KHz
Input voltage	60V
Capacitor C_1	180μF
Capacitor C_2	100 μF
Coupled inductor n_1:n_2 L_m:L_k	12:25 (24.8 μH:1.9 μH)
Switched capacitors C_s	2.2 μF

Table I shows the simulation parameters of high step up DC-DC converter

A. Multilevel Inverter

In this circuit there are two pairs of switches and two diodes are consists in a three level diode clamped inverter. The DC voltage is divided into three voltage levels with the help DC capacitors. The voltage across each capacitor is $V_{dc}/2$. At any time a set of two switches is on for a three level inverter. Fig.5 shows the three-level diode clamped multilevel inverter.

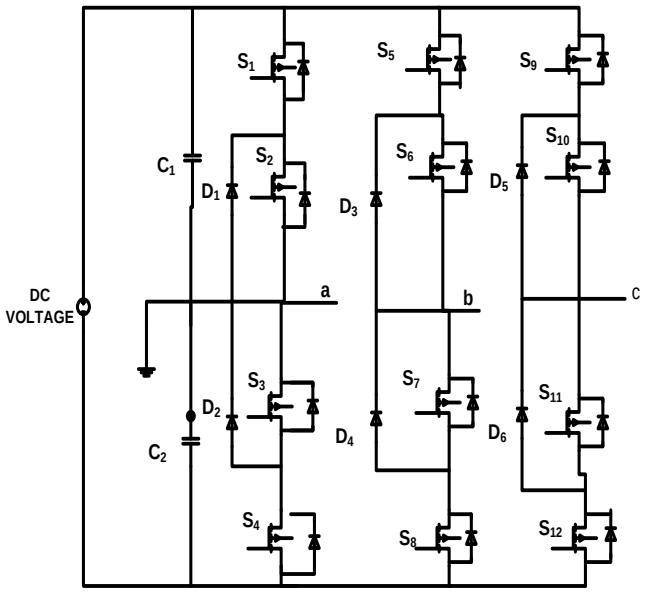


Figure.4 Diode clamped multilevel inverter circuit for 3-phase 3-level inverter

TABLE-II Switching states in one leg of three level diode clamped inverter

Switch state	State	Pole voltage
S1=ON, S2=ON S3=OFF, S4=OFF	S= +ve	V_{a0}=Vdc/2
S1=OFF, S2=ON S3=ON, S4=ON	S= 0	V_{a0}=0
S1=OFF, S2=OFF S3=ON, S4=ON	S= -ve	V_{a0}=-Vdc/2

Table-II shows the switching states in one leg of three-level diode clamped inverter. A three-level inverter, also known as a neutral-clamped inverter, consists of two capacitor voltages in series and uses the center tap as neutral. Each phase leg of the three-level inverter has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes. The output obtained from a three-level inverter is a quasi-square wave output if fundamental frequency switching is used. Multilevel inverter are being considered for an increasing number of applications duo to their high power capability associated with lower output harmonic and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load.

The phase a output voltage Van has three stats: Vdc/2, 0, -Vdc/2. The gate signals for chosen three level DCMLI are developed using MATLAB/SIMULINK. The order of numbering of the switches for phase a is S1, S2, S3 and S4 and likewise other two phases. The DC bus consists of two capacitors C1 and C2, acting as voltage divider.

TABLE III 3-PHASE INDUCTION MOTOR SPECIFICATIONS

Parameter	Rating
Nominal power	4KW
Line-line RMS voltage	400V
Frequency	50HZ
Rotor nominal speed	1480RPM
Stator resistance	1.405Ω
Stator inductance	0.5839Mh
Rotor resistance	1.395Ω
Rotor inductance	0.5893mH
Mutual inductance	172.2mh
Pole pair	2

Table III shows the 3-phase induction motor parameter ratings. The two transistors *S1*, *S2* bear the same voltage stress about 120V. Low-voltage-rated MOSFETs with a small on-state resistance can therefore be used to improve the efficiency. With the resonant design, the two diodes *D1*, *D2* operate under ZCS condition. With synchronous rectification achieved by *S1* and *S2*, the excitation current will drop to below zero when the output power is lower than 120W. As a result, a part of energy charged in the capacitor *C1* will flow back to the input source and this will produce more conduction losses. One method to overcome this problem is to increase the magnetizing inductance *Lm* and another one is to avoid the converter operate under low power condition. The duty ratio of the converter increases from about 0.4 to 0.6. Within this range which is the recommended operating range, power loss caused by the change of the duty ratio is little. In contrast, a lower input voltage causes more conduction losses as the input current is higher. This is why there is a slightly higher efficiency when the input voltage is higher. Overall, the efficiency can be higher than 91%.

IV.SIMULATION RESULTS

The simulation results of the proposed system have been discussed in this system. The proposed system has been simulated by using MATLAB/SIMULINK. The MATLAB/SIMULINK model of the proposed high step up DC-DC converter is MATLAB 2012b. In this section demonstrate all simulated wave form of the proposed converter. Fig.5 shows the simulation diagram of the proposed converter. This proposed converter is combination of high step up DC-DC converter, 3-level diode clamped multilevel inverter and induction motor drive.

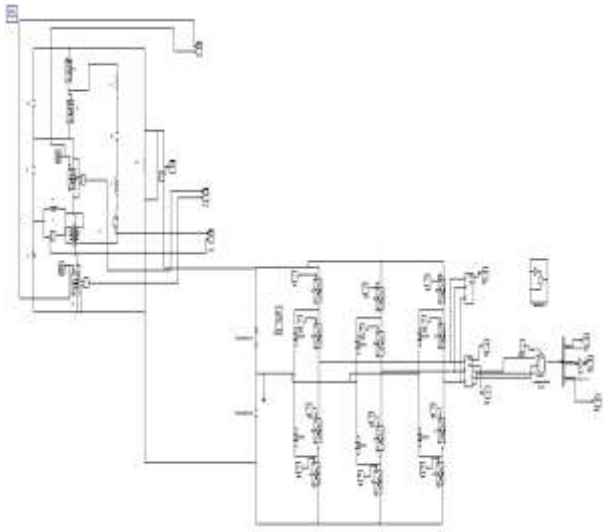


Figure.5 Simulation diagram for proposed converter with soft-switching.

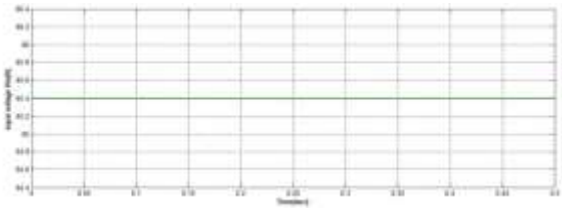


Figure.6 Simulation waveform of proposed converter input voltage V_{in}=60V

Fig.6 shows input voltage of the converter and it is 60V. In this proposed converter, the capacitors C_1, C_2 is connected in series with input voltage. Because of this the capacitors voltage is also added to the input voltage.

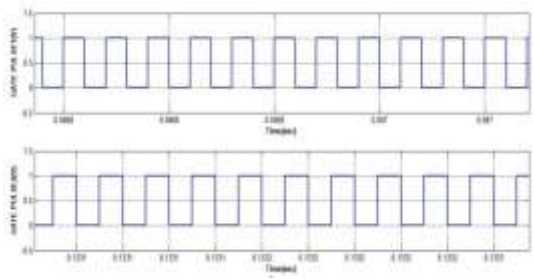


Figure.7 simulation waveform of gate pulse

Fig.7 shows proposed converter simulation waveform of the gate pulses across switches. This gate pulses switching frequency is 50KHZ and duty ratio is 0.5. Two switches operate in complementary manner by using this gate pulses

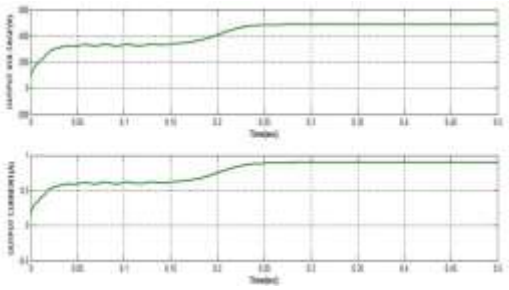


Figure.8 Simulation waveform of proposed converter output voltage V_0=489V & I_0=0.9A

Fig.8 shows the simulation waveform of proposed converter output voltage V_0=489V & output current I_0=0.9A.The output voltage and output current is study state at 0.3sec, because the proposed converter is connected to the multilevel inverter and induction motor drive.

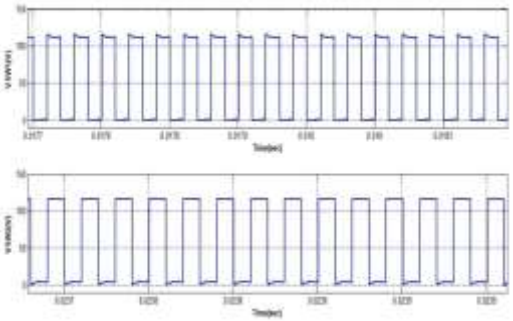


Figure.9 simulation waveform for Vsw1,Vsw2

Fig.9 shows the proposed converter simulation waveform of switches V_{SW1}, V_{SW2}. In this proposed converter MOSFET switches are used, because the MOSFET ON-state resistance is very low and power losses are also low. The voltage across the switches is 120V.

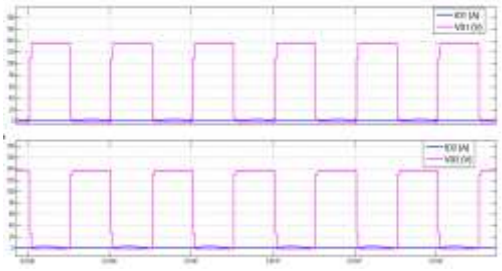


Figure.10 simulation waveform for ID1, VD1,ID2,VD2

Fig.10 shows the proposed converter simulation waveform of ID1, VD1, ID2, VD2. The diodes are operated in this proposed converter under soft switching technique by

using leakage inductance of coupled inductor. The power losses across the diodes are less.

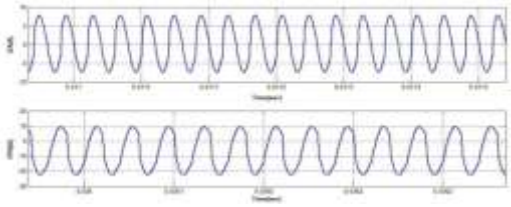


Figure.11 simulation waveform of I_{LK}, I_{PRI}

Fig.11 shows the proposed converter simulation waveform of i_{lk} is the current flowing through the R-LK-CS tank as well as secondary side winding of the coupled inductor and IPRI is the current flowing through the primary side winding of the coupled inductor.

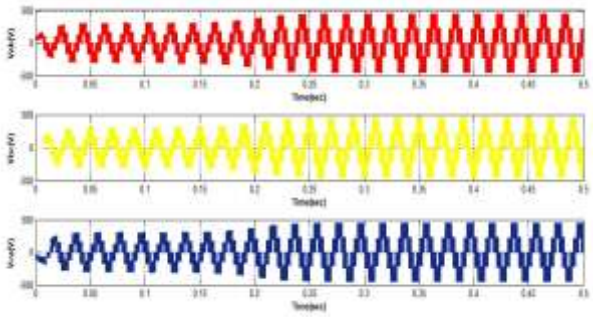


Figure.12 simulation waveform of line-line voltages.

Fig.12 shows the proposed converter simulation waveform of line-line voltages.

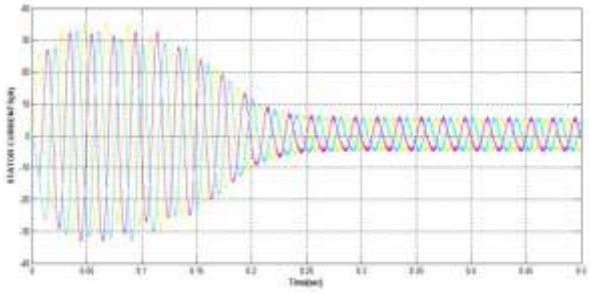


Figure.13 simulation waveform for Line currents

Fig.13 shows the proposed converter simulation waveform of 3-phase stator currents.

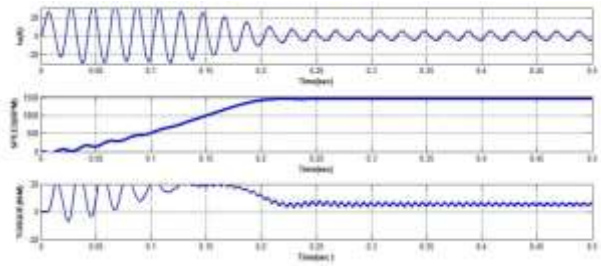


Figure.14 simulation diagram of Stator current, speed, torque

Fig.14 shows the proposed converter simulation diagram of stator current, speed and torque. The stator current of 3-phase induction motor is 6A, The speed of the induction motor is 1480rpm, The torque of the induction motor is 6 N/m when the input voltage 60V, output voltage 489V of the high step up DC-DC converter.

V.CONCLUSION

This paper presents a non isolated high step-up PWM dc–dc converter combining both coupled-inductor and switched capacitor (SC) techniques for Induction motor application. The novel converter output voltage can be extended for Induction motor application. The drop inductance of the coupled inductor is utilized to get soft-switching of the diodes employed in the proposed converter. The voltage stress on the main switches is the same as that in the conventional boost converter with the same input voltage and duty ratio. In this converter used low-voltage-rated MOSFETs with small on-state resistance to improve the efficiency. In this converter high step-up pulse width modulation dc-dc converter combining both coupled-inductor and switched capacitor (SC) techniques is fed to an induction motor and the performance of the motor is analyzed by using MATLAB/SIMULINK R2012b software.

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