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A NOVEL LOW POWER AND LESS TRANSISTOR COUNT LEVEL TRANSLATOR USING 16nm CMOS TECHNOLOGY

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ABSTRACT: - In modern ICs design era many more circuits are design using CMOS because of lowest power consumption. The selections of designing of ICs in various ways i.e. multiple threshold voltage, small signal variations, network configuration etc. In this success with improving technology we are proposing a level translator which is designed and simulated on 16nm technology. In this work we have used modern technology 16nm FinFET is defining new design specification of level translator which shows 58ps delay and 207nW power consumption. Consequentially the energy per transition also reduce as 0.012fJ with the voltage range 0.25mV to 3.5mV and transistor counts is low using 12 transistor only.The frequency obtained in this work is 0.31GHz at 0.25 volt power supply.We have also calculated EDP for this work which is 0.7.

***Index Terms*—Level translator, low power, low gate count, CMOS Technology.**

I INTRODUCTION

In today's System-on-Chip designs **e**nergy efficiency is one of the most important issues to address. Among the techniques known in the literature to reduce power dissipation, those based on power supply voltage reduction are considered very effective even though they can severely penalize speed performances [2]. Power consumption in CMOS circuits is proportional to the square of the supply voltage as well as supply current. Energy and Energy–delay product have become two of the most important design metrics in the current deep submicron technologies for the System–on–chip (CMOS) solutions and multi–core computing architectures for many common applications [4].

Therefore, it is a common practice to use separate supply voltages, in different parts of CMOSs and multi–core processors, in order to reduce the energy consumption [3]. in moderate-speed mixed signal circuits or in digital circuits where different blocks operate at different speeds, employing two or more different supply voltages is advantageous from the power dissipation viewpoint [5]. However, between the part of having a low supply voltage of VDDL and the other part of having a high supply voltage of VDDH, a voltage level translator is needed to convert the logic levels of (VSS, VDDL) to (VSS, VDDH) with minimum additional power dissipation and propagation delay [10].

(a) Level Translator

Level translator is final stage use for shift the output DC level at the second stage down to about 0 volt to ground. It provide interfacing between the components that operate at different level maxim offer a wide range of high speed level, logic level smart card level translator in both unidirectional and bidirectional type. A level translator in digital electronic, also called a logic-level translator, is a circuit used to translate signals from one logic level translator or voltage domain to another.

II. LITERATURE REVIEW

Alexander Shapiro and E. by G. Friedman et. Al. Since the minimum feature size has shrunk beyond the sub-30-nm node, power density has become the major factor in modern microprocessors. Techniques such as dynamic voltage scaling operating down to near threshold voltage levels and supporting multiple voltage domains have become necessary to reduce dynamic as well as static power. A key component of these techniques is a level translator that serves different voltage domains. This level translator must be high speed and power efficient. The proposed level translator translates voltages ranging from 250 to 790 mV, and exhibits 42% shorter delay, 45% lower energy consumption, and 48% lower static power dissipation. In addition, the proposed level translator exhibits symmetric rise and fall transition times with up to 12% skew at the extreme conditions over the maximum range of voltages [1]

Jos´e C. Garcia, and Juan A. Montiel–Nelson et. Al. had implemented on a 65nm CMOS technology they said that highly efficient CMOS level translator qc–level translator, under the large capacitive loading condition (2pF), qc–

level translator has a lower active area (94%), and energy–delay product (21%) than the reference bootstrap level translator circuit. They also said about qc–level translator has very small effective input capacitance in comparison with ts–level translator as it does not need a bootstrap capacitor connected to its input [3]. Manoj Kumar, Sandeep K. Arya, Sujata Pandey et. Al. level shifter for low power application in 0.35µm technology utilize the merits of stacking technique with smaller leakage current and reduction in leakage power, total power consumption 0.49833nW with existing circuit. Single supply level translator has been modified with addition of two NMOS transistors that gives total power consumption of 108.641Pw [6]. Marco Lanuzza et. Al. the multithreshold CMOS technique along with novel topological modifications to guarantee a wide voltage conversion range with limited static power and total energy consumption. When implemented in a 90-nm technology process [7].

The proposed design reliably converts 180-mV input signals into 1-V output signals, while maintaining operational frequencies above 1-MHz, also taking into account process-voltage-temperature variations. Post-layout simulation results demonstrate that the new LS reaches a propagation delay less than 22 ns, a static power dissipation of only 6.4 nW, and a total energy per transition of only 74 fJ for a 0.2-V 1-MHz input pulse [8].

As of above previous work the proposed work are divided in six parts I is introduction about level translator, II is related works, III functioning about of proposed work, IV simulation result, V conclusion and VI future work.

III. PROPOSED WORK

The proposed level translator is based on DCVS in CMOS. Rather than increasing the size of the NMOS transistors, however, the proposed circuit dynamically changes the current sourced by the relevant PMOS pull-up transistor to ensure that the weak NMOS pull-down transistor sinks more current than the PMOS pull-up network sources [9] .The proposed low voltage level translator is shown in Fig. 1. For better performance we put down PMOS W/L ratio 0.004/0.016 where as NMOS W/L ratio kept 3 times higher than PMOS it is 1.2/0.016nm. Let's see the working of proposed circuit for that we divide into two parts one for lower (0) voltage and one for high (1) voltage. Consider the fig 2 (a).

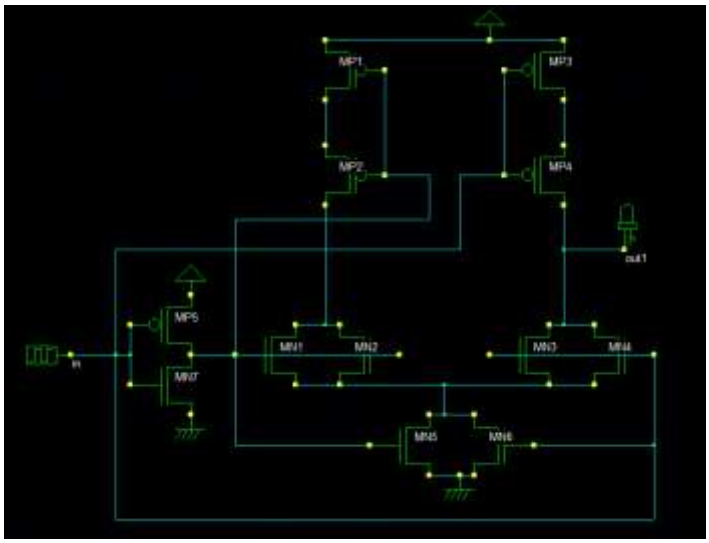

Fig: 1 Proposed circuit diagram of Level Translator

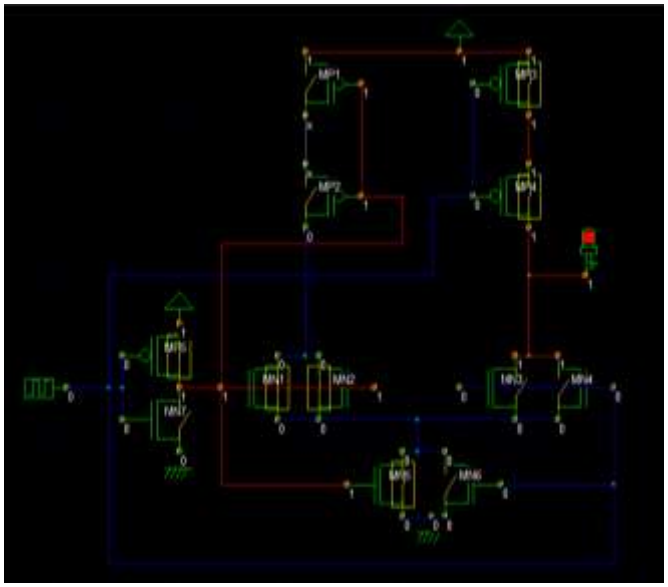

Fig: 2 (a) Output go high of level translator

When the input IN goes down (0) this input divided into three parts, one part input directly feed into series connected inverter (INV), second part feed in second stage of differential amplifier NMOS MN4 and MN6 and the feeder for PMOS MP3 and MP4. The series connected PMOSs provide current mirror of input signal with same time controlling of the current of another PMOSs. Same time another PMOSs are turn off and two inverting NMOSs MN & MN5 is on (1) and rest all NMOSs are turn off with amplifying the signal as well as inverting the current direction.

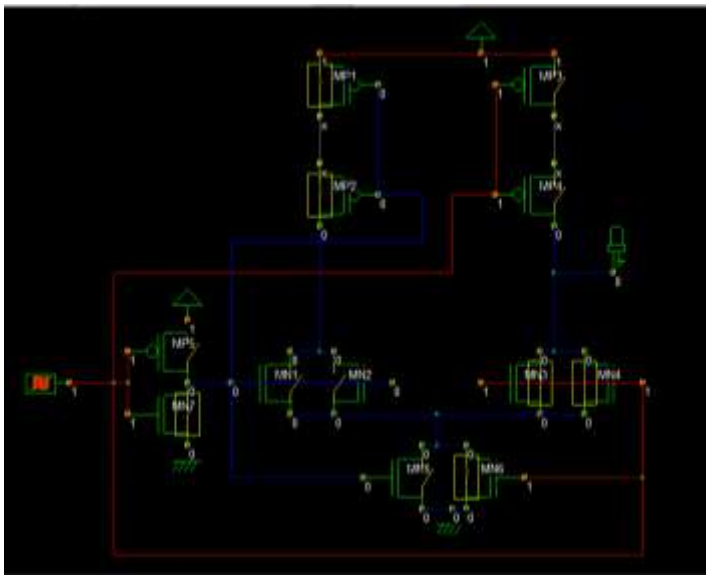

Fig 2 (b): Output goes low of Level translator

Now taking another input value when input IN goes high (1) the same process happens as previous with inverting signal in this time another PMOSs MP1 &MP2 now both are ON by input signal and MN4 & MN6 both are on for inverting of current direction, amplifying signal and giving mirror image of next level of signal or current. As the put down different value of W/L ratio of PMOS and NMOS giving fast switching between them. NMOS keeping higher W/L ratio so it is reducing the lower signal variations.

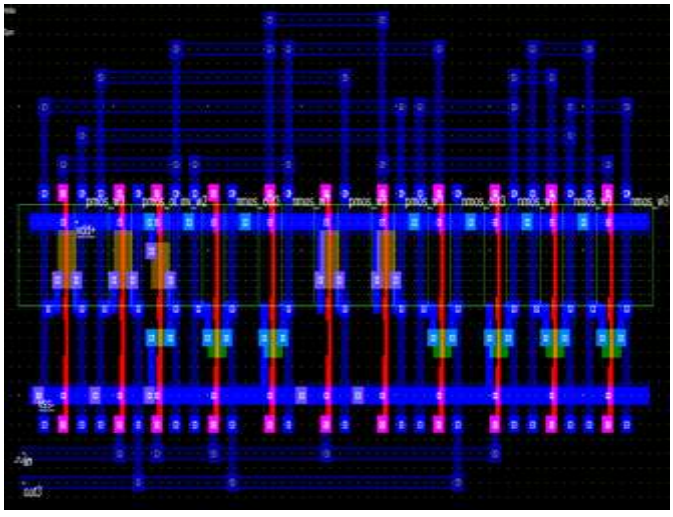

Fig: 3 Layout diagram of proposed level Translator

While dealing with the different kind of signals static power dissipation may be increased in bit of values. And the consideration of Monte Carlo threshold voltage increasing working functions of PMOS and NMOS and reducing the signal distortions while adding noise. The selection of design structure give us less area absorption.

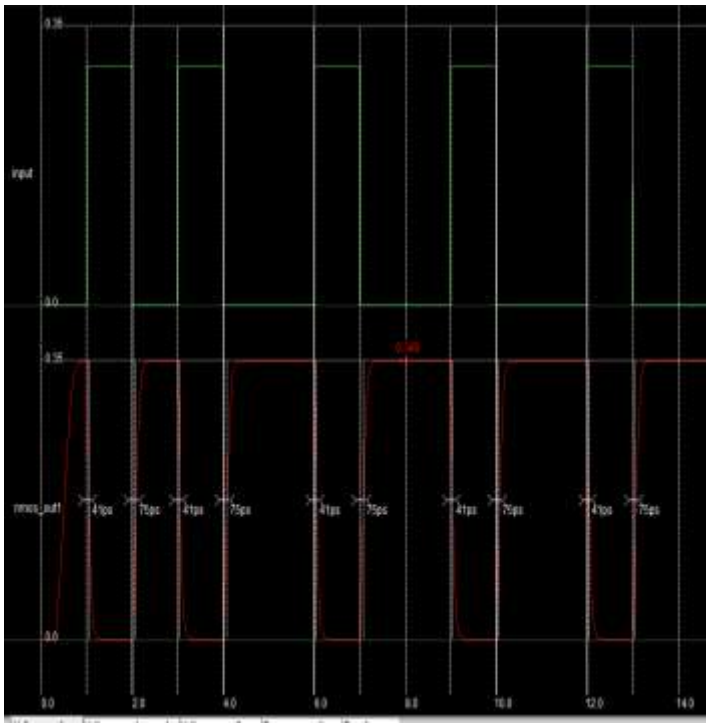

Fig: 4 Waveform & Delay of proposed level translator

IV. SIMULATION RESULT

Extensive Monte Carlo distribution and BSIM4 analysis is carried out on the level translator and includes the intermediate voltage generator as an internal block. The simulation results are given in Table 1. In here by the fast switching of proposed device energy per transition is very less its more then 100 times less to previous work. For reducing static power consumption reducing the 20% of threshold voltage of PMOS and NMOS. Delay has also reduced by the fast transition between each MOSFET. Then temperature variation for analysis 40^0C to 125^0 C. This symmetry degrades for shorter conversion ranges. For the 250mV to 350 mV conversion range, the fall time is lesser than the rise time. With respect to the maximum voltage conversion range, with the best case corners, the mean energy per transition is close to 0.012fJ. The simulation of proposed circuit fig 3 showing layout diagram, fig 4 simulation waveform.

TABLE 1: Comparison between previous work published level translator.

	This work CMOS(16nm)	Previous work FinFET(16nm)
Technology	16nm	16nm
Power Consumptions	207nW	307nW
Energy/ Transition	0.012fj 0.25v,0.31GHz	1.38fj 0.25v,6.3GHz
Delay (ps)	58ps	71.2ps
EDP	0.7	1
Voltage Range	250 to 350mV	250 to 790mV

V. CONCLUSION

As the over all simulation results are showing that the proposed circuit has better performance in three major concentrations The voltage range for this work is 250mv to 350mv. 1. Static power consumption, delay concentration, energy per transition and also reducing the less number of used transistor for this designing. The static power consumption of proposed device is 32.57% less than the previous work with reducing more than 19.57 % of delay, energy/transition is also reduced 99.1% of proposed work. As of the future work for this level translator that can be the dual input signal as well as higher frequency range.

VI. FUTURE WORK

The proposed work has simulated in 16nm CMOS technology as of future it work different other technologies. The proposed work can also design and tested in different transistor level. It can be improve its speed, power and applications.

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