Single Switched Capacitor High Gain Boost Quasi-Z Source Converter

Neelam Lohitha[1], Kamal Kiran Tata[2]

[1]M.Tech Student, EEE Dept., MVR College of Engineering & Technology, Paritala, AP, India
[2]Assistant Professor, EEE Dept., MVR College of Engineering & Technology, Paritala, AP, India

***

Abstract - *A single switched capacitor high gain boost quasi-z source converter proposed to coordinate the separate benefits of quasi-z source converter and switched capacitor. The single switch proposed converter maintains low current stress across the switch, lowers the voltage stress of diodes at output and maintains an excellent voltage gain across the load unlike other step-up DC – DC converters with utilizing almost same components like other step-up DC – DC converters. By maintaining all these, the proposed converter achieves the maximum efficiency of 92 to 94% (theoretically and practically) with increased reliability. The topological provenience, working standard, parameter choice, and correlation with other DC– DC converters are exhibited. Finally, both simulations and experimental results are given to verify the characteristics of the proposed converter. At long last, the two MATLAB results and hardware results about are given to check the attributes of the proposed converter.*

Key Words: DC–DC converter, High voltage gain, Quasi-Z-source network, Switched-capacitor

1. INTRODUCTION

With the advance of modern industrial applications and the massive exploitation of conventional fossil energy, environmental pollution and energy shortages are becoming more and more serious. Therefore, it is necessary to develop new energy resources such as solar energy, and wind energy, which are renewable and environmental protection, to replace the traditional fossil energy [1, 2]. However, the output voltage of renewable energy sources tends to be low, and far from the desired dc-link voltage level of grid-connected inverters. Thus, there is more and more demand for high step-up DC–DC converters, and lots of research has been carried out on this topic. Many other industrial applications, such as TV-CRTs, X-ray systems, auxiliary power supplies for electrical vehicles, high-intensity discharge (HID) lamps for automobiles, also require dc/dc converters with high step-up voltage conversion ratio [3, 4].

Among the non-isolated DC–DC converter topologies, the traditional boost converter is one of the most commonly used topologies for voltage step-up. Theoretically speaking, its output voltage will be much higher than the input voltage when the duty ratio approaches 1. However, the duty ratio is limited when considering the parasitic parameters of each component. Therefore, in practical applications, the output voltage gain of the conventional boost converter is limited, which often cannot meet the requirements [5–7].

To obtain a higher voltage gain, conventional boost converters can be connected in series [8]. However, the whole system will become complicated due to many components and additional control units, which will increase its cost and size, degrade its efficiency and reliability. In addition to cascading, the voltage gain of the non- isolated DC–DC converters can be increased effectively by using coupled inductors with an appropriate turn ratio instead of traditional inductors [9, 10]. However, the energy stored in the leakage inductance is another problem, which needs to be solved by additional snubber circuits, leading to high volume, high weight and low efficiency.

A converter adopting interleaved configuration has been presented in [11], which can be used to reduce the voltage and current stress and obtain a high voltage gain. In [12] and [13], some high step-up DC–DC converters with voltage multiplier cells have been presented. Moreover, using switched-inductors to replace traditional inductors, some non-isolated high step-up converters have been pro-posed in [14–16]. Similarly, as presented in [17–22], switched capacitor techniques can also be utilized in DC– DC converter topologies to achieve high voltage gain.

However, the above DC–DC converters are all very complex, and the output voltage gain is still not high enough for many practical applications. Therefore, in 2003, the simple, novel and efficient idea of a Z-source network was firstly proposed by [23]. The Z-source impedance network consists of two inductors and two capacitors, connected in an X-shape. The Z-source network was firstly applied in DC–AC inverters, i.e., the traditional Z-source inverter (ZSI) [23], which gives the inverter both buck and boost conversion ability in a single-stage topology. Since then, the Z-source network has greatly advanced due to its distinct advantages, e.g., it utilizes the shoot-through zero state to realize high voltage gain, no dead time is needed, and it avoid mis gating-on caused by the electromagnetic interference (EMI). Therefore, the Z-source inverter is suitable for renewable power generation systems, such as, fuel cells and photovoltaic (PV) applications. Based on the Z-source network, many publications have been reported to develop the performance of ZSI, e.g., the improved ZSI in [24] and the quasi-Z-source inverter (qZSI) in [25–29].

Especially, the quasi-Z-source inverter, not only retains the main characteristics of the ZSI, but also has its own new features, such as continuous input current, low capacitor voltage stress and a common ground for the input and output. The Z-source network and the quasi-Z-source network can also be applied to boost the output voltage gain of DC–DC converters. In [30], a PWM Z-source DC– DC converter is proposed, and its output voltage gain is higher than the traditional boost converter. In [31], a novel Z-source DC–DC converter is presented, which uses the Z-source network to replace the traditional inductor in a conventional boost converter. In [32], based on the quasi-Z-source network, a modified Z-source DC–DC converter is proposed, which provides a higher voltage gain than the converter in [30]. However, the output voltage-gains of these Z-source DC–DC converters are still not large enough for many industrial applications, so it remains a challenge to design higher step-up DC–DC converters.

In this paper, a novel high step-up quasi-Z-source DC–DC converter with a single switched-capacitor branch is proposed and thus named a switched-capacitor quasi-Z - source converter (SC-qZSC). When the switch is turned off, the energy transferred from the inductors is used to charge the capacitors in parallel. When switch is on, the switched capacitors are connected in series to supply the load. Therefore, the converter can provide higher output voltage gain.

The rest of the paper is organized as follows. Section 2 describes the derivation and configuration of the proposed converter. The operating principle and parameter selection are presented in Section 3 and Section 4, respectively. Section 4 also presents the boundary condition between continuous conduction mode (CCM) and discontinuous conduction mode (DCM), and the load ranges of the pro-posed converter under the CCM condition. It is followed by the comparison with other DC–DC converters in Section 5. In Section 6 and Section 7, the simulation and experimental results are presented respectively to verify the theoretical analysis. Finally, a conclusion is drawn in Section 8.

2. CONFIGURATION OF PROPOSED CONVERTER

Based on the switched-capacitor converter in Fig -1[17], and the quasi-Z-Source converter in Fig -2 [32], the proposed converter is depicted in Fig -3.

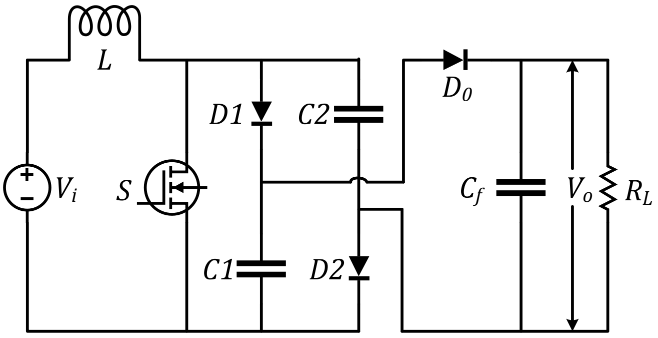

Fig -1: Boost converter with a switched capacitor cell

The basic idea of the proposed converter is using an additional single switched capacitor branch *(C_2, D_2)* combined with another single switched-capacitor branch *(C_1, D_1)* which is hidden in the quasi-Z-source network to form a switched-capacitor cell *(C_1, C_2, D_1, D_2)*. As shown in Fig -3a and Fig -3b, the quasi-Z-source network consists of inductors L_1, L_2, capacitors C_1, C_3, and diode D_1. By combining the switched-capacitor cell with the quasi-Z-source network, the proposed converter can reach a higher out-put voltage gain. According to the position of the additional switched-capacitor branch *(C_2, D_2)*, two kinds of SC-qZSC can be constructed, as shown in Fig -3a and Fig -3b.

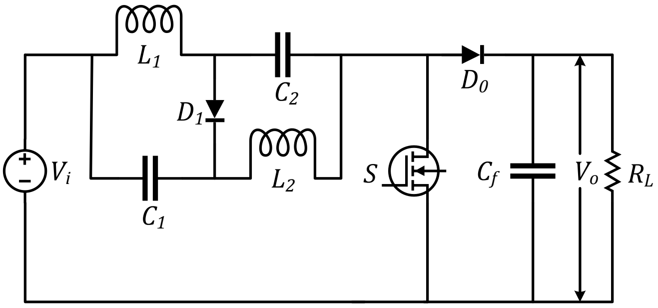

Fig -2: Modified Z-Source DC-DC Converter

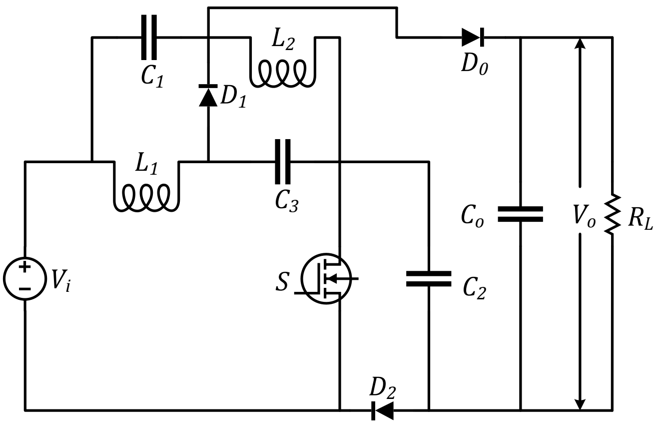

Fig -3a: Proposed Converter (Type -1 model)

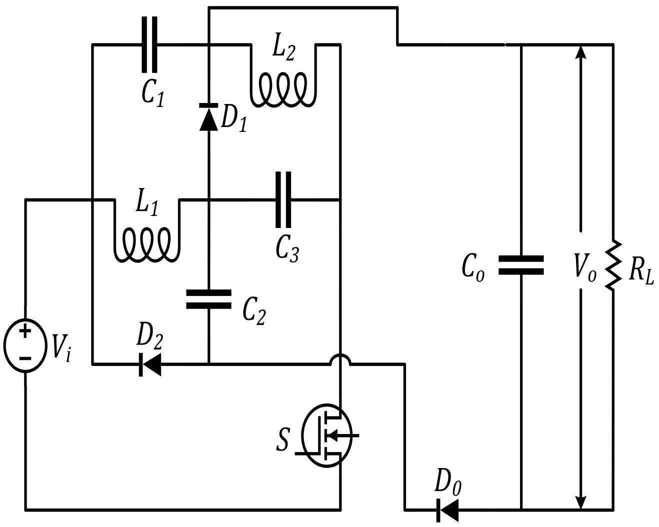

Fig -3b: Type -2 model

3. OPERATING MODES IN PROPOSED CONVERTER

For simplicity, the steady state analysis of the proposed converter is based on the following assumptions.

1) The power switch S (MOSFET), diodes, load resistors, inductors and capacitors are all ideal, and the parasitic effect is ignored.

2) $L_1 = L_2 = L$ and $C_1 = C_3 = C$ in the quasi-Z-source network, and $C_1 = C_2 = C$ in the switched-capacitor cell, thus $C_1 = C_2 = C_3 = C$.

Referring to Fig -3a, when the converter is operating in CCM, there will exist two operation modes, and the corresponding equivalent circuits are shown in Fig -4a and Fig -4b.

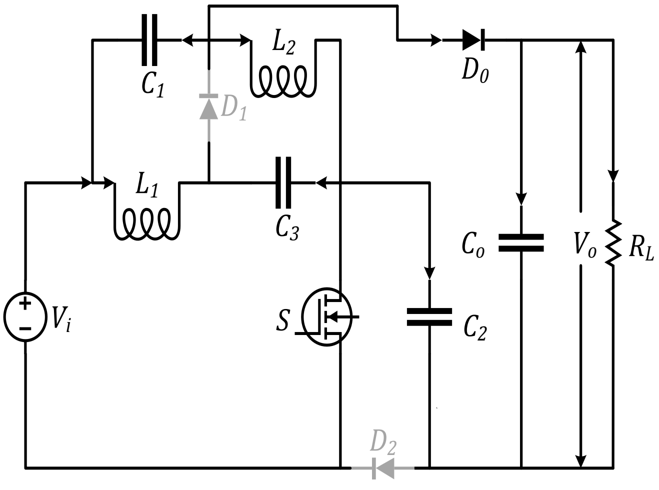

Fig -4a: Mode 1: S, D_o on, D_1 and D_2 off

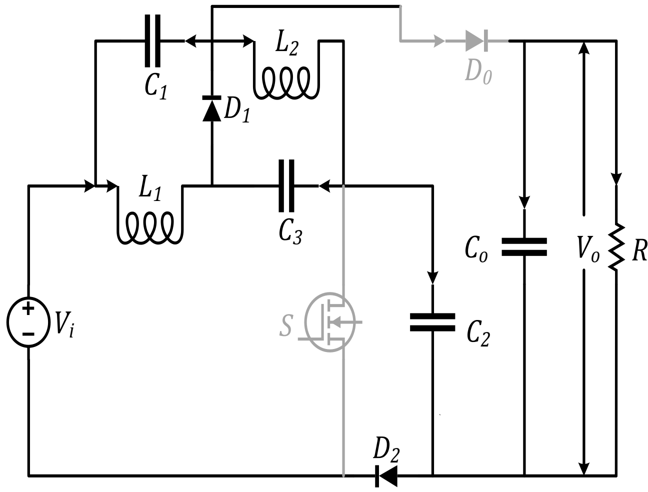

Fig -4b: Mode 2: D_1, D_2 on, S and D_o off

When switch S is on, as shown in Fig -4a, diodes D_1 and D_2 are off due to the reverse parallel connection with capacitors. The input voltage V_i and C_3 charge L_1, and V_i and C_1 charge L_2. Meanwhile, C_1 and C_2 are in series with V_i to supply the load through S. By applying Kirchhoff voltage law, the following steady-state equations can be derived: $\mathrm{v_{L1}}$⍰ $= V_i + V_{C3}$, $\mathrm{v_{L2}} = V_i + V_{C1}$ and $\mathrm{v_o}$⍰ $= V_i + V_{C1} + V_{C2}$. When S is turned off, as shown in Fig -4b, D_1 and D_2 are on, D_o is reverse blocking, inductor L_1 charges C_1, L_2 charges C_3, V_i and L_1 are in series with L_2 to charge C_2, and the load R_L is powered by capacitor C_o. Thus, similar relationships can be obtained: $V_{L1} + V_{C1} = 0, V_{L2} + V_{C3} = 0$ and $V_i = V_{L1} - V_{C3} + V_{C2}$. By the volt-second balance principle of the inductor, the average voltage across an inductor is zero in the steady state. Defining the duty cycle of S as $D = T_{on}/T_s$, where T_{on} is the conduction time of switch S, T_s is the corresponding switching period. Thus, we have:

$$V_{C1} = V_{C3} = \frac{D}{1-2D} V_i \quad \dots\dots\dots\dots\dots \ (3.1)$$

$$V_{C2} = V_i + V_{C1} + V_{C3} = \frac{2-D}{1-2D} V_i \quad \dots\dots\dots \ (3.2)$$

From (3.1) and (3.2), the output voltage V_o can be derived as

$$V_0 = V_i + V_{C1} + V_{C3} = \frac{2-D}{1-2D} V_i \quad \dots\dots\dots \ (3.3)$$

Thus, the output voltage gain G of the proposed SC-qZSC Type-1 converter can be obtained as:

$$G = \frac{V_o}{V_i} = \frac{2-D}{1-2D} \quad \dots\dots\dots\dots\dots\dots\dots (3.4)$$

Similarly, for the converter in Fig -3b, when S is turned on, diodes D_1 and D_2 are off, V_i and C_3 charge L_1, and V_i and C_1 charge L_2. Meanwhile, C_1 and C_2 are in series with V_i and C_3 to supply the load through S. By applying the Kirchhoff's voltage law, the following equations can be obtained. Those equations are: $V_{L1} = V_i + V_{C3}$, $V_{L2} = V_i + V_{C1}$ and $V_O = V_i + V_{C1} + V_{C2} + V_{C3}$ when S is turned off, D_1 and D_2 are on, diode D_o is reverse blocking, the inductor L_1 charges C_1 and C_2 in parallel, L_2 charges C_3, and the load is powered by capacitor C_o. Thus, $V_{L1} + V_{C1} = 0$, $V_{L1} + V_{C2} = 0$ and $V_{L2} + V_{C3} = 0$.

By the volt-second balance principle of inductors L_1 and L_2, one can obtain:

$$V_{C1} = V_{C2} = V_{C3} = \frac{D}{1-2D} V_i \quad \dots\dots\dots\dots (3.5)$$

$$V_O = V_i + V_{C1} + V_{C2} + V_{C3} = \frac{1+D}{1-2D} V_i \quad \dots\dots (3.6)$$

Therefore, the output voltage gain *G'* of SC-qZSC Type-2 can be derived as:

$$G = \frac{V_O}{V_i} = \frac{1+D}{1-2D} \dots\dots\dots\dots\dots\dots\dots (3.7)$$

Comparing the output voltage gain (3.4) with (3.7), it can be found that the output voltage gain of SC-qZSC Type-1 is higher than that of SC-qZSC Type-2. That is, *G=G'+1*. Therefore, take the SC-qZSC Type-1 as the example to present a detailed analysis in the rest of the project.

4. PARAMETER SELECTION

Based on the operating principle analysis in Section 3, parameter selection for SC-qZSC Type-1 will be discussed in this section. Normally, parameter selection of passive and active components in a converter mainly depends on their rated voltages and rated currents. Hence, the voltage and current stresses of each component will be deduced first.

4.1. Voltage stress of each component

According to the operating principle analysis in Section 3, when switch S is on, diodes D_1 and D_2 are off. From Fig -4a, the voltage stresses of D_1 and D_2 can be obtained as:

$$V_{D1} = V_{D2} = \frac{1}{1-2D} V_i \dots\dots\dots\dots\dots\dots (4.1)$$

When S is off, diodes D_1 and D_2 are on, and D_o is off. From Fig -4b, the voltage stresses of S and D_o can be obtained as:

$$V_S = V_{Do} = \frac{1}{1-2D} V_i \quad \dots\dots\dots\dots\dots\dots (4.2)$$

The output voltage V_o and capacitor voltage stresses have been derived in Section 3.

4.2. Current stress of each component

Based on the ampere-second balance property of capacitor C, the average current through a capacitor in steady state is zero, and applying Kirchhoff current law to capacitors C_1, C_2, C_3 and C_O in Fig -4a and Fig -4b have:

$$\begin{cases} \int_0^{DT_s} \left(i_{L1_{on}} - i_{in_{on}}\right) dt + \int_{DT_s}^{T_s} \left(i_{L1_{off}} - i_{in_{off}}\right) dt = 0 \\ \int_0^{DT_s} \left(i_{L1_{on}} + i_{L2_{on}} - i_{in_{on}}\right) dt + \int_{DT_s}^{T_s} i_{in_{off}} dt = 0 \\ \int_0^{DT_s} \left(-i_{L1_{on}}\right) dt + \int_{DT_s}^{T_s} \left(i_{L2_{off}} - i_{in_{off}}\right) dt = 0 \\ \int_0^{DT_s} \left(i_{in_{on}} - i_{L1_{on}} - i_{L2_{on}} - I_0\right) dt + \int_{DT_s}^{T_s} (-I_0) dt = 0 \end{cases} \quad (4.3)$$

Where i_{L_on}, i_{L_off} and i_{in_on}, i_{in_off} are the inductor currents and the input currents when S is on and off, respectively. Assuming that the inductors are large enough, and the inductor currents in each operating mode change linearly, the average inductor current can be expressed as:

$$I_L = \frac{1}{DT_s} \int_0^{DT_s} i_{L_{on}} dt = \frac{1}{(1-D)T_s} \int_{DT_s}^{T_s} i_{L_{off}} dt \dots \ (4.4)$$

Combining (4.4) with (4.3) obtain:

$$\begin{cases} I_{L1} = \frac{2-D}{1-2D} I_o \\ I_{L2} = \frac{1+D}{1-2D} I_o \end{cases} \dots\dots\dots\dots\dots\dots\dots (4.5)$$

When switch S is turned on, the currents through S and the output diode D_o are:

$$\begin{cases} I_S = \frac{1+D}{D(1-2D)} I_o \\ I_{Do} = \frac{I_o}{D} \end{cases} \dots\dots\dots\dots\dots\dots (4.6)$$

When S is turned off, the currents through diodes D_1, D_2 are:

$$\begin{cases} I_{D1} = \frac{2-D}{(1-D)(1-2D)} I_o \\ I_{D2} = \frac{1}{1-D} I_o \end{cases} \dots\dots\dots\dots (4.7)$$

Therefore, the average current flow through switch S and the diodes over a switching period can be derived as:

$$\begin{cases} I_{D1} = \frac{2-D}{1-2D} I_o \\ I_{D2} = I_{Do} = I_o \\ I_S = \frac{1+D}{1-2D} I_o \end{cases} \dots\dots\dots\dots\dots\dots\dots (4.8)$$

Table-1: Voltage and current stresses of the proposed converter proposed SC-qZSC Type-1

Parameter	Voltage stress	Parameter	Current stress
C₁, C₃	$\frac{D}{1-2D}V_i$	*L₁*	$\frac{2-D}{1-2D}I_0$
C₂	$\frac{1}{1-2D}V_i$	*L₂*	$\frac{1+D}{1-2D}I_0$
D₁, D₂	$\frac{1}{1-2D}V_i$	*D₁*	$\frac{2-D}{1-2D}I_0$
D₀	$\frac{1}{1-2D}V_i$	*D₂* and *D₀*	I_0
S	$\frac{1}{1-2D}V_i$	*S*	$\frac{1+D}{1-2D}I_0$

4.3. Parameter selection of inductors

1) Inductors L_1 and L_2: When switch S is off, the inductance of L_1 and L_2, can be derived based on following differential equation:

$$L = \frac{v_L dt}{di_L} \quad \dots\dots\dots\dots\dots\dots\dots\dots \quad (4.8)$$

Where di_L is the inductor current ripple during the OFF state, and $dt = (1-D)T_s$ is the duration of the OFF state. Generally, a larger inductor current ripple will cause a larger current stress in the switch and diodes. Thus, the inductor current ripple should be limited to a permitted range. x_L% of the inductor current, di_L can be expressed as:

$$di_L = \frac{V_L dt}{L} = x_L\% I_L \quad \dots\dots\dots\dots\dots\dots \quad (4.9)$$

Then from Fig -4b, (4.8) and (4.9), we have:

$$L_1 = \frac{(1-D)T_s V_{C1}}{x_L\% I_{L1}} L_2 = \frac{(1-D)T_s V_{C3}}{x_L\% I_{L2}} \quad \dots \quad (4.10)$$

Substituting (3.1) and (4.5) into (4.10), the inductance L_1 and L_2 should satisfy the following equations:

$$\begin{cases} L_{1min} \geq \dfrac{D(1-D)(1-2D)R_L}{(2-D)^2 x_L\% f_s} L_2 \\ L_{2min} \geq \dfrac{D(1-D)(1-2D)R_L}{(1+D)(2-D)x_L\% f_s} L_2 \end{cases} \quad \dots\dots \quad (4.11)$$

It can be observed that for a given load resistance R_L and the duty ratio D, the inductance of L_1 and L_2 will be determined by (4.11) directly.

2) Boundary condition between CCM and DCM: In order to ensure the proposed converter operates in continuous conduction mode, the inductor currents (i_{L1}, i_{L2}) should be maintained continuously during a whole switching cycle, thus

$$\begin{cases} I_{L1} - \frac{1}{2}\Delta i_{L1} \geq 0 \\ I_{L2} - \frac{1}{2}\Delta i_{L2} \geq 0 \end{cases} \quad \dots\dots\dots\dots\dots\dots \quad (4.12)$$

Substituting (4.5) and (4.9) into (4.12), then we have:

$$\begin{cases} \dfrac{2L_1}{R_L T_s} \geq \dfrac{D(1-D)(1-2D)}{(2-D)^2} \\ \dfrac{2L_2}{R_L T_s} \geq \dfrac{D(1-D)(1-2D)}{(1+D)(2-D)} \end{cases} \quad \dots\dots\dots\dots \quad (4.13)$$

Because the Z-source network is symmetric, $L_1 = L_2 = L$. Therefore, from (4.13), the boundary condition between CCM and DCM can be expressed as:

$$\frac{2L}{R_L T_s} \geq \frac{D(1-D)(1-2D)}{(1+D)(2-D)} \quad \dots\dots\dots\dots \quad (4.14)$$

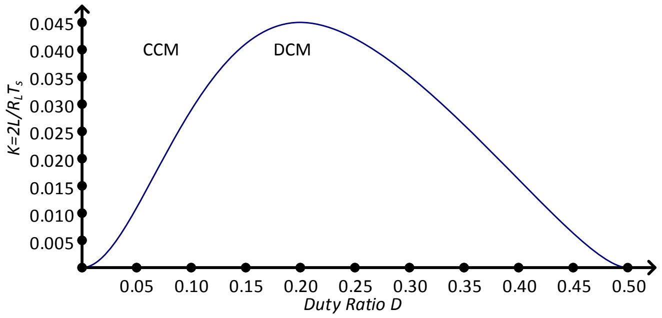

Fig -5: Boundary condition *K* as a function of Duty Cycle *D*

Denote $K=2L/R_L T_s$, and then, Fig -5 shows a plot of the critical ratio K as a function of duty ratio D at the CCM and DCM boundary. From (4.14), we can obtain:

$$R_L \leq \frac{2Lf_s(2+D-D^2)}{2D^3-3D^2+D} \quad \dots\dots\dots\dots\dots \quad (4.15)$$

which is the limited load condition for the converter operating in CCM. The load R_L is proportional to the inductance L in (4.15). Thus, by increasing the inductance L, the load capacity of the converter can be further enhanced. Based on (4.15), when the duty ratio D is equal to 0.204, the maximum load resistance R_{Lmax} can be derived as (4.16) for CCM operation.

$$R_{Lmax} = \frac{2Lf_s}{0.0445} \quad \dots\dots\dots\dots\dots\dots \quad (4.16)$$

Therefore, the proposed converter will operate in continuous conduction mode regardless of the duty ratio D as long as the load R_L satisfies $R_L \leq R_{Lmax}$.

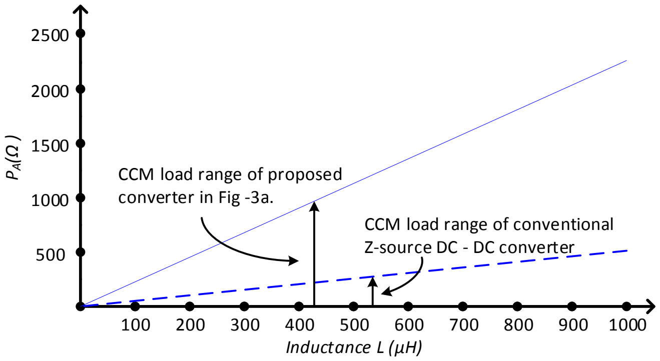

Fig -6: Comparison CCM load ranges between the proposed converter and the conventional Z-Source DC-DC converter

Moreover, a comparison of the CCM load range has been made between the proposed converter and the conventional Z-source DC–DC converter in [30], as shown in Fig -6, for which the switching frequency fs is set to 50kHz. It can be seen that the load range of the proposed SCqZSC Type-1 converter is much wider than that of the conventional Z-source DC–DC converter with the same inductance.

4.4. Parameter selection of capacitors

1) Capacitors C_1, C_2 and C_3: From the above analysis, when switch S is on, the capacitor voltages V_{C1} and V_{C2} are in series with the input voltage V_i to power the load R_L. However, because the sum of V_{C1}, V_{C2} and V_i is a little higher than the output voltage V_o, there will exist a small voltage ripple ΔV_C on the capacitors at the switching frequency. In order to limit ΔV_C to a small range, a permitted fluctuation range $X_C\%$ of capacitor voltage V_C is introduced here.

During the ON state of switch S, capacitors can be designed based on the following differential equation:

$$C = \frac{I_{c_{on}} dt}{dv_c} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.17)$$

where I_{C_on} is the capacitor current when S is on; $dt=DT_s$ is the ON time of S, and $dv_C=x_C\%V_C$. Now $I_{C1\_on} = I_{in\_on} - I_{L1}$, $I_{C2\_on} = I_{L1} + I_{L2} - I_{in\_on}$, and $I_{C3\_on} = - I_{L1}$, so substituting these three equations into (4.17) leads to:

$$\begin{cases} C_1 = \dfrac{(D^2 - D + 1)I_o}{Dx_C\%V_i f_s} \\ C_2 = \dfrac{(1-2D)I_o}{x_C\%V_i f_s} \\ C_3 = \dfrac{(2-D)I_o}{x_C\%V_i f_s} \end{cases} \ldots\ldots\ldots\ldots\ldots (4.18)$$

Therefore, the capacitance of C_1, C_2 and C_3 can be designed by (4.18) directly.

2) Output filter capacitor C_o: Similarly, when S is off, the output diode (D_o) will be reverse blocking. Therefore, the current flow through capacitor C_o will be equal to the output current I_o. Thus:

$$C_0 = \frac{I_0 dt}{\Delta v_{C0}} = \frac{I_0 dt}{x_C\%V_0} \ldots\ldots\ldots\ldots\ldots\ldots (4.19)$$

where dt = $(1-D)T_s$. Substituting (3.3) into (4.19), the capacitance of capacitor C_o can be obtained as:

$$C_0 = \frac{(1-D)(1-2D)I_0}{(2-D)x_C\%V_i f_s} \ldots\ldots\ldots\ldots\ldots (4.20)$$

4.5. Parameter selection of switching devices:

Generally, the parameters of diodes and MOFETs can be selected according to their voltage and current stresses, which have been summarized in Table-1.

5. COMPARISON WITH OTHER DC CONVERTERS

5.1. Comparison of output voltage gains

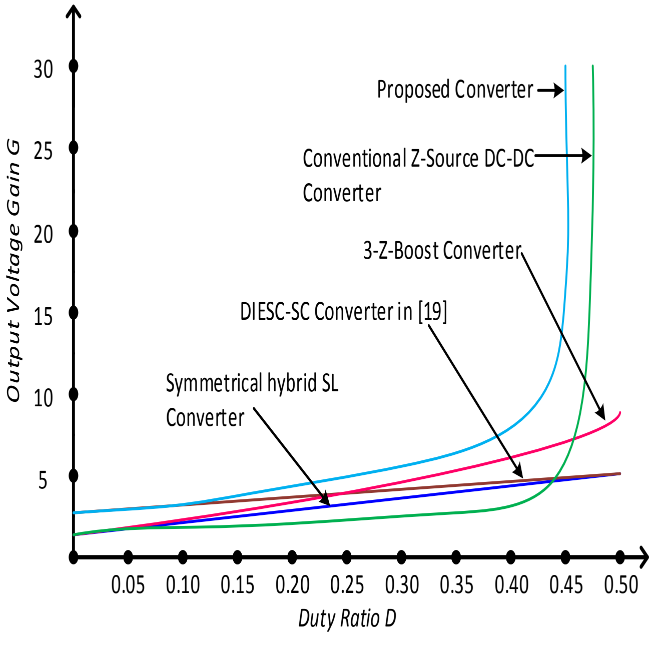

Fig -7: Comparison of output voltage gains

The output voltage gain of the proposed SC-qZSC Type-1 is plotted in Fig -7as a function of the duty ratio D, and compared with the 3-Z-network boost converter in [6], the symmetrical hybrid switched-inductor converter (SH-SLC) in [16], the converter in [19] (the turns ratio of the coupled inductor is set to 1), the high step-up converter with double inductor energy storage cell based switched-capacitors (DIESC-SC converter) in [20] and the conventional ZSC in [30] (Table-2).

Table-2: Comparison of the number of components

Topologies	Inductors	Capacitors	Diodes	Switches
Symmetrical hybrid-SL converter	4	1	7	2
Converter in [19]	1-coupled inductor	4	4	1
DIESC-SC Converter	4	2	9	1
3-Z-network boost converter	2	5	4	1
Proposed Converter	2	4	3	1

The ideal expressions for the output voltage gains are given in Table 3. And all these five converters are non-isolated DC–DC topologies. From Fig -7, it can be observed that the output voltage gain of the proposed converter is higher than that of the other four converters for all duty ratios in the range (0, 0.5).

5.2. Comparison of the number of components

Table-2 shows the comparison of the number of passive and active components used in these five converters. From this table, it can be seen that the total number of components used in the proposed converter is no more than in the other four DC–DC converters. Therefore, compared with these four topologies, the proposed converter can provide higher output voltage gain by using the same or similar active and passive components.

5.3. Comparison of stresses

In this section, the voltage and current stresses of these five converters are compared under the same DC input voltage Vi, input current I_{in}, and output voltage gain G. The stresses on components of these five DC–DC topologies have been summarized and tabulated in Table-3.

The comparison of the output diode voltage stress for these five converters is depicted in Table-3. It can be seen, for producing the same output voltage gain G, the proposed converter has lower output diode voltage stress than the SH-SLC converter and the 3-Z boost converter. Although it is a little higher than the DIESC-SC converter and converter in [19], it requires one less inductor and one less capacitor than DIESC-SC converter and one less diode than the converter in [19]. It can be seen that the proposed converter has lower switching voltage stress than the 3-Z boost converter. However, when the output voltage gain G is larger than 5, it will be a little higher than the SH-SLC converter and the DIESC-SC converter. This is due to the proposed converter has higher boost ability. It can be observed that the proposed converter only has a slightly higher switching current stress than DIESC-SC converter when G is larger than 5, but lower than the other three DC–DC converters.

Table-3: Stress comparison in the same V_i, I_{in} and G

Converter Topologies	ybrid SL	IESC SC	[19]	Z – oost	Proposed
Voltage gain	$\frac{1+3D}{1-D}$	$\frac{2+D}{1-D}$	$\frac{2+D}{1-D}$	$\left(\frac{1+D}{1-D}\right)^2$	$\frac{2-D}{1-2D}$
Voltage stress of switches	$\frac{(1+G)V_i}{2}$	$\frac{(1+G)V_i}{3}$	$\frac{(1+G)V_i}{3}$	GV_i	$\frac{(2G-1)V_i}{3}$
Current stress of switches	$\frac{(G+3)I_{in}}{2G}$	$\frac{(G-1)I_{in}}{G}$	I_{in}	$\frac{\left(\begin{smallmatrix}G+2\sqrt{G}\\+1\end{smallmatrix}\right)I_i}{G}$	$\frac{(G-1)I_{in}}{G}$
Voltage of output diodes	$(1+G)V_i$	$\frac{(1+G)V_i}{3}$	$\frac{(1+G)V_i}{3}$	GV_i	$\frac{(2G-1)V_i}{3}$
Voltage of other diodes	$\frac{(G-1)V_i}{4}$	$\frac{(1+G)V_i}{3}$	$\frac{(1+G)V_i}{3}$	$\frac{\sqrt{G}-1)V_i}{2}$	$\frac{(2G-1)V_i}{3}$
Inductor current	$\frac{(G+3)I_{in}}{4G}$	$\frac{I_{in}}{G}$	I_{in}	$\frac{G+\sqrt{G})I_{in}}{2}$	$\frac{(G-1)I_{in}}{G}$

6. SIMULATION RESULTS

The simulation parameters are selected as per the design conditions in Section 4: Input voltage $V_i = 10V$, capacitors $C_1 = C_2 = C_3 = 330\mu F$, inductors $L_1 = L_2 = 220\mu H$, output filter capacitor $C_o = 330\mu F$, with switching frequency $f_s = 30KHz$, rated output power $P_{out} = 64W$ and $R_L = 1K\Omega$. The simulation circuit in MATLAB shown in Fig - 8.

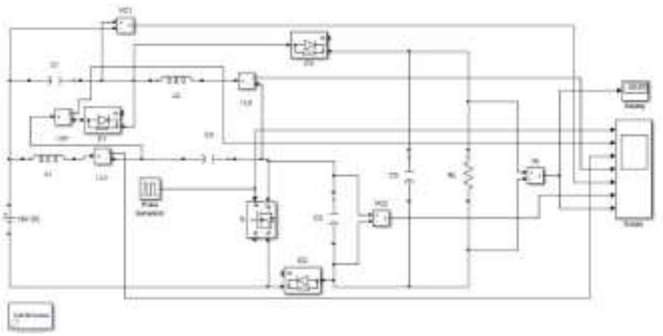

Fig -8: MATLAB simulation circuit for proposed converter

The simulation results are shown in Fig -9a, 9b and 9c. The three graphs each show, from top to bottom, the simulated waveforms for the drain-source voltage of switch S, the voltage of diode D_1 (or D_2), the currents in L_1 and L_2, the voltages of C_1 (or C_3) and C_2, and the output voltage V_o.

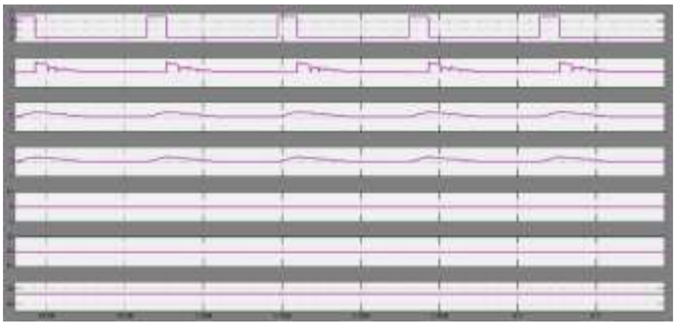

Fig -9a: Duty cycle *D = 0.2*

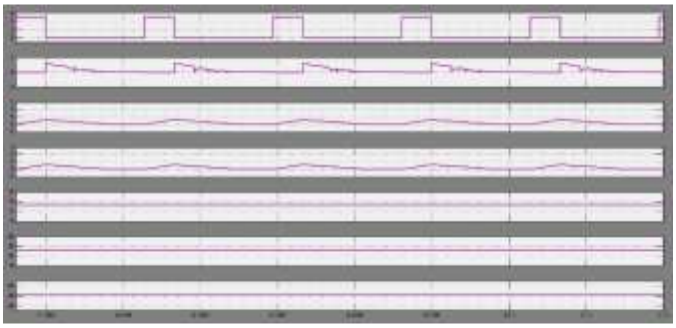

Fig -9b: Duty cycle *D = 0.3*

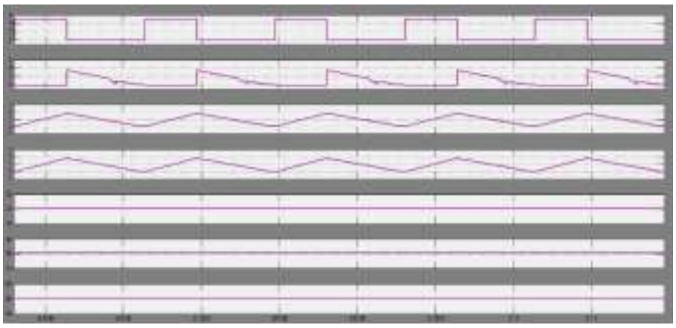

Fig -9c: Duty cycle *D = 0.4*

As shown in Fig -9a, 9b and 9c, the converter operates in CCM and includes two operating states. When the duty ratio is equal to 0.2, the capacitor voltages V_{C1} (or V_{C3}) is about 3.3V and V_{C2} is about 16.67V, and the output voltage V_o is about 30V. When the duty ratio is 0.3, the capacitor voltage V_{C1} (or V_{C3}) is 7.5V, V_{C2} is 25V, and the output voltage is 42.5V. When the duty ratio is 0.4, the capacitor voltage V_{C1} (or V_{C3}) is 20V, V_{C2} are 50V, and the output voltage is 80V. These are all in accordance with the theoretical values calculated from [1], [2], and [3].

7. EXPERIMENTAL RESULTS

A prototype of the proposed converter shown in Fig -10 was built to verify the steady state analysis in Section 3. The experimental parameters were chosen to match the simulation parameters given in Section 6.

The semiconductor switch S (Type: IRFP250N) is driven by the UC3525 basic board with driver IR2101, and three MBRF30H150CT diodes are used for D_1, D_2 and D_o. The ON resistance r_{DS} of switch S is 0.075Ω.

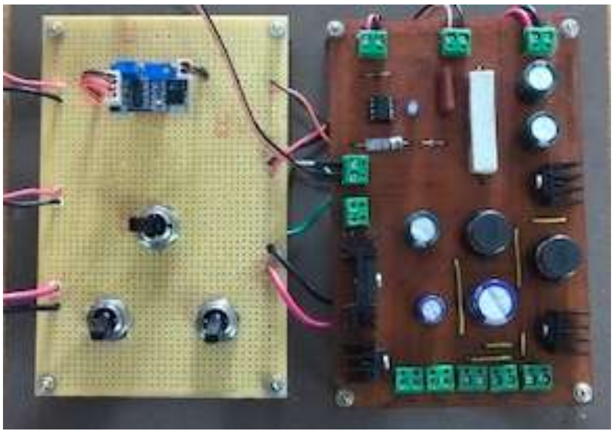

Fig -10: Prototype of the proposed converter

The experimental waveforms of the proposed converter with a regulated DC input voltage source $V_i = 10V$, are shown in Fig -11a, 11b and 11c. From the top to the bottom, in each graph, the waveforms are the driven voltage of switch *S*, V_{GS}; the current of inductor L_1, i_{L1}; the current of inductor L_2, i_{L2}; the capacitor voltages V_{C1} (or V_{C3}) and V_{C2}; and the output voltage V_o. As shown in Fig -11a, when the duty ratio $D = 0.2$, the measured values of capacitor voltages and output voltage are $V_{C1} = V_{C3} = 2.3V$, $V_{C2} = 15.5V$, and $V_o=27.2V$, while the theoretical values are $V_{C1} = V_{C3} = 3.3V$, $V_{C2} = 16.67V$, and $V_o= 30V$. As shown in Fig -11b, when the duty ratio $D = 0.3$, the measured values of capacitor voltages and the output voltage are $V_{C1}= V_{C3} = 5.2V$, $V_{C2} = 22.8V$, and $V_o = 38.1V$, while the expected values are $V_{C1} = V_{C3} = 7.5V$, $V_{C2} = 25V$, and $V_o = 42.5V$. Fig -11c shows the experimental waveforms when $D = 0.4$, the measured values of capacitor voltages and the output voltage are $V_{C1} = V_{C3} = 16.8V$, $V_{C2} = 45.1V$, and $V_o= 70.3V$, while the theoretical values are $V_{C1} = V_{C3} = 20V$, $V_{C2} = 50V$, and $V_o= 80V$. The comparison between theoretical values and measured values is given in Fig -12. It shows there are some differences between the measured values and theoretical values, which are mainly caused by the equivalent series resistance (ESR) of each component and the forward voltage drop of diodes.

In order to take the parasitic parameters of passive and active components into consideration, we assume that the forward voltage drops on diodes are V_D, the parasitic resistances of the inductors are r_L, the equivalent series resistances (ESRs) of capacitors are r_C, and the equivalent drain-to-source on-resistance of switch *S* is r_{DS}.

The efficiency of the proposed converter under the condition of $V_i = 10V$, duty ratio $D = 0.2$ to 0.4, $R_L = 100Ω$ was measured, and a comparison between the measured and the theoretical predicted efficiencies is presented in Fig -13. It can be seen that by increasing the value of the duty cycle the measured efficiency of the proposed converter is reduced, and the difference between the calculated and experimental results is increased. The reason is that by increasing the duty cycle the conduction power losses on devices will be increased, too. This fact applies to all kinds of converters based on impedance source network.

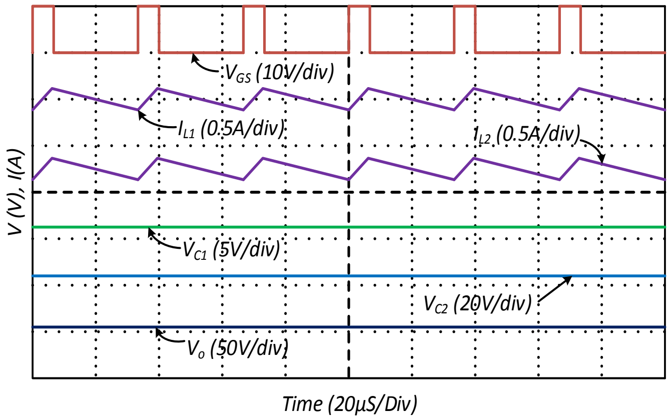

Fig -11a: Duty cycle $D = 0.2$

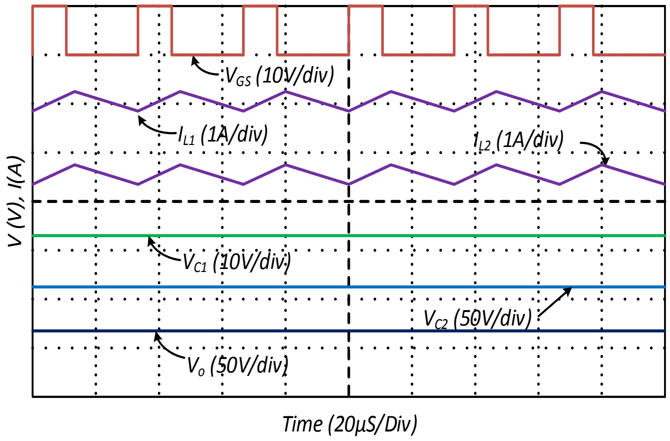

Fig -11b: Duty cycle $D = 0.3$

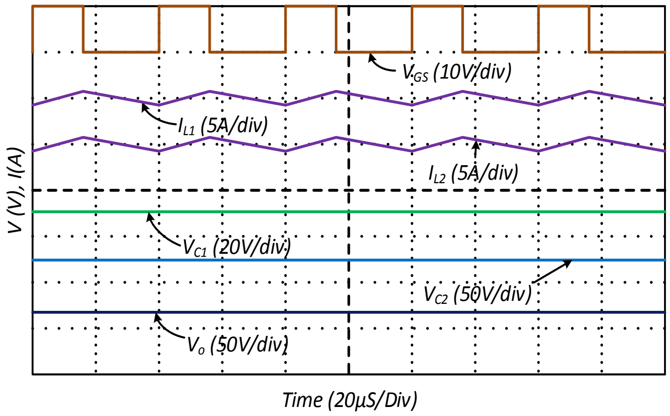

Fig -11c: Duty cycle $D = 0.4$

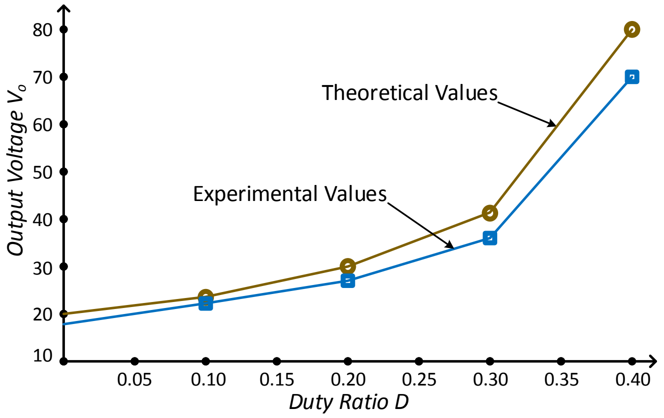

Fig -12: Comparison of experimental & theoretical values

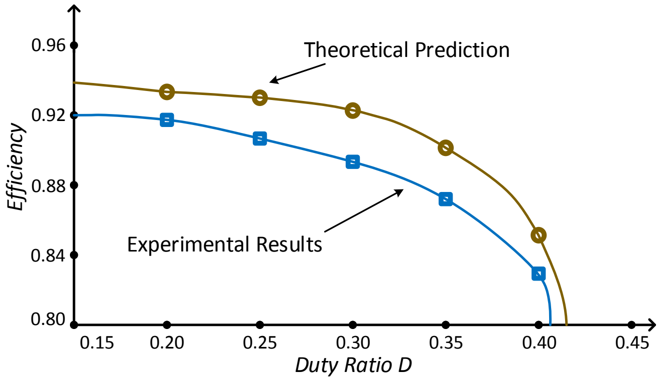

Fig -13: Comparison of practical & theoretical efficiencies

8. CONCLUSION

Based on the respective merits of the switched - capacitor converter and the quasi-Z-source converter, a new high step-up quasi-Z-source DC–DC converter with a single switched-capacitor branch was proposed in this paper. The operating principle analysis, parameter selection, the boundary condition between continuous and discontinuous conduction mode (CCM and DCM), and the comparison with other existed high step-up DC–DC converters have been presented in detail. Finally, both the simulations and experimental results are given to validate the effectiveness of the proposed converter. In comparison with other existed high step-up DC–DC converters, the proposed converter provides higher output voltage gain, lower voltage stress across the output diodes, and lower current stress across the switches. Thus, the efficiency and reliability of the pro-posed converter can be improved, which implies that it would be suitable for high step-up voltage conversion applications, such as TV-CRTs, X-ray systems, high intensity discharge lamps for automobile headlamps, as well as grid connection of renewable energy sources. This work was supported by the Key Program of National Natural Science Foundation of China (No. 51437005).

REFERENCES

[1] Li WH, He XN (2011) Review of nonisolated high step-up DC/ DC converters in photovoltaic grid-connected applications. IEEE Trans Ind Electron 58(4):1239–1250

[2] Shahin A, Hinaje M, Martin JP et al (2010) High voltage ratio DC–DC converter for fuel-cell applications. IEEE Trans Ind Electron 57(12):3944–3955

[3] Rosas-Caro JC, Ramirez JM, Peng FZ et al (2010) A DC–DC multilevel boost converter. IET Power Electron 3(1):129–137

[4] Ioinovici A (2013) Power electronics and energy conversion systems. Wiley, Hoboken

[5] Hua CC, Chiang HC, Chuang CW (2014) New boost converter based on Sheppard–Taylor topology. IET Power Electron 7(1):167–176

[6] Zhang GD, Zhang B, Li Z et al (2015) A 3-Z-network boost converter. IEEE Trans Ind Electron 62(1):278–288

[7] Zhao Q, Lee FC (2003) High-efficiency, high step-up DC–DC converters. IEEE Trans Power Electron 18(1):65–73

[8] Walker GR, Sernia PC (2004) Cascaded DC-DC converter connection of photovoltaic modules. IEEE Trans Power Electron 19(4):1130–1139

[9] Hsieh YP, Chen JF, Liang TJ et al (2012) Analysis and implementation of a novel single-switch high step-up DC–DC converter. IET Power Electron 5(1):11–21

[10] Wu TF, Lai YS, Hung JC et al (2008) Boost converter with coupled inductors and buck-boost type of active clamp. IEEE Trans Ind Electron 55(1):154–162

[11] Henn GAL, Silva RNAL, Praca PP et al (2010) Interleaved-boost converter with high voltage gain. IEEE Trans Power Electron 25(11):2753–2761

[12] Prudente JM, Pfitscher LL, Emmendoerfer G et al (2008) Voltage multiplier cells applied to non-isolated DC–DC converters. IEEE Trans Power Electron 23(2):871–887

[13] Tseng KC, Huang CC (2014) High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system. IEEE Trans Ind Electron 61(3):1311–1319

[14] Axelrod B, Berkovich Y, Ioinovici A (2008) Switched -capac-itor/switched-inductor structures for getting transformerless hybrid DC–DC PWM converters. IEEE Trans Circuits Syst I 55(2):687–696

[15] Berkovich Y, Axelrod B (2011) Switched-coupled inductor cell for DC–DC converters with large conversion ratio. IET Power Electron 4(3):309–315

[16] Tang Y, Fu DJ, Wang T et al (2015) Hybrid switched-inductor converters for high step-up conversion. IEEE Trans Ind Electron 62(3):1480–1490

[17] Ismail EH, Al-Saffar MA, Sabzali AJ et al (2008) A family of single-switch PWM converters with high step-up conversion ratio. IEEE Trans Circuits Syst I 55(4):1159–1171

[18] Luo FL, Ye H (2004) Positive output multiple-lift push-pull switched-capacitor Luo-converters. IEEE Trans Ind Electron 51(3):594–602

[19] Liang TJ, Chen SM, Yang LS et al (2012) Ultra-large gain step-up switched-capacitor DC–DC converter with coupled inductor for alternative sources of energy. IEEE Trans Circuits Syst I 59(4):864–874

[20] Wu G, Ruan XB, Ye ZH (2015) Non isolated high step-up DC-DC converters adopting switched-capacitor cell. IEEE Trans Ind Electron 61(1):383–393

[21] Tang Y, Wang T, He YH (2014) A switched-capacitor based active-network converter for high step-up conversion. IEEE Trans Power Electron 29(6):2959–2968

[22] Tang Y, Wang T, Fu DJ (2015) Multicell switched inductor / switched capacitor combined active network converters. IEEE Trans Power Electron 30(4):2063–2072

[23] Peng FZ (2003) Z-source inverter. IEEE Trans Ind Appl 39(2):504–510

[24] Tang Y, Xie SJ, Zhang CH et al (2009) Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability. IEEE Trans Power Electron 24(2):409–415

[25] Anderson J, Peng FZ (2008) Four quasi-Z-source inverters. In:Proceediings of IEEE power electronics specialists conference, Rhodes, Greece, 15–19 June 2008, 7pp

[26] Cao D, Peng FZ (2009) A family of Z-source and quasi-Z-source DC–DC converters. In:Proceediings of 24th annual IEEE applied power electronics

conference and exposition, Washington, DC, USA, 15–19 Feburay 2009, 5pp

[27] Zhu M, Yu K, Luo FL (2010) Switched inductor Z-source inverter. IEEE Trans. Power Electron. 25(8):2150–2158

[28] Li D, Loh PC, Zhu M et al (2013) Generalized multicell switched-inductor and switched-capacitor Z-source inverters. IEEE Trans Power Electron 28(2):837–848

[29] Li D, Loh PC, Zhu M et al (2013) Cascaded multicell trans-Z-source inverters. IEEE Trans Power Electron 28(2):826–836

[30] Galigekere VP, Kazimierczuk MK (2012) Analysis of PWM Z-source DC–DC converter in CCM for steady state. IEEE Trans Circuits Syst I 59(4):854–863

[31] Fang XP (2009) A novel Z-source DC–DC converter. In:Pro-ceediings of IEEE international conference on industrial tech-nology, Chengdu, China, 21–24 April 2008, 5pp

[32] Yang LQ, Qiu DY, ZhangB et al (2014) A modified Z-source DC–DC converter. In:Proceediings of 16th european conference on power electronics and applications (EPE'14-ECCE Europe), Lappeenranta, Finland, 26–28 August 2014, 10pp

BIOGRAPHIES

Neelam Lohitha received B.Tech. degree in ASIST Engg. College in Vijayawada, India in 2015. Currently she is student of M.Tech in Power Electronics & Drives at MVR College of Engineering and Technology, Paritala, Vijayawada, AP, India.

Kamal Kiran Tata received B.Tech. degree in PVPSIT in Vijayawada, India in 2004. He received M.Tech in Power Electronics & Drives at VIT University, Vellore, India in 2008. Currently he is working Asst. Prof. in MVR College of Engg. & Tech, Paritala. His current research interests is in power electronic SC converters and Inverters.