A Review of Multiplier using Feed through Logic

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Abstract-- *The low power and high performance design of VLSI circuit using a new CMOS logic family called feedthrough logic. Low power VLSI circuits have become important criteria for designing the energy efficient for high performance and portable devices. For designing the digital signal processing more efficient Multiplies are the main structure. Now a day's multiplier plays most important role in the microprocessor and the digital signal processor and many electronics devices. When the standard CMOS technologies is compared with the FTL arithmetic circuits it gives low and efficient power. The circuit which consist large critical path and cascaded inverting gates then FTL is more convenient for design. The FTL circuit has low dynamic power consumption. The simulation of this circuit is carried out on CMOS process technology.*

Keywords: Multiplier, Feedthrough logic (FTL) dynamic CMOS logic, low power adder, CMOS logic circuit.

I. INTRODUCTION

Today Multipliers plays an important role in digital signal processing and different applications. Such as microprocessor, DSP these are the high performance circuit etc. which are design by using addition and multiplication of two binary numbers and used for arithmetic operations. More than 70% instructions in microprocessors and DSP algorithm perform on addition and multiplication [7].

So, these operation dominates the execution time. So, there is need of high speed multiplier. Nowadays there is demand of high speed processing and power consumptions device i.e. computers and signal processing application are increased [9].

A new logic family is introduced known as feedthrough logic [5] which improves the performance of logic circuits basically for having long logic depth with reduced power dissipation [6].This logic works properly with domino concept for cascaded logic, differential style and multiple output with iterative networks has shown high design flexibility with the feature of partial evaluation of output before getting a valid input. This feature results in very fast evaluation of output in computational block [10].

II. DYNAMIC CIRCUIT

Dynamic circuits have high performance and low power consumption than static CMOS[1,2] which are being increasingly used due to their compactness and introduction of pre charge and evaluation phase using clock. However excessive power dissipation due to switching and clock activities, less noise margin due to charge leakage and charge sharing and requirement of additional inverter for cascading are the major drawbacks of this logic circuit. In order to reduce excessive power dissipation in dynamic gate various power gating techniques such as dual supply voltage and dual threshold voltage [3, 4] are prosed in the literature.

Major advantage of feedthrough logic [5] is which does not require any additional circuits like keeper circuits for the reduction of leakage power and FTL can be cascaded without the use of inverters. In this paper a modified FTL based dynamic circuit is proposed for improved power reduction and better performance.

The power dissipation in CMOS logic is given by

P total = P static + P dynamic + P short circuit

Total power is the sum of static, dynamic and short circuit power. Static power means the power dissipated when the power supply is on. It is equivalent to the product of supply voltage and leakage current. Dynamic power is the power dissipated due switching activity. Dynamic power of a logic circuit is proportional to capacitance of the node, total swing of voltage and switching activity. Short circuit power is the power dissipated due to short circuit current from supply voltage to ground. It is equal to the product of supply voltage and total short circuit current in that network [10].

III. BASIC FTL PRINCIPLE

The basic structure of FTL is shown in Figure 1. It consist a NMOS reset transistor Tm for resetting the output node to low logic level, a pull up PMOS load transistor ***Ts*** and an NMOS block. ***Ts*** and ***Tm*** controlled by the clock signal CLK. The basic principle of operation of a FTL circuit was presented in [3] and is briefed here. When CLK is high i.e. reset phase, ***Tm*** turned on and the output node pulled to ground through ***Tm***. When CLK goes low i.e. evaluation phase ***Tm*** is turned off and the output node conditionally evaluates to logic high i.e. V_{OH} or low i.e. V_{OL} depending upon input to NMOS block. A long chain of inverter is designed using FTL structure. When CLK=1, all the output nodes are at logic zero. When CLK goes low, the output node of all inverters rises to the gate threshold voltage V_{TH}. At this point any small variation in the input node causes a fast variation in voltage at the output node.

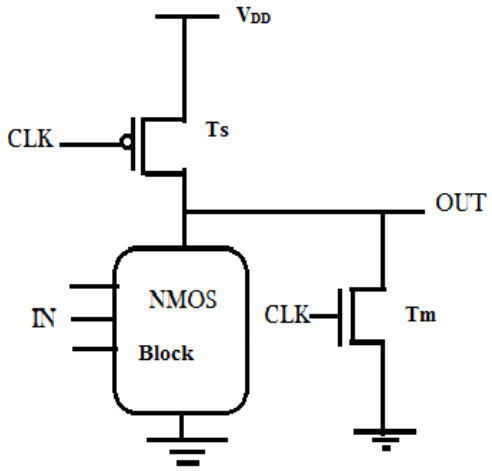

Figure 1: Feed through logic [9]

In the multiplier the low power consumption is more important issue while designing. To reducing dynamic power which is a major part of total power consumption so the need of high speed and low power multiplier has increased. Designer mainly concentrate on high speed and low power efficient circuit design. The main function of good multiplier is to provide high speed and low power consumption unit [9].

IV. METHODOLOGY

In this, the multiplier will be design by using new approach i.e. feed through logic. All the proposed multiplier are design through the new concept i.e. FTL for the low power and efficient energy. Our main focus area will be the power optimization in CMOS design circuit as it is the need of today's world. The design of multiplier using FTL is under process and the complete flow chart of the designing process is shown in Figure 2.

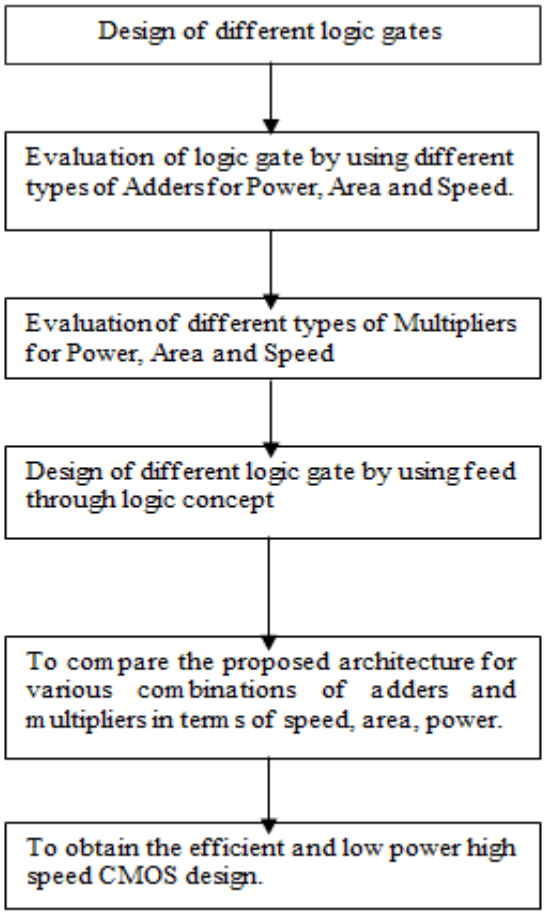

Figure 2: Flow chart

V. CONCLUSION

The outcomes of the proposed research work may have several applications in the field of microprocessors digital signal processing units and different electronics equipment's. In these applications the addition and 2-bit, 4-bit and 8-bit multiplication will be often used. The proposed work will be used to design the low power multiplier. Multiple optimization technique will be incorporated to reduce the power consumption and to increase the energy. Reduction of power will help to increase the performance of the CMOS circuit. In this way, FTL logic plays important role in reducing the dynamic power of CMOS circuits.

Applications-

1. Increased the speed of microprocessors and different DSP processors.

2. Proposed logic will helps in designing. Low power and high speed and efficient energy for the multiplication.

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