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FPGA Based Implementation of Decimator Filter for Hearing Aid Application

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Abstract - *The design of decimator filter requires a set of filters for hearing aid applications that gives reasonable signal for the concerned type of hearing loss. Using a variable bandwidth filter, helps a person with hearing loss to listen and communicate by making sounds audible and clearer. The design of variable bandwidth filter is carried out for a set of selected bandwidths. Each of these bands is frequency shifted and provided with sufficient magnitude gain, such that, the different bands combine to give a frequency response that closely matches with audiogram. The technique employed for the design of the filter is Canonic Signed Digit (CSD) representation. The higher sampling rate of the signal is decimated to low sampling rate by implementing the filter using the multi rate approach. The two FPGA devices can be used Spartan-3E and Virtex 2Pro. Furthermore, multi rate filtering method is used to attain high-resolution. It may reduce the complexity of the circuit and also the overall power consumed.*

Key Words: Decimation filter, CIC filter, FIR Filter, FPGA, Half Band filter, MATLAB, Xilinx.

1. INTRODUCTION

A Field Programmable Gate Arrays or FPGAs are based around a matrix of configurable logic blocks (CLBs]. It is an integrated circuit that may be programmed or reprogrammed to the desired capability or software after manufacturing. Important characteristics of field-programmable gate arrays consist lower complexity, higher speed, programmable functions and volume designs. Nowadays, FPGAs as cost-effective integrated tools have many applications in the field of communication and a growing range of other areas. Using FPGAs for hardware acceleration in software defined radios (SDR) offers extensive processing power to realize promised portability of waveforms and re-configurability. The decimation filter (decimator) is one of the basic building blocks of a sampling rate conversion system. The decimation filter performs two types of operations: low-pass filtering as well as down sampling. The filter converts low resolution high bit-rate data to high resolution low frequency data. It is mostly used in such applications as speech processing, radar systems, antenna systems and communication systems. Considerable attention has been focused in the previous years on the design of high efficiency decimation filters. The decimation process requires a low-pass filter of high quality and a sampling rate converter that helps to reduce the sampling frequency to a low level. A hearing aid is helpful for the people having hearing loss to hear more precisely in both quiet and whirring situations.

It helps a person with hearing loss to listen and communicate by making sounds audible and clearer. The minimum frequency of a person hearing is usually considered to be 20 Hz whereas the maximum limit is 20 kHz, but the ear is more sensible to audio from 1 KHz to 4 KHz. Thus, it is beneficial to design a deaf aid application that operates in the desired range of frequency and makes use of oversampling concept. Furthermore, multi rate filtering method is used to attain high-resolution. It can reduce the complexity of the circuit and also the overall power consumed. There are two important parameters which effects hearing. One is loudness that is the intensity of sound and the other one is pitch, which is the frequency of the fundamental component in the sound.

In 1981, Eugene Hogenauer invented a new class of economical digital filters for decimation and interpolation (converting the sampling rate from low to high) called a cascaded integrator comb (CIC) filter. This filter was composed of an integrator part and comb part. It then has experienced some modifications towards improvements in power consumption and frequency response. This filter is a combination of digital integrator and digital differentiator stages, which can perform the operation of digital low pass filtering and decimation at the same time. In this paper, we analyze the decimation filter using MATLAB and then performing stimulation with Xilinx ISE or Quartus II.

2. LITERATURE REVIEW

From the last few years, there has been a vast growth in the field of VLSI, Optimized decimation filters for wireless communication receivers based on FPGA is use by Vennached Karunakeroud [1], concluded poly phase required more area in comparison with CIC based filter and for both the decimation and interpolation, CIC filters are used multi-rate digital signal processing. Number of signal processing algorithm have been developed by Siddharth Raghuvanshi [2], which allow the user to focusing on real time signals such as speech to convert the signal with desired quality. The digital hearing aids are performed on Application Specific Integrated Circuit (ASIC) , not only the efficiency and

complexity of Hearing aid increases but also required more space and because implementation of hearing aid in digital is not interesting task and more power consuming also on ASIC. Stephen Colaco explains the decimator filter for audio application using canonic signed digit (CSD) representation. The use of the CSD multiplier design results in a multiplier less solution to digital filters, where the complexity of design is a function of the number of non-zero digits in the filter coefficients. This method has less power consumption as well as reducing the cost. R. Mehra [4] gives an easy way to measure high speed CIC decimator for wireless applications using software defined radios. Expensive anti-aliasing analog filters are getting reduces and performing different types of signals with different sampling rates. For the operation of additions/subtractions, the Cascaded Integrator comb used decimation filter which performed sample rate conversion (SRC). L. Singh [5] In this paper, FPGA's possess a very attractive solution for more flexibility, time-to-market, performance and cost. Vivek Venugopal [6] performed the filtering at a high rate and also implemented the decimation filter with the help of canonic signed digit (CSD) way. Oversampling concept is used as well as sigma delta analog to digital converters is done in hearing aid application. Abdul Rehman Buzdar [7] used a various digital signal processing technique in hearing aid such as Wavelet Transforms, uniform and non-uniform filter bank and Fast Fourier Transform (FFT). In uniform filter banks all the filters have equal bandwidth and use a input signal sampled at the same frequency, actually it is a group of band pass as well as high pass filter. In this paper, it achieved acceleration and also implementing echo cancellation, noise reduction adaptive filtering to make hearing aid work better. Divya Naga Padmini P [8] represents different ways of realizing half-band FIR low pass filter and provides comparison of critical path delay and clock frequencies for direct form, transposed form and DA (Distributed Arithmetic) type of architectures, In this paper, because of using multipliers which gives rise to few demerits in terms of increase in area and increase in the delay which ultimately results in less performance. To resolve this issue, DAA (Distributed Arithmetic Architecture) is used which is a popular method for implementing digital FIR filters on FPGAs through which delay can be reduced and multiplier less realization can be achieved. Vishal Awasthi [9] explains data rate conversion as well as filtering. In this paper, it consists of three classes of filters FIR, IIR and CIC filters. IIR filters are easy to realize but do not satisfy linear phase requirements which are required in time sensitive features like a video or a speech. FIR filters have a well defined frequency response but they need lot of hardware to store the filter coefficients. CIC filters overcome this drawback they are coefficient less so hardware requirement is much reduced but as they don't have well defined frequency response. So another structure is an implement which takes advantage of good feature of both the structures and thus have a cascade of CIC and FIR filters.

3. SYSTEM WORK

In digital signal processing, decimation is the process of reducing the sampling rate of a signal. The term down sampling usually refers to one step of the process, but sometimes the terms are used interchangeably. Complementary to up sampling, which increases sampling rate, decimation is a specific case of sample rate conversion in a multi-rate digital signal processing system. A system component that performs decimation is called a decimator. The block diagram of decimation filter is as follows:

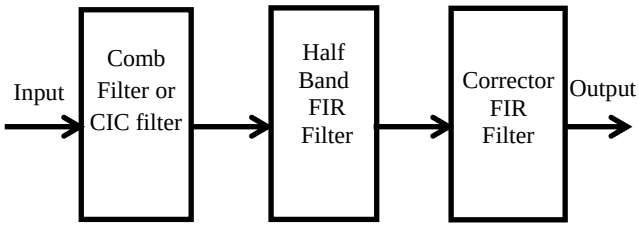

Figure 1: Block diagram of decimation filter

- The CIC Filter: The sampling rate is converted from low to high is called a cascaded integrator comb (CIC) filter. The comb filters do not need any multipliers and hence includes simple functions that are desirable at high frequencies. The response of the comb filter is a low pass filter with a distinct cutoff.

- Design half band FIR filter: Half-band filter is a fundamental building block in multi rate signal processing. Half-band filters are mostly used for their efficiency in multi-rate applications. The two important characteristics of Half band filters are pass band and stop band, the ripples of these band must be the same, and the pass band-edge and stop band-edge frequencies are equal distance from the half band frequency.

- Using Corrector Filter: Corrector filter is used for removing the unwanted signals. Digital filters with finite-duration impulse response (all-zero, or FIR filters) have the advantages are exactly linear phase, always stable as well as the filter startup transients have finite duration.

These filters are designed using two forms as Direct Form and Direct Form Symmetric. The FIR Direct Form structure is the most straightforward structure from a filter transfer function perspective. The figure 2 shows the FIR Direct Form structure.

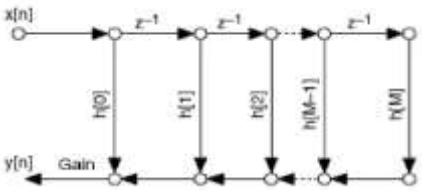

Figure 2: Direct Form Realization of FIR Filter.

The FIR Direct Form Transposed structure is the alternate direct form implementation for FIR filters. The figure 3 shows the FIR Direct Form Transposed structure. It has better timing performance because the delays following the adders in this structure can store the summation results temporarily for performing the summations in parallel.

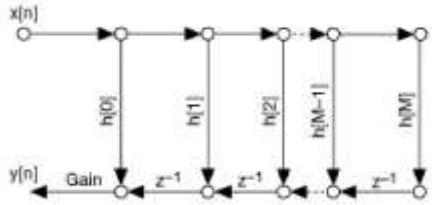

Figure 3: Transposed Form Realization of FIR Filter

This is the FPGA based project; to implement it MATLAB is used for getting coefficients and MODELSIM for simulation purpose. MODELSIM increases design quality and debug productivity. Finally it implemented in XILINX for synthesis. Xilinx's algorithms for synthesis allow designs to run up to 30% faster than competing programs, and allows greater logic density which reduces project time and costs.

Xilinx allows different FPGA platform due to which we can test the program and finding better hardware for implement it in real time. Xilinx provide different specifications or parameters such as number of slice's Registers, number of slice LUTS, Number of Fully Used LUT-FF pairs, Number of Bonded IOBs, Number of BUFG/BUFGCTRs and Timing Analysis as per programming code. This project is implemented on Spartan 3E, Virtex 4 and Spartan 6.

4. RESULTS

The table 1 shows the resources used by Spartan-6E for two form of FIR structure that is direct form and direct form symmetric. Also the code is test on Spartan-3E and Virtex 4.

Table 1: Resource Utilization of Spartan-6

Structure of filter		Direct Form	Direct Form Symmetric
Sr. no.	Logic Utilization	Used/Available	Used/Available
1.	Number of Slices	49/54576	64/54576
2.	Number of Flip Flop's	43/177	20/402
3.	Number of LUT's	171/27288	358/27288
4.	Number of Bonded IOBs	25/296	25/296
5.	Speed in MHz	269.513MHz	69.499MHz

The Table 2 reflects the comparison of resource utilization of Spartan 3E, Virtex 4 and Spartan 6 of direct form and direct form symmetric.

Table 2: Comparison of Resource Utilization of Direct Form and Direct Symmetric Form

Structure of filter		Direct Form			Direct Form Symmetric		
Sr No.	Logic Utilization	Spartan 3E	Virtex 4	Spartan 6	Spartan 3E	Virtex 4	Spartan 6
1.	Number of Slices	99	95	49	337	333	64
2.	Number of Flip Flop's	50	50	43	64	64	20
3.	Number of LUT's	186	178	171	647	637	358
4.	Number of Bonded IOBs	25	25	25	25	25	25
5.	Speed in MHz	144.21	222.79	269.53	29.500	48.90	69.499

```
Design Specifications
Sampling Frequency : 3.25 MHz
Response           : CIC Compensator
Specification      : Fp,Fst,Ap,Ast
Number0fSections   : 5
DifferentialDelay  : 1
Passband Edge      : 500 kHz
Stopband Edge      : 1.625 MHz
Passband Ripple    : 0.005 dB
Stopband Atten.    : 66 dB

Measurements
Sampling Frequency : 3.25 MHz
Passband Edge      : 500 kHz
3-dB Point         : 1.4996 MHz
6-dB Point         : 1.5376 MHz
Stopband Edge      : 1.625 MHz
Passband Ripple    : 0.00072786 dB
Stopband Atten.    : 307.8477 dB
Transition Width   : 1.125 MHz
```

Figure 4: Design Specification of CIC Filter.

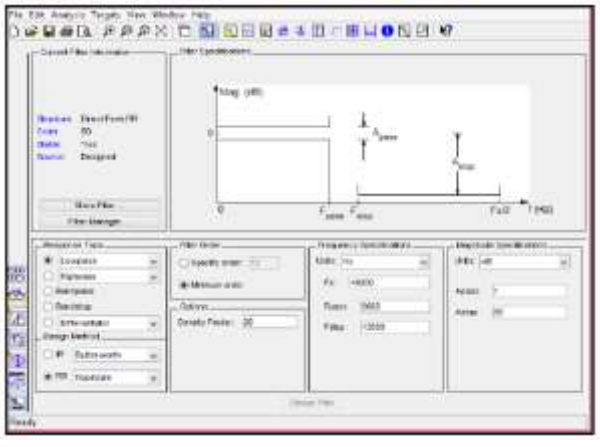

Figure 5: Filter Specification in Matlab

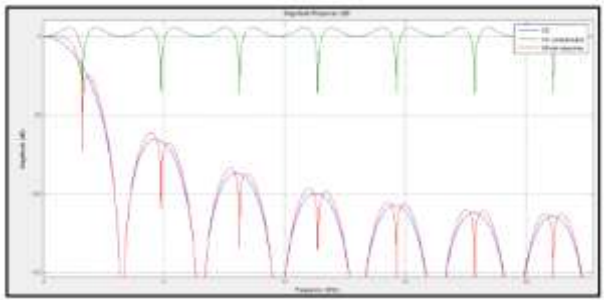

Figure 6: Analysis of CIC Filter.

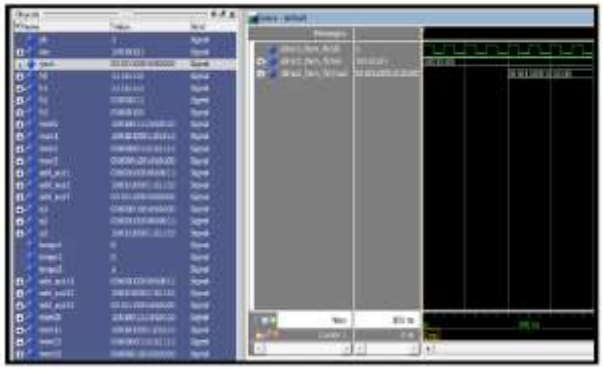

Figure 6: Modelsim Simulation of Direct Form Transponse.

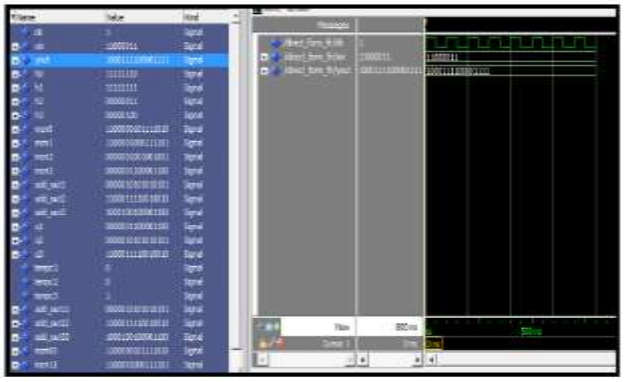

Figure 7: Modelsim Simulation Direct Form of Symmetric

Figure 8: Synthesis Output of Direct Form Transpose of Spartan 6.

```
Clock Information:
------------------
+---------------------------------+-------------------------+-------+
| Clock Signal                    | Clock buffer(FF name)   | Load  |
+---------------------------------+-------------------------+-------+
| Clk                             | BUFGP                   | 49    |
+---------------------------------+-------------------------+-------+

Asynchronous Control Signals Information:
-----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 3.710ns (Maximum Frequency: 269.513MHz)
   Minimum input arrival time before clock: 7.863ns
   Maximum output required time after clock: 3.597ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

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Figure 9: Timing Analysis of Direct Form Transpose of Spartan 6.

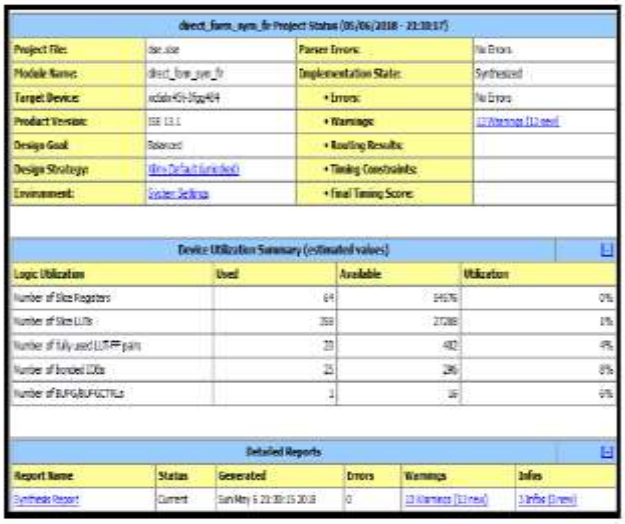

Figure 10: Synthesis Output of Direct Form Symmetric in Xilinx.

Figure 11: Timing Analysis of Direct Form Symmetric in Xilinx.

5. APPLICATIONS

1. Used in Military, Forensic area etc.

2. For amplify the signal and also reduce the sampling frequency to a low level.

3. A hearing aid is helpful for the people having hearing loss to hear more precisely in both quiet and whirring situations.

6. CONCLUSION

In this project, design analysis of decimation filter on FPGA is presented. The filter coefficient analyzed in MATLAB and then, it is stimulated in MODELSIM and finally synthesized using Xilinx synthesized tool (ISE) on Spartan-6 target FPGA device. It is observed that Spartan-6 is faster than Spartan-3E and Virtex 4 in Direct Form structure and also faster in Direct Form Symmetric structure. Hence direct form FIR filter gives better speed and better resource utilization. The maximum delay in Spartan-6 is 3.597ns. The count of slices is 49 and LUTs is 171. Thus, from the overall analysis, it can be concluded that Spartan-6 in Direct Form structure of filter gives better results in terms of speed, timing analysis and resource utilization.

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