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A 2-Dimensional Optical Router for Optical Networks- on -Chip.

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Abstract *–ONoC (Optical Network -on -chip) based on on-chip optical interconnects and routers having significant bandwidth and power advantages. In this work , we design a non-blocking low power consumption and efficient 5*5 2-D Optical Router architecture based on mesh topology , X-Y Routing and parallelism techniques .Through such techniques , it is possible to reduce number of wavelength , routing elements and crosstalk, thereby reducing insertion loss and improving power consumption. The fabrication of a five-port optical router composed of fifteen microring-resonator-based switching elements, five optical waveguides and thirteen waveguide crossings. Hence, the obtain insertion loss is 0.65dB.*

Key Words: **Network-on-chip (NoC) , Optical Router, Micro-resonator.**

1.INTRODUCTION

NOCs (network-on- chip) is a emerging wireless communication subsystem on an integrated circuit .typically between intellectual property (IP) cores in a processors. Network on Chip gradually becomes the bottleneck of communication system. NoC concept is based on “route packets, not wires”. Each processing core is connected to a local router. All the routers, and the links interconnecting the routers, form the NoC. The communication between two processing cores in a NoC is very similar to that between two nodes in a computer network . As the demand of latency and bandwidth keep increasing, Optics is playing vital role in communication due to its high bandwidth, low bit-rate and low power consumption.

Optical NoCs are based on on-chip optical interconnect and routers having significant bandwidth and power advantages .ONoC is similar to the wavelength router, a light path is establish according to the shortest path and less congestion so that any data can be transmitted in the optical layer .Currently, most ONoC uses micro-resonator as the building block for optical communication which can work at very high speed. Thus transferring data at a scalable and tremendous speed which provide low latency and high bandwidth.

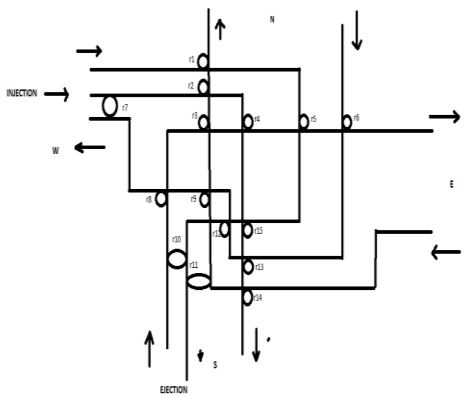
2. OPTICAL ROUTER

A Router is a backbone device for forwarding of data packets. The optical Router is based on the principle of Optical Fiber. Technology that carry the data at the speed of light i.e. to provide IP at a speed of light . We design a 5*5 Optical Router .

2.1 5*5 OPTICAL ROUTER

A 5*5 Optical Router is a non-blocking optical router. The five bidirectional ports include injection/ejection, east, south, west and north ports.

FIGURE 1: 5*5 2D OPTICAL ROUTER DESIGN



In the given figure 1 we can see that there are five bidirectional optical ports, including East, South, West, North and a local port (injection/ejection) which is connected to the O/E interface in 5*5 2d optical router design.

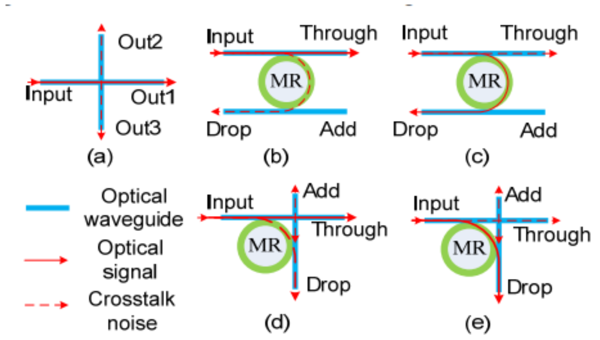
TABLE 1: ROUTING TABLE FOR 5*5 OPTICAL ROUTER

OUTPUT/INPUT	LOCAL	NORTH	EAST	SOUTH	WEST
LOCAL	---	R12	R11	R10	NONE
NORTH	R2	---	NONE	R3	R1
EAST	R4	R6	---	NONE	R5
SOUTH	NONE	R13	R14	---	R15
WEST	R7	NONE	R9	R8	---

The above table 1 shows that how data packets are being transferred from one port of optical router to the other with the help of MRs.When powered on, the MRs have an on-state resonance wavelength λon. While an optical signal with a centre wavelength λon comes into the input port, a powered-on MR will deliver the optical signal to the ejection port of the desired port;i.e they switch the input single to the desired destination port in on state as shown in figure 2.If MRs is in off state,then there will be no power consumption and signal will be delivered directly to the throughput port

Multiple basic switching elements may be combined together to implement predefined switching functions. By turning on/off MRs properly, the injected optical signal can be controlled to propagate from an input port to any output port.

FIGURE 2:Basic optical switching elements (a) Waveguide crossing (b) Parallel switching element in OFF state (c) Parallel switching element in ON state (d) Crossing switching element in OFF state (e) Crossing switching element in ON state

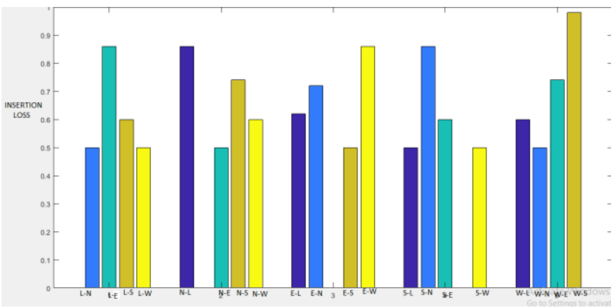


2.2 INSERTION LOSS

Insertion losses of an optical router decide its feasibility as well as the power consumption required by the O/E interfaces to generate, modulate, and detect optical signals. In our comparison, we considered two major sources of optical insertion losses, the waveguide crossing insertion loss andmicroresonator insertion loss. In our comparison, we considered two major sources of optical insertion losses, the waveguide crossing insertion loss and microresonator insertion loss. The microresonator insertion loss is 0.5dB . The insertion loss for each path is calculated by

I.L.=0.5*no. of on-State Micro-resonator+0.12*no. of crossing waveguide

FIGURE 3: Graph showing insertion loss for various ports



2.3 CROSSTALK

Crosstalk is also an important figure of merit of the optical router, which significantly limits the scalability of the photonic NoC employing such optical routers. Crosstalk of the optical router stems from the MRRs and the waveguide crossings. If PI is the power of the input optical signal, the output powers at Out1, Out2 and Out3 ports are PO1=LCPI and PO2=PO3=K1PI, where LC is the power loss per crossing and K1 is the crosstalk coefficient per crossing. PO2 and PO3 will become crosstalk noise when they are mixed with other optical signals. s. When the parallel switching element is in the OFF state, the output powers at the through and drop ports can be calculated as PT=LP1PI and PD=K2PI. While the parallel switching element is in the ON state, the output powers at the through and drop ports can be calculated as PT=K3PI and PD=LP2PI. The output powers of the crossing switching element in the OFF state can be calculated as PT=LC1PI, PD=(K2+L2 P1K1)PI, and PA=K1LP1PI. When it is in the ON state, the output powers can be expressed as PD=LC2PI, PT=LCK3PI, and PA=K1K3PI. PT, PD and PA are the output powers of the through, drop and add ports, respectively. LP1 is the power loss, and K2 is the crosstalk coefficient of the parallel switching element in the OFF state. LP2 and K3 are the power loss and crosstalk coefficient when the parallel switching element is in the ON state. LC1 is the power loss of the crossing switching element in the OFF state. LC2 is the power loss of crossing switching element in the ON state. When the crossing switching element is powered on, its crosstalk model is the same as the parallel switching element. The values of the losses and crosstalk coefficients are shown in Table 2 and 3.

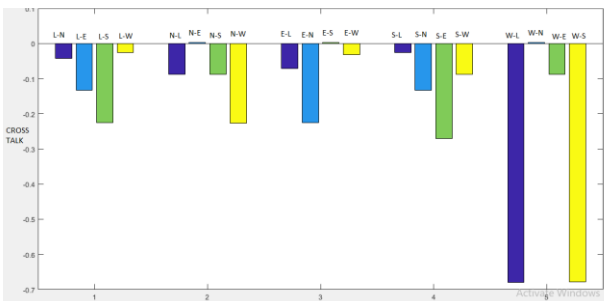
TABLE 2:OPTICAL POWER LOSSES

L_C	L_{C1}	L_{C2}	L_B	L_{P1}	L_{P2}
-0.12dB	-0.125dB	-0.5dB	-0.005dB/90°	-0.005dB	-0.5dB

TABLE 3: Crosstalk coefficients

K_1	K_2	K_3
-40dB	-45dB	-25dB

FIGURE 4:Graph showing crosstalk in db

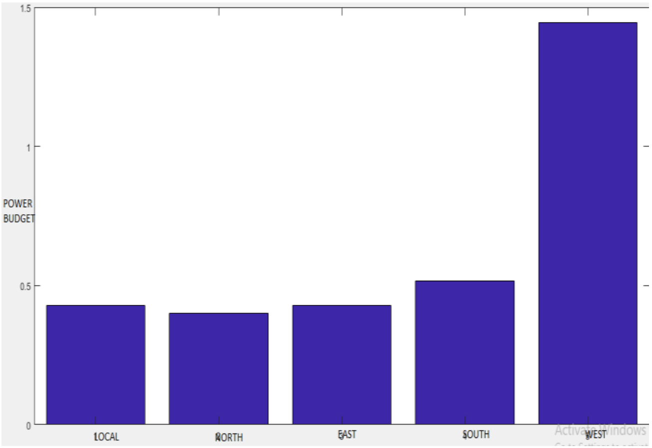


2.4 OPTICAL POWER BUDGET

It is the allocation of available optical power among various loss-producing mechanisms such as launch coupling loss, fiber attenuation,splice losses, and connector losses, in order to ensure that adequate signal strength (optical power) is available at the receiver. In optical power budget attenuation is specified in decibel (dB) and optical power in dBm.It can be determined by,

P(budget)=P(injected)-P(extracted) (dB)

FIGURE 5: Graph showing power budget



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3. CONCLUSIONS

This paper proposed a low power 5*5 2-dimensional optical router which uses optical characterstics as a center of attraction for doing communication due to which the latency and power dissipation reduced and the growing demand of high bandwidth is overcome.The architecture of the 5*5 Optical Router we designed is having insertion loss of about 0.64dB.

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REFERENCES

[1] L. Benini, G. De Micheli, “Networks on chip: A new paradigm for systems on chip design”, Design, Automation and Test in Europe Conference and Exhibition, 2002.

[2] S. Li, L. Peh, A. Kumar, and N. K. Jha, "Temperature-Aware On-Chip Networks," IEEE Micro, vol. 26, pp. 130-139, 2006.

[3] J. Henkel, W. Wolf, S. T. Chakradhar, “On-chip networks: A scalable, communication-centric embedded system design paradigm”, in Proc. 17th International Conference on VLSI Design, 2004.

[4] S. Kumar, A. Jantsch, J.P. Soininen, M. Forsell, M. Millberg, J. Öberg, K. Tiensyrjä, and A. Hemani, “A network on chip architecture and design methodology”, IEEE Computer Society Annual Symposium on VLSI, 2002.

[5] J. Xu, W. Wolf, J. Henkel, and S. Chakradhar, “A Design Methodology for Application-Specific Networks-on-Chip”, ACM Transactions on Embedded Computing Systems, July 2006.

[6] K. Goossens, J. Dielissen, A. Radulescu, “Æthereal network on chip: Concepts, architectures and implementations”, IEEE Design Test Comput, Vol.22, No.5, pp414–421. 2005..

[7] K. Srinivasan, K. S. Chatha, and G. Konjevod, "Application Specific Network-on-Chip Design with Guaranteed Quality Approximation Algorithms," Asia and South Pacific Design Automation Conference, pp. 184-190, 2007.

[8] M. Haurylau, G. Chen, H. Chen, J. Zhang, N.A. Nelson, D.H. Albonesi, E.G. Friedman, P.M. Fauchet, "On-Chip Optical Interconnect Roadmap: Challenges and Critical Directions," IEEE Journal of Selected Topics in Quantum Electronics, vol.12, no.6, pp.1699-1705, 2006.