A Novel Topology for Multilevel Inverters with Reduced Device Count

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Abstract – Currently multilevel converter structures have been rising since last few decades because it consists of lesser number of power switches and DC sources. Research of multilevel inverter (MLI) has always been a noteworthy inspiration to increasing number of levels with decreasing total harmonic distortion (THD). Multilevel converter topology conjoins the stepped waveform to produce waveform approximation of sine waveform. In this paper, an optimal structure of novel dc source converter configuration with less switch count is introduced. Comparison results prove that the presented cascade topology requires fewer numbers of components. Multicarrier pulse width modulation techniques are adopted for firing the gate pulses of the switches. The operation of the proposed topology is explained with 31-level output voltage. The simulation results are carried out by using MATLAB/Simulink software package.

Index terms – Multilevel inverter, PWM, asymmetric

I. INTRODUCTION

Multilevel inverter has become popular in industries and electric drive. It is best suited for medium to high power applications [1]-[3]. Multilevel inverter synthesizes desired stepped voltage waveform by arranging power switches and lower DC voltages. Multilevel inverter synthesizes stepped waveform to a near sinusoidal waveform with low harmonic distortion and low stress. Main advantage of multilevel inverter is that as the number of voltage level increases, stepped output waveform approaches to a near sinusoidal voltage or current waveform and harmonic distortion decreases [4]. There are three types of most popular topology, Neutral point clamped multilevel inverter topology, flying capacitor multilevel inverter topology and Cascaded H-Bridge multilevel inverter topology [5]. Cascaded H-bridge topology is very efficient due to its modularity and simplicity [6]. Neutral Point clamped topology uses many diodes to clamp the DC bus Voltage. As increase the number of voltage level, complexity of the neutral point clamped inverter increases [7]. Similarly, flying capacitor multilevel inverter topology has the many number of capacitors for charging and discharging. It is difficult to balancing the charging and discharging controlling of inverter due to this problem [8]. Cascaded multilevel inverters are best suited for many numbers of voltage levels and complexity does not increase more. Cascaded H-bridge multilevel inverter uses large number of isolated DC sources required to supply voltage to each H-bridge cell [9]. To overcome this difficulties many new topology are presented. Multilevel inverter topology required large high semiconductor power switches due to which complexity and cost of power converter increases [10]. To reduce power switches and complexity many new topologies with reduced number of switches and DC sources have been presented [10]-[13].

In order to increase the number of output voltage levels, the magnitudes of dc voltage sources are selected to be different, these topologies are called asymmetric [8-9]. Reducing the stress on power switches and fault-tolerant operations, extendibility, modularization, simplicity of control and high reliability are some of main advantages of these inverters in comparison with two other basic topologies of multilevel inverters. However, high number of required dc voltage sources and semiconductor power switches by increasing the number of generated output levels are disadvantageous of this inverter [10-12].

In this paper, in order to increase the number of output levels by using lower number of power electronic switches a novel unit is proposed. In order to generate all positive and negative levels at the output, two algorithms to determine the magnitude of dc voltage sources are proposed. The proposed inverter is compared with several conventional cascaded multilevel inverters to investigate its advantages and disadvantages. Finally, the accuracy performance of the proposed inverter is reconfirmed by using simulation results on proposed 31-level converter.

II. Proposed structure of 31-level MLI

The structure of the proposed basic unit is presented in Fig. 1. This circuit consists of six unidirectional switches (K_1, K_2, K_3, K_4, S_a, S_b), four bidirectional switches (S_1, S_2, T_1, T2), and six dc sources. Three of the dc sources have the same magnitude of V_{dc} and the value of the three other sources is $4V_{dc}$. The switching states of the unit proposed to generate all levels are provided in Table I. As shown in this Fig.1, the unidirectional and bidirectional power switches are used in the basic unit. Each unidirectional power switch consists of an IGBT with an anti-parallel diode as a common emitter

configuration that is able to conduct current in both direction and block voltage in one polarity. While, the bidirectional power switches include of two IGBTs with two anti-parallel diodes that conducts current in both direction and blocks voltage with both positive and negative polarities. Fig.2 show the basic configuration of the switches used.

To obtain the maximum number of levels with constant number of power electronic elements, two algorithms are described for determining the values of sources of MLI structure as follows.

A. First Algorithm

In this algorithm, the values of sources in the proposed MLI structure are similar and the maximum nine-level voltage output can be obtained. However, the values of sources in various MLIs are non-equal and are obtained using the following equations.

$$E_{11} = E_{12} = \ldots\ldots = E_{1n} = E_{21} = E_{22} \ldots\ldots\ldots\ldots E_{2n} = V_{dc} \quad (1)$$

Then, the maximum amplitude of the output voltage in the MLI ($V_{o,max}$) will be

$$V_{o,max} = n\, V_{dc} \quad (2)$$

Where 'n' is the number of sources used in the proposed structure.

B. Second Algorithm

In contrast to the described first algorithm, the values of dc sources of proposed MLI are equal. In fact, the dc sources amplitudes of each have two different values which are determined as follows:

$$E_{11} = E_{12} = E_{13} = E_{1n} = V_{dc} \text{ and } E_{21} = E_{22} = E_{23} = E_{2n} = 4V_{dc} \quad (3)$$

The maximum output voltage of the MLI ($V_{o,max}$) is

$$V_{o,max} = (nE_{1n} + nE_{2n})\, V_{dc} \quad (4)$$

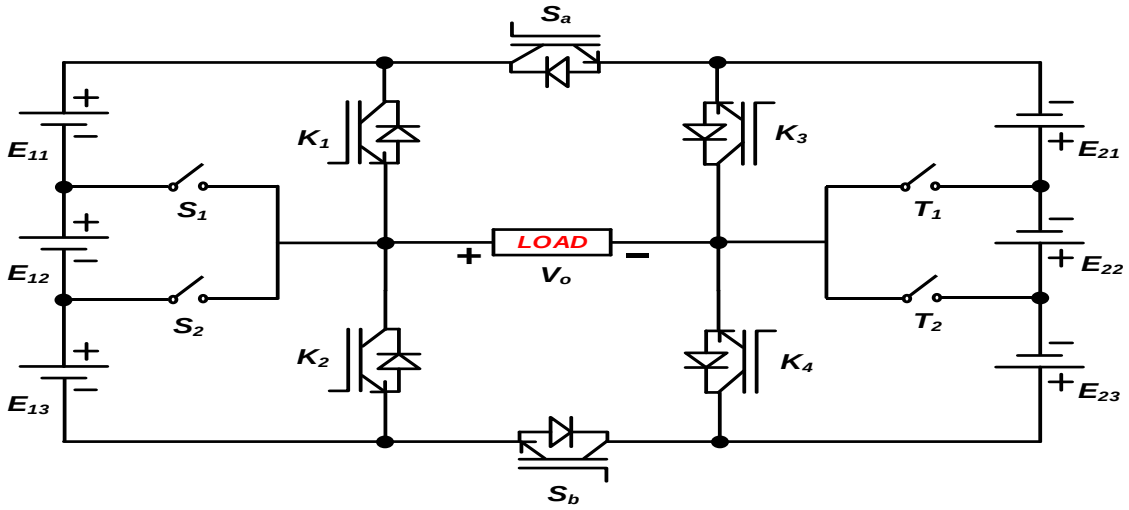


Fig.1 A 31-level inverter topology based on the illustrated second algorithm.

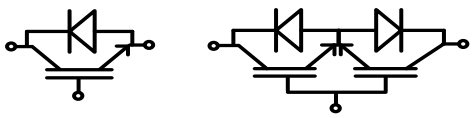


Fig.2 Switching configurations used in the proposed structure

Table I

Valid switching states for the structure proposed

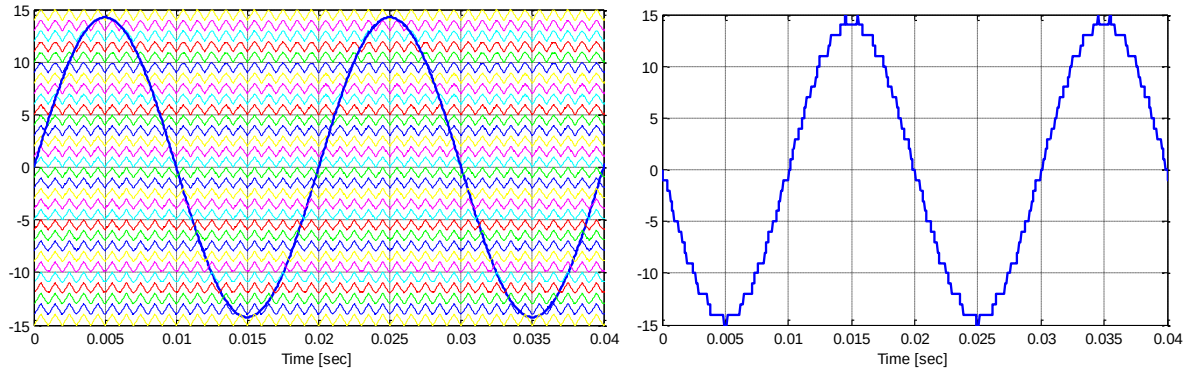
Modes	On State Switches	Output Voltage [$V_o(t)$]	$E_1 = E_2 = E_3 = V_{dc} = 25V$ $E_4 = E_5 = E_6 = 4V_{dc} = 100V$
M1	K_1, S_b, K_3	375	$E_1+E_2+E_3+E_4+E_5+E_6$
M2	S_1, S_b, K_3	350	$E_2+E_3+E_4+E_5+E_6$
M3	S_2, S_b, K_3	325	$E_3+E_4+E_5+E_6$
M4	K_2, S_b, K_3	300	$E_4+E_5+E_6$
M5	K_1, S_b, T_1	275	$E_1+E_2+E_3+E_5+E_6$
M6	S_1, S_b, T_1	250	$E_2+E_3+E_5+E_6$
M7	S_2, S_b, T_1	225	$E_3+E_5+E_6$
M8	K_2, S_b, T_1	200	E_5+E_6
M9	K_1, S_b, T_2	175	$E_1+E_2+E_3+E_6$
M10	S_1, S_b, T_2	150	$E_2+E_3+E_6$
M11	S_2, S_b, T_2	125	E_3+E_6
M12	K_2, S_b, T_2	100	E_6
M13	K_1, S_b, K_4	75	$E_1+E_2+E_3$
M14	S_1, S_b, K_4	50	E_2+E_3
M15	S_2, S_b, K_4	25	E_3
M16	K_2, S_b, K_4 K_1, S_a, K_3	0	0
M17	S_1, S_a, K_3	-25	$-E_1$
M18	S_2, S_a, K_3	-50	$-(E_1+E_2)$
M19	K_2, S_a, K_3	-75	$-(E_1+E_2+E_3)$
M20	K_1, S_a, T_1	-100	$-E_4$
M21	S_1, S_a, T_1	-125	$-(E_1+E_4)$
M22	S_2, S_a, T_1	-150	$-(E_1+E_2+E_4)$
M23	K_2, S_a, T_1	-175	$-(E_1+E_2+E_3+E_4)$
M24	K_1, S_a, T_2	-200	$-(E_4+E_5)$
M25	S_1, S_a, T_2	-225	$-(E_1+E_4+E_5)$
M26	S_2, S_a, T_2	-250	$-(E_1+E_2+E_4+E_5)$
M27	K_2, S_a, T_2	-275	$-(E_1+E_2+E_3+E_4+E_5)$
M28	K_1, S_a, K_4	-300	$-(E_4+E_5+E_6)$
M29	S_1, S_a, K_4	-325	$-(E_1+E_4+E_5+E_6)$
M30	S_2, S_a, K_4	-350	$-(E_1+E_2+E_4+E_5+E_6)$
M31	K_2, S_a, K_4	-375	$-(E_1+E_2+E_3+E_4+E_5+E_6)$

III. Simulation Study And Comparison

In order to validate the functionality of the proposed structure, a simulation study is carried out using MATLAB/Simulink software package. The circuit shown in Fig.1 is modelled with asymmetric sources and the modulation strategy, a thirty-one level inverter with ten switches and six sources configured as $E_{11}= E_{21} = E_{31} = V_{DC}$, $E_{21} = E_{22} = E_{23} = 4V_{DC}$. The R–L load with the values of R = 120 Ω and L = 50 mH is used for the topology introduced in this work. Phase disposed triangular signals with frequency 1.7 kHz is employed as carriers and sinusoidal reference with frequency 50 Hz is used with an amplitude modulation index $M_a = 1$. The so-called 'universal control scheme' as proposed in [11] is used to modulate the proposed structure.

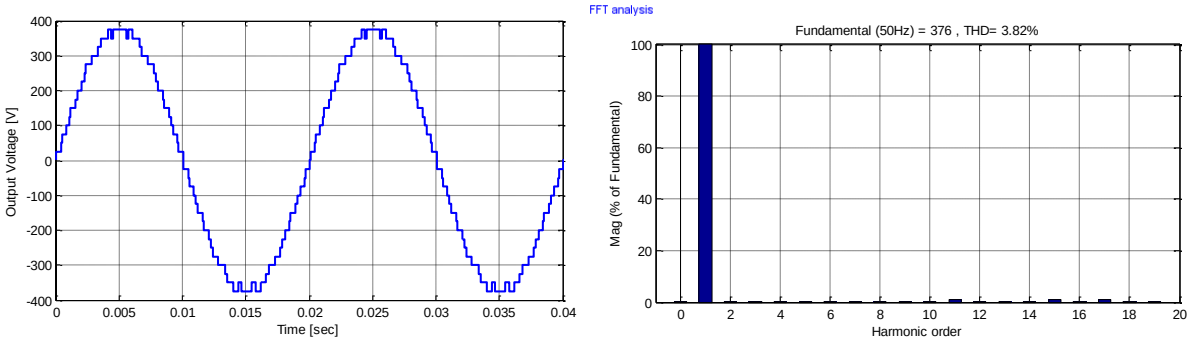
For a 31-level inverter, carrier and reference signals are shown in Fig. 2(a) and aggregated signal is depicted in Fig. 2(b).The load current waveform is sinusoidal and is inductive in nature as expected.

The output voltages and harmonic profile are shown in Fig.3.The value of output voltage frequency is 50 Hz. The output voltage waveform of 31-level inverter is indicated in Fig. 3(a). It is clear that the maximum output voltage is 375 V. It consists of equal sized steps of 25V each. According to figure 1, the levels are 0, ±25 V, ±50V, . . . , ±350 V, ±375 V. Fig. 3(b) shows the output current of the 31-level inverter. The load current waveform is sinusoidal and is inductive in nature as expected. Also, load current waveform and its harmonic spectrum are depicted in Fig.4 (a) and (b) respectively. The maximum voltage on bidirectional switches S_1 and S_2 is 50 V and maximum standing voltage on switches T_1 and T_2 is 200V.



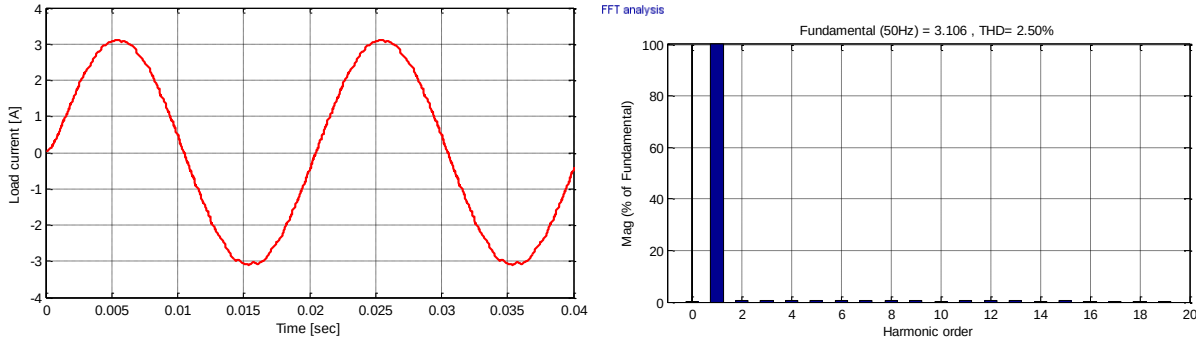
(a) **(b)**

Fig.2 (a) Reference and Carrier Waveforms, (b) Aggregated signal "a (t)"



(a) **(b)**

Fig.3 Simulated waveforms for 31-level inverter; (a) load voltage ($V_L(t)$) ; and (b) harmonic profile of load voltage



(a) **(b)**

Fig.4 (a) Load current waveform of 31-level CCCS-MLI with RL load (R = 120 Ω and L = 50 mH);

(b) Harmonic spectrum of load current

Table 2

Comparison of the proposed topology with classical and some recently introduced topologies

MLIs/Components	DCMLI	FCMLI	CHBMLI	Ref [8]	Ref [7]	Proposed MLI
Number of switches	60	60	60	12	12	10
Number of DC sources	1	1	15	4	4	6
Total number of output	31	31	31	31	31	31
Number of driver circuit	60	60	60	12	12	10
Clamping diodes	56	-	-	-	-	-
Clamping capacitors	-	28	-	-	-	-
DC bus capacitors	30	30	-	-	-	-

IV. Conclusion

In this paper, an optimal design of multilevel converter topology is investigated. Then, two different algorithms are proposed to determine the magnitudes of dc voltage sources. This power circuit uses lower number of power switches, diodes and driver circuits for a specific number of voltage levels in comparison with many of conventional multilevel inverters that have been presented in literature. THD is also reduced subsequently as per IEEE standard 519 without using filters i.e. 3.82%. Also a multicarrier PWM scheme is introduced which helps to optimize the switching frequencies of various power switches with different voltage stresses. Finally, all of the obtained theoretical issues are reconfirmed by using simulation results on a proposed 31-level inverter based on second proposed algorithm. The proposed configuration is used in high power applications like EV and HEV drives.

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