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Design of Charge Pump for PLL with Reduction in Current Mismatch and Variation having Improved Voltage Swing

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Abstract - *A charge pump circuit which provides low current inequality and current variation is designed in CMOS 180nm technology and supply voltage of 1.8 V using Cadence Virtuoso tool. This charge pump is fit for stumpy power applications of PLL. Current steering topology is used because it eliminates drawbacks of conventional charge pump. Feedback loop is used to revoke arbitrary and deterministic mismatch between Iup and Idn. Compensation circuit is used to decrease the current deviation to evade bandwidth variation and loop volatility. Proposed charge pump has current mismatch in range of 10%- 21%. Also get flat output current for output voltage variation of 0.514 V and output voltage swing is 1.525V.*

Key words: PLL, charge pump.

1. INTRODUCTION

As we all know that Phase Locked Loop (PLL) is very important unit of modern communication system. Hence design of all the blocks of PLL is very crucial. There are two type of PLL that is simple PLL and Charge Pump (CP) PLL in Fig 1 CP PLL is superior to simple PLL as it removes drawbacks of simple PLL like swapping between settling speed and swell on Voltage Control Oscillator (VCO) control line, phase error and restricted possession range [3].

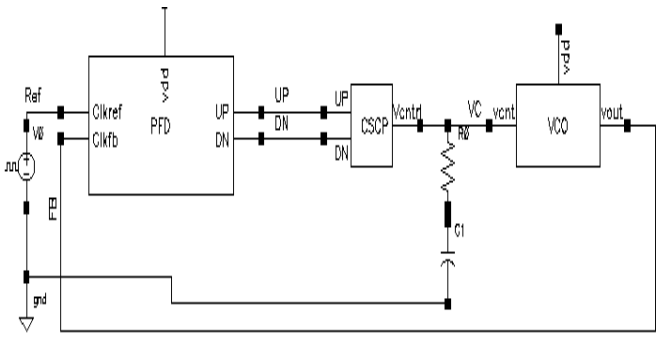


Fig 1 Basic block Diagram of PLL

CP PLL has following blocks Phase Frequency Detector (PFD), CP, Loop filter and VCO. Among these blocks performance of CP is directly affects the functionality of PLL. PLL used for clock generation and clock recovery. Implementation of charge pump is more Challenging as it is important block of PLL. CP operates on UP and DOWN (DN) output signal generated by PFD and converts phase and frequency difference between reference input and feedback input into equivalent output voltage. CP in PLL is followed with loop filter. Depending on status of UP and DN signal, CP charges and discharges loop filter. When reference signal leads feedback signal UP goes high hence CP charges the loop filter and vice versa. Voltage which is generated across loop filter is used as control voltage of VCO. The conventional CP has non idealities like charge division, charge insertion and clock feed through. These non idealities are removed by using current steering topology of charge pump as PMOS and NMOS switches are outlying as of output node. But Conventional Current Steering Charge Pump (CSCP) illustrate in Fig 2 also has some problem like current mismatch between I_{UP} and I_{DN} and current deviation with transform in output voltage. Mismatch between charging and discharging current is because charging current is source by PMOS and discharging current is sink by NMOS. So current source by PMOS is not exactly match with current sink by NOMS due to process variation and physical properties of PMOS and NMOS. Also a current variation is because channel length modulation effect of output transistors, which can be eliminated by using long transistors at output. On the other hand, long transistors can't utterly eradicate the consequences and large parasitic capacitance limits the speed and operation.

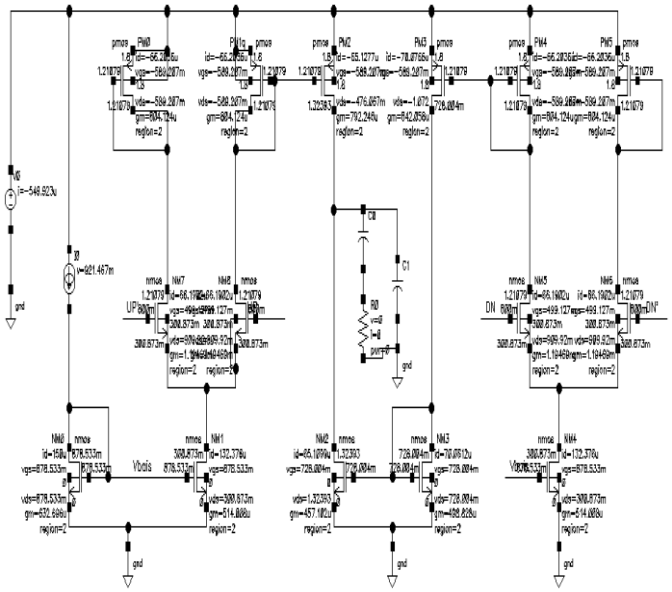
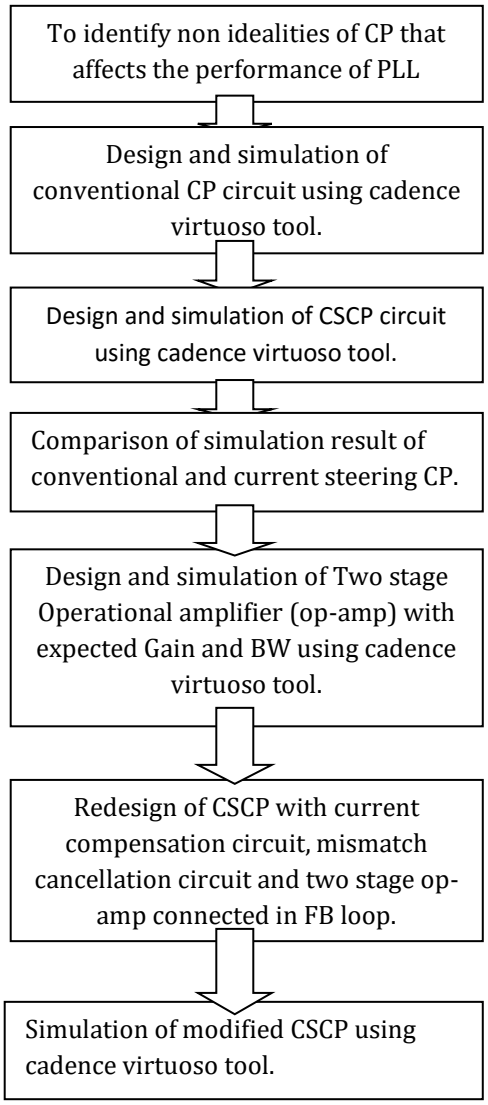


Fig 2 Schematic of CSCP

A current compensation circuit is used to broaden the smooth assortment of output voltage notably to curtail the current deviation. In some cases two compensation circuits are used to diminish current variance and current deviation. Gain-boosted charge pumps[9] use synchronized cascode to increase the output resistance for decreasing current deviation keeping the I_{UP} and I_{DN} currents just about steady with the driving voltage, but this lowers the voltage conformity range and a higher supply voltage is desired for appropriate action. Instead of this, in this paper new technique is used to reduce current mismatch.

2. DESIGN FLOW CHART:



2.1 Design issues of conventional charge pump:

1. **Saturation voltage: -** Saturation voltage of Current Source (CS) transistor should be low as it will be closer to rail the CP such that it operates properly. Without changing loop dynamics and loop dynamics [1].

$$VDS_{Sat} = \sqrt{\frac{2id(\frac{W}{L})}{\mu_n C_{ox}}} \qquad (1)$$

To get output voltage of CP closer to rail to rail W/L should be large and i_d should be low.

2. **CS output impedance:-** Difficulty with CS transistors in CP is that they have finite output resistance still in saturation [1]. Even if the currents are similar at mid rail they will not be entirely matched at all output voltages.

$$r_{ds} = \frac{1}{\lambda I_{DS}} \propto \frac{L}{I_{DS}} \qquad (2)$$

Difference in UP and DN current when output impedances are same and voltages [1] moves from mid rail.

$$\frac{\Delta I}{I_{DS}} \propto \frac{(V_{OCP} - V_M)}{L} \qquad (3)$$

V_{OCP} - CP output voltage
V_M - Mid rail voltage
So for purpose of current matching having long device is good.

3. **Reference Feed through: -** It can have an effect on how much time the CP must leftovers ON in the locked state [1].

$$\text{Spur}=20\log\{\frac{(\delta^2.\Delta I.K_{vco})}{4\pi.C_2}.[1+\frac{\Delta I}{I_{CP}}]\}\ \text{dBc} \qquad (4)$$

4. **Transistor Gain: -** The problem is that when the CP current source turns ON and OFF it take finite amount of time, this will increase current mismatch [1]. So it is best to match the transconductance of both the NMOS and PMOS current source.

$$g_m = \sqrt{2\mu c_{OX}(\frac{W}{L})I_{DS}} \qquad (5)$$

To improve matching it is best to scale the number of transistor and if possible to use a common layout.

2.2 Design of two stage op amp:

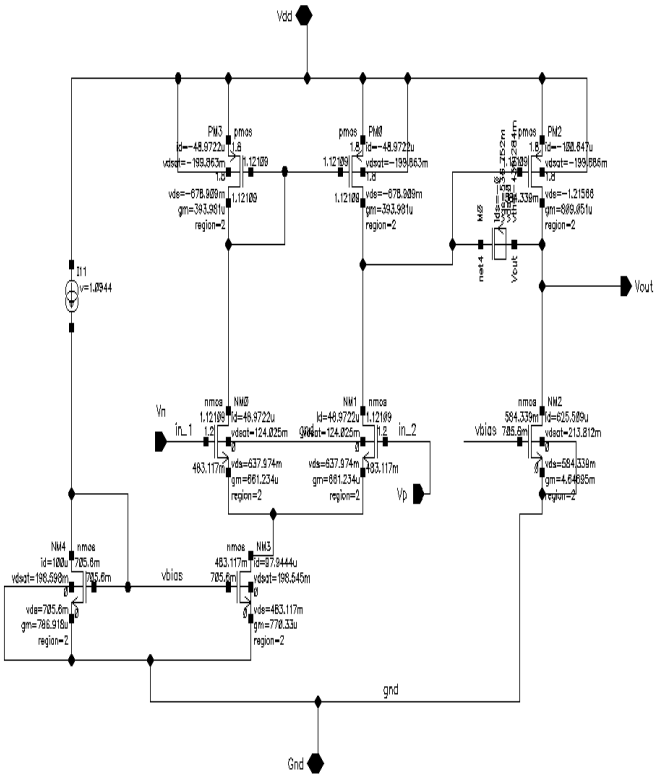


Fig 3 Schematic of two stage op amp

Two stage op amp made known in Fig 3 is designed in 180nm technology with 1.8V power supply using cadence virtuoso tool. The op amp has vital task in current matching. It should have sufficient gain to attain very low gain inaccuracy and due to this perfect matching between I_{UP} and I_{DN} currents. This op amp is used in a feedback loop of CSCP to reduce current mismatch. This op amp has gain approximately equal to 40dB and bandwidth equal to 3.4 MHz.

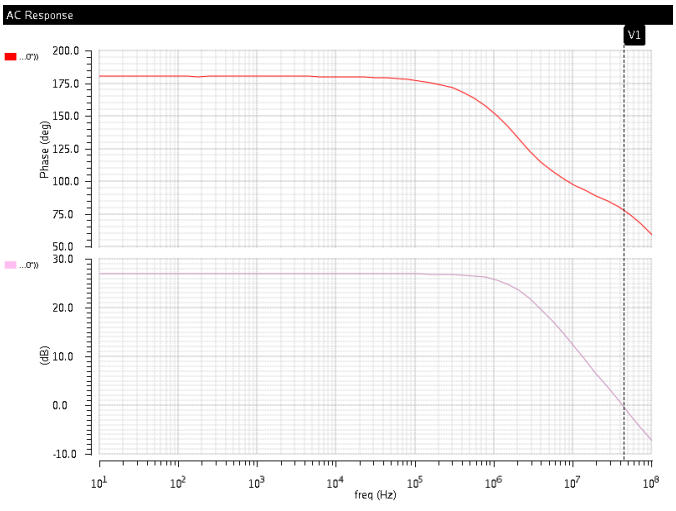


Fig 4 Gain and Phase plot of two stage op-amp

Table1. Results of two stage op amp

Sr. No.	Parameter	Values
1.	DC Gain	35.25 dB
2.	GBW	3.4MHz
3.	PM	61.09 deg
4.	Power	297 µW

3. Design of modified current steering charge pump

CP is only analog block in PLL architecture; hence design of charge pump has important part in PLL performance. This paper proposed a CP in Fig 5 with current compensation circuit and mismatch cancellation circuit. CP is designed with supply voltage in the range of 1.8 V to 3 V, V_{DSsat} ≥ 350mV and for the PLL with reference frequency 40MHz also having PFD feedback delay δ= 1ns and biasing current of 150µA.

Width of transistors at output stage is determined by following formula.

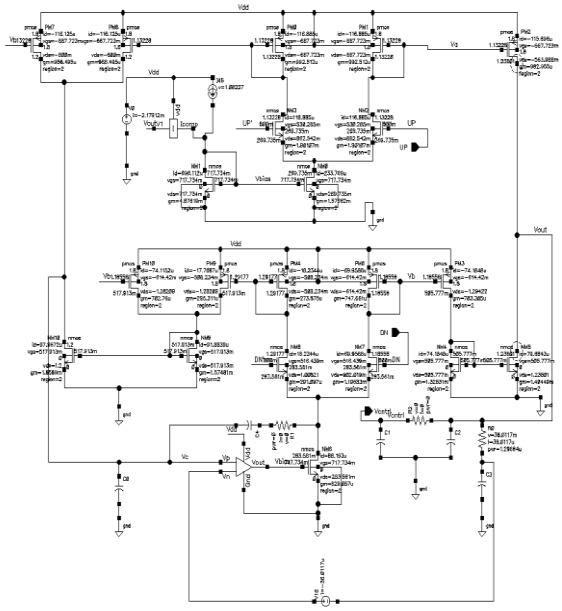


Fig 5 Schematic of modified CSCP

$$\frac{W}{L} = \frac{2I_D}{V_{DSsat}^2 \cdot \mu C_{ox}} \qquad (6)$$

For low 1/f noise contribution, length L kept between 2µm to 3µm.

If CS are mismatched by an quantity ΔI and retune path has a setback [1] of time δ then a charge q is placed on the loop filter where q is of value

$$q = \delta . \Delta I \qquad (7)$$

So it is necessary that another CS should be ON for a time 't' to take out the charge [1].

$$t = \frac{\delta . \Delta I}{I_{cp}} \qquad (8)$$

A circuit similar to charge pump in addition with an integrating capacitor C_x and an op amp are used in negative feedback loop for removing current mismatch [2]. Opamp compares voltage across C_x with average control voltage. Opamp output tune I_{DN} to follow variation in I_{UP}. Current compensation circuit contains transistors in triode region and current mirrors are used for removing current deviation [2]. This circuit is driven by output voltage of CP. The negative feedback loop must be steady for proper operation.

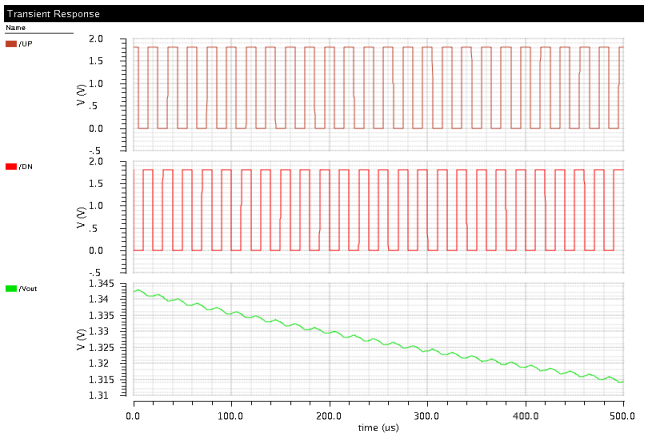


Fig 6 Transient analysis of CSCP

4. SIMULATION RESULTS

The projected CP circuit is designed in a180nm CMOS technology to be utilizing in a PLL with reference frequency 40MHz.

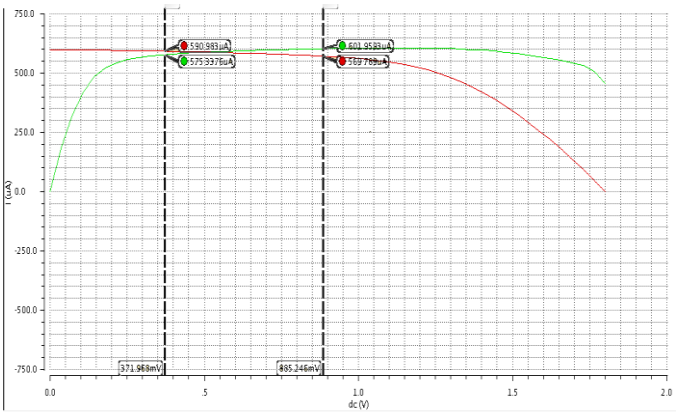


Fig 7 plot of I_{DN} and I_{UP} VS V_{ocp} of proposed CSCP

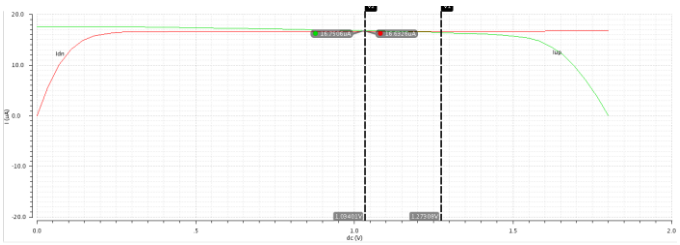


Fig 8 plot of I_{DN} and I_{UP} VS V_{ocp} of simple CP

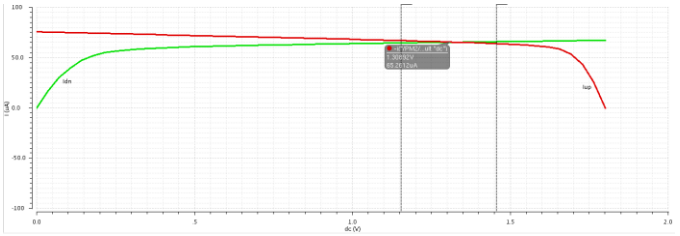


Fig 9 plot of I_{DN} and I_{UP} VS V_{ocp} Conventional CSCP

Proposed charge pump is biased with 150µA current and after simulation got current mismatch between I_{DN} and I_{UP} approximately in the range of 10% to 21%. I_{DN} And I_{UP} is matching for the output voltage varies from 371mV to 885mV. That is for 0.514V get flat output current with variation in output voltage of charge pump. Proposed charge pump circuit superior to simple charge pump and conventional CSCP charge pump. As output voltage swing, current variation with charge pump output voltage is improved. Also current mismatch is reduced.

Table2. Comparison of different CP circuits

Sr. No.	Circuit	Current mismatch	V_{ocp} range for low current variation	Output Voltage swing
1.	Simple CP	27% - 40%	239mV	0.63V to 242mV
2.	CSCP	15% - 25%	302mV	1.6V to 205mV
3.	Proposed CSCP	10% - 21%	514mV	1.609 to 84mV

5. CONCLUSION

Method of reduction in Current mismatch and variation of charge pump is presented which reduces deterministic and random current mismatch and improves current variation. Negative feedback tunes I_{DN} to any changes in I_{UP}, which reduce current mismatch. Eventually get current mismatch in very small amount. Also current variation is least with variation in output voltage of charge pump.

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