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Comparative study analysis of Z-source NPC & Z-source T NPC MLI using SVM

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Abstract: *Comparative analysis of a Z-source neutral point clamped inverter & Z Source -T shape - Neutral point Diode Clamped (NPC) - Multi Level Inverter (MLI) power conversion system (Z-T-NPC-MLI) using Space Vector PWM (SVPWM) is presented. This exploits the redundancy switching vector option for both shoot through (ST) and regular switching, which offers a self-control neutral point fluctuation. The conduction losses of the Z-T NPC-MLI are much lower when compared to Z source NPC-MLI. Z-source inverter based adjustable speed drive system effectively uses the shoot-through state to boost DC bus voltage by simultaneously gating on both the upper and lower switches of a same phase leg. The shoot-through zero state has no harmful effect on the inverter and is used to boost the DC link voltage. The adopted approach enables the operation of the Z-source arrangement to be optimized and implemented digitally without introducing any extra commutations. The proposed techniques are simulated using MATLAB/SIMULINK & the results are presented. The results shown that the improved harmonic performance of the ULST over the FST strategy and also this simulation results shown that the Z-source NPC inverter Z-T NPC MLI with space vector modulated algorithm is able to boost the output line to line voltage to a value higher than the available dc supply voltage with enhanced sinusoidal output current waveforms.*

Index Terms: **Buck–boost, neutral point clamped (NPC) inverter, space vector modulation (SVM), Induction Motor drive, Z-source inverter.**

I. INTRODUCTION

The inverters are the unavoidable parts in the Photovoltaic systems (PVS), as the output of any PVS will be DC. Many industrial applications require higher power converters (inverters) to drive high power applications. Multilevel converters offer many benefits for higher power applications which include an ability to synthesize voltage waveforms with lower harmonic content [1],[2]. Harmonic performance of the converter plays important role and it is the major factor to synthesize to nearer sinusoidal output. In power systems, lower THD means reduction in peak currents, heating, emissions, and core loss in motors.

The most commonly used topologies are the cascaded inverter [3]–[5], the diode clamped inverter [6], [7], and the capacitor clamped inverter [8]–[10]. Among the above three, the three-level diode clamped [also known as the neutral point clamped (NPC)] inverter has become an established topology in medium voltage drives.

However, the neutral point clamped (NPC) inverter is constrained by its inability to produce an output line-to-line voltage greater than the dc source voltage. The multilevel inverter

Main functions are to produce a desired Alternating current voltage level from several Direct Current voltage sources. The Z-source inverter topology was proposed to over-come the above limitations in traditional inverters. The Z-source concept was extended to the Neutral point clamped inverter in, where two additional Z-source networks which consist of mainly L and C were connected between two isolated dc sources and a traditional NPC inverter. In spite of its effectiveness in achieving voltage buck–boost conversion i.e. both buck and boost.

The space vector modulation approach offers better harmonic and this can more conveniently handle the overall switching patterns. In these inverters, a DC voltage/current source supported by a relatively large capacitor/ large inductor feeds the main three phase bridge inverter circuit. Z-source inverter (ZSI) is a direct current (DC) to alternating current (AC) power conversion concept that is very promising in the fields of power conditioning especially in alternative energy sources and distributed generation and adjustable speed drives (ASD).

II. REVIEW OF Z-SOURCE CONCEPT

The two-level Z-source inverter is shown in Fig. 1. The only difference between the Z-source inverter and a traditional voltage source inverter (VSI) is the presence of a Z-source network mainly comprising a split-inductor and two capacitors. The important and unique feature of the two-level Z-source inverter is that the output fundamental ac voltage can be controlled to be any values between the zero and (theoretically) infinity. Thus, the Z-source inverter is having a capability of both buck and boost, buck–boost inverter that has a very wide range of obtainable output voltage. Z-source inverter bridge has fifteen permissible switching states unlike the traditional two-level voltage source inverter has only 8. However, the two-level Z-source inverter bridge has seven extra zero states (termed as shoot-through states). In this when the load terminals are shorted through both upper and lower devices of any one phase leg (i.e., both devices are gated ON), any two phase legs, or all three phase legs. The Z-source network makes the shoot-through zero states possible and provides the means by which boosting operation can be obtained.

Consequently, taking also the PWM modulation index M into account, the phase ac output voltage V_x can be expressed by (2)

$$V_i = \frac{E}{(1-2T_{ST}/T)} = B.E \qquad (1)$$

$$V_X = \frac{M.V_1}{\sqrt{3}} = B\{ME/\sqrt{3}\} \qquad (2)$$

where T_{ST} and T are the shoot-through interval and switching period, respectively, B is the boost factor .

Equations (1) and (2) show that the ac output voltage of a Z-source inverter can be regulated from zero to the nor-mal maximum by altering M and maintaining B = 1, or can be boosted above that obtainable with a traditional VSI by choosing B > 1.

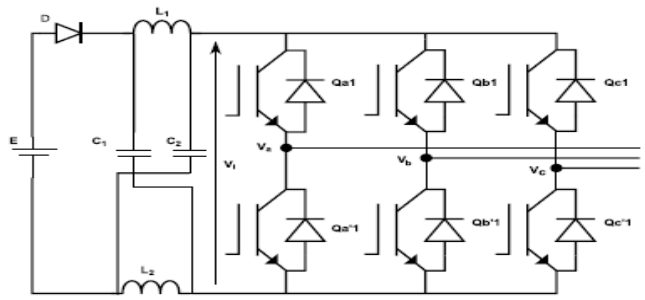


Fig. 1. Topology of two-level Z-source inverter.

III. TOPOLOGY OF REC Z-SOURCE NPC and Z-T NPC INVERTER

A. Extension of the Z-Source Concept to the NPC Inverter

To describe the operating principle of the REC Z-source NPC inverter shown in Fig. 2. The operation of each inverter phase leg of a traditional NPC inverter can be represented by three switching states P, O, and N. Switching state "P" denotes that the upper two switches in a phase leg are gated ON, "N" indicates that the lower two switches conduct, and "O" signifies that the inner two switches are gated ON.

These extra switching states occur when all the four switches in any phase leg are gated ON [full-shoot-through (FST)], or the three upper switches in any phase leg are gated ON [upper-shoot-through (UST)] or the three bottom switches in any phase leg are gated ON [lower-shoot-through (LST)].

TABLE I SWITCHING STATES OF AN REC Z-SOURCE NPC INVERTER

State type	ON switches	ON Diodes	V_{xo}	Switching state
NST	Qx1,Qx2	D1,D2	$+V_i/2$	P
NST	Qx2,Qx'1	D1,D2, {Dx1 or Dx2}	0	O
NST	Qx'1,Qx'2	D1,D2	$-V_i/2$	N
FST	Qx1,Qx2,Qx'1,Qx'2	—	0	FST
UST	Qx1,Qx2,Qx'1	Dx2,D1	0	UST
LST	Qx2,Qx'1,Qx'2	Dx1,D2	0	LST

TABLE II SWITCHING TABLE OF Z-T NPC MLI

Mode	State	Switches Triggered	Diodes Forward biased	V_{OUT}
Non Shoot through Mode	+1	S_1 S_2	D_3	$(V_{DC}/2)+L_1*(di/dt)$
	0	S_2 S_3	-	0
	-1	S_3 S_4	D_2	$-(V_{DC}/2)-L_2*(di/dt)$
Shoot through Mode	T	S_1 S_2 S_3	-	0 (L_1 Charging)
	B	S_2 S_3 S_4	-	0 (L_2 Charging)

A. Non shoot through mode:

During the non-ST mode the input DC-link voltage and the inductor voltage together are fed to the inverter which leads to the boosting of the input voltage.

B. Shoot through mode:

However, Full ST state (where all the four switches are 'ON' in a leg) is not used in the Z-T NPC-MLI to have independent control on the charging of two inductors (L1 and L2). Hence, the proposed inverter operation uses only top ST (TST) and bottom ST (BST).

C. Circuit Analysis:

The Z-source NPC inverter implemented using a single LC impedance network (see Fig. 2) is considered to be an optimized topology in terms of component count , By controlling the switches of each phase leg according to the combinations presented in Table I, each output phase voltage V_{xo} (x_{a, b, c}) has three possibilities. Those possibilities are: V_i /2, 0, $-V_i/2$.When the REC Z-source NPC inverter is operated without any shoot-through states, then V_i is equivalent to 2E.

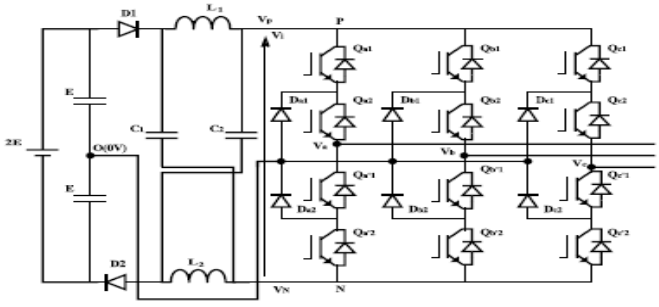


Fig. 2. Topology of an REC Z-source NPC inverter.

Therefore, to obtain an output line-to-line voltage greater than 2E, shoot-through states are carefully inserted into selected phase legs to boost the input voltage to V_i > 2E before it is inverted by the NPC circuitry. Two new switching states namely the UST and LST states were identified, in addition to the FST state and the non-shoot-through (NST) states (P, O, and N). Although operation

using the FST and NST states is possible, it is generally preferable to use the UST and LST states in place of the FST states (termed the ULST operating mode). The ULST operating mode is preferred because it produces an output voltage with enhanced waveform quality.

However, the output line-to-line voltage obtained using the minimal loss FST approach has higher harmonic distortion (compared to the ULST approach) in its output voltage wave-form because the voltage levels produced do not have adjacent level switching. The ULST operating mode is used for controlling the REC Z-source NPC inverter. Fig. 3(a) shows the simplified equivalent circuit for the NST state, while Fig. 3(b) and (c) shows the UST and LST states. Assuming that the Z-source network is symmetrical ($L_1 = L_2 = L$ and $C_1 = C_2 = C$), then $V_{L\,1} = V_{L\,2} = V_L$ & $V_{C1} = V_{C\,2} = V_C$ and the voltage expressions for the NST state are as follows:

No shoot through

$$V_L = 2E - V_C \qquad (3)$$

$$V_p = +\frac{V_i}{2},\ V_N = \frac{-V_i}{2} \qquad (4)$$

$$V_i = 2(V_c - E) \qquad (5)$$

Similarly, the voltage expressions for the UST and LST states are as follows:

Upper shoot through

$$V_{L1} = E \qquad (6)$$

$$V_p = 0\,V,\quad V_N = E - V_{C1}. \qquad (7)$$

Lower shoot through

$$V_{L2} = E \qquad (8)$$

$$V_P = -E + V_{C2}, V_N = 0\,V. \qquad (9)$$

We denote the duration of the NST, UST, and LST states by T_N, T_U, and T_L, respectively, and the switching period by T. Also, we assume that T_U and T_L are equal and denote the total combined UST and LST duration by $T_{U\,LST}$. At steady state, the average voltage across the inductors is zero; therefore, averaging the inductor voltage over one switching period, we have

$$\frac{(2E-V_C).T_N+E.T_U+E.T_L}{T} = 0 \qquad (10)$$

$$T_N + T_U + T_L = T \qquad (11)$$

Solving for Vc using (10) and (11), we have

$$V_C = (2E).\left\{\frac{1-\frac{T_{ULST}}{2T}}{1-\frac{T_{ULST}}{T}}\right\} \qquad (12)$$

Substituting (12) in to (5), we have the dc-link voltage Vi during the NST state as

$$V_{iNST} = \left\{\frac{2E}{1-T_{ULST/T}}\right\} \qquad (13)$$

Similarly, when (12) is substituted into (7) and (9) and noting that $V_i = V_P - V_N$, we have the dc-link voltage during the UST and LST states as

$$V_{i_{UST}} = V_{i_{LST}} = \left\{\frac{E}{\left(1-\frac{T_{ULST}}{T}\right)}\right\} \qquad (14)$$

It is noted from (13) and (14) that the higher dc-link voltage is present during the NST states The fundamental peak ac output voltage V_{xo} (x_{a, b, c}) is given b

$$\widehat{V_{xo}} = \frac{M}{\sqrt{3}}.V_{i\_NST} \qquad (15)$$

$$\widehat{V_{xo}} = \left(\frac{1}{1-\frac{T_{ULST}}{T}}\right)\left\{\frac{M}{\sqrt{3}}(2E)\right\} = B'\left\{\frac{M}{\sqrt{3}}(2E)\right\} \qquad (16)$$

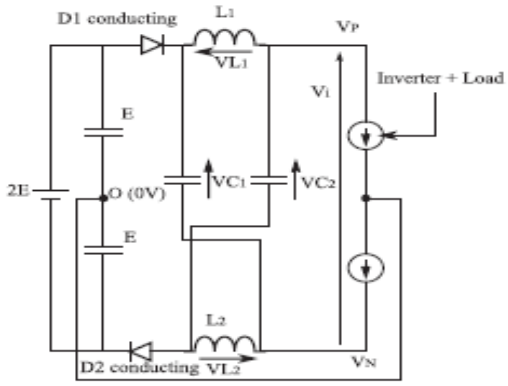


Fig.3 (a). Simplified representation of REC Z-source NPC inverter in Non shoot through state

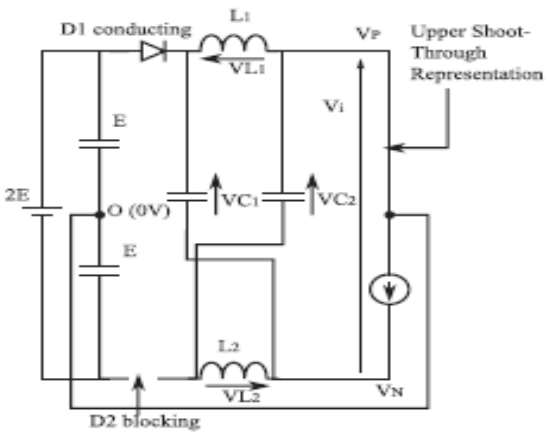


Fig.3 (b). Simplified representation of REC Z-source NPC inverter in Upper shoot through state

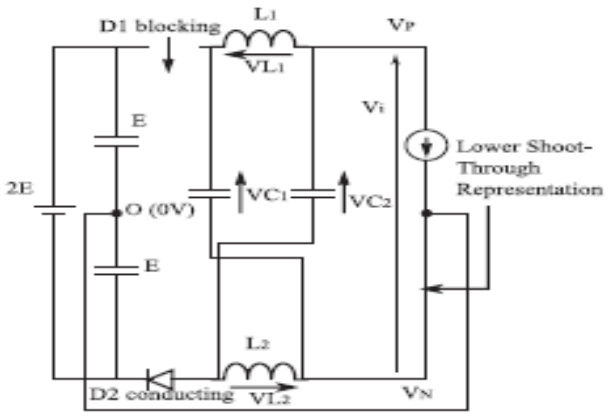


Fig. 3(c). Simplified representation of REC Z-source NPC Lower shoot through states

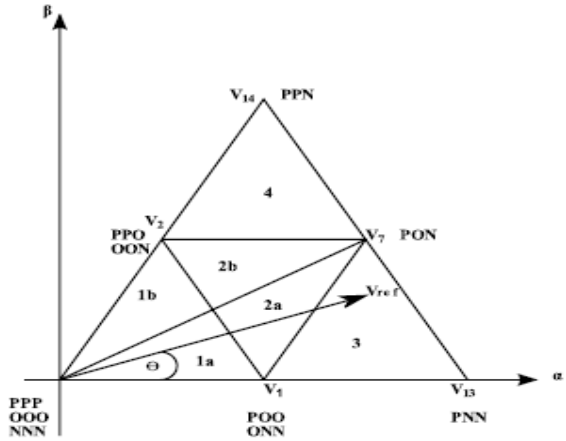


Fig. 4. Space vector diagram of sector 1 for a three-level inverter.

where B ≥ 1 is the boost factor

IV. MODIFIED SVM OF THE REC Z-SOURCE NPC & Z-T NPC INVERTER

A. Duty Cycle Calculation

The space vector diagram of a traditional NPC inverter for sector 1 is shown in Fig. 4. The reference vector $\vec{V}$ref can be expressed as $V_{ref}(t) = \frac{2}{3}[V_{ao}(t).e^{j\theta} + V_{bo}(t).e^{\frac{2\pi}{3}} + V_{co}(t).e^{\frac{4\pi}{3}}]$ (17)

Generally, in SVM, the $\vec{V}$ref is synthesized with three nearest space vectors, which are selected based on the triangle in which the reference vector is located at the sampling instant. If the reference vector is located in triangle 3, the nearest three vectors are $\vec{V}_1$, $\vec{V}_7$, and$\vec{V}_{13}$, respectively. Let the duty ratios denoted by d_1 , d_2 , and d3 , respectively. The modulation law with a sequence of the nearest three vectors based on the volt–second product is then as follows: $d_1.\overrightarrow{V_1} + d_2.\overrightarrow{V_7} + d_3.\overrightarrow{V_{13}} = \overrightarrow{V_{ref}}$

$$d_1+d_2+d_3 = 1. \quad (18)$$

The voltage vectors $\vec{V}_1$, $\vec{V}_7$, $\vec{V}_{13}$, and $\vec{V}$ref in Fig. 4 can be expressed as $\overrightarrow{V_1} = \frac{1}{3}$. (2E)

$$\overrightarrow{V_7} = \frac{\sqrt{3}}{3} . e^{j\pi/6}. (2E)$$

$$\overrightarrow{V_{13}} = \frac{2}{3} . (2E)$$

$$\overrightarrow{V_{ref}} = V_{ref} . e^{j\theta}. \quad (19)$$

Substituting (19) into (18), the duty ratios of the nearest three voltage vectors are given by (20), where M is the modulation index and $0 \le \theta \le \pi/3$. $d_1 = 2 - 2M \sin(\frac{\pi}{3} + \theta)$

$$d_2 = 2M \sin\theta$$

$$d_3 = 2M \sin\left(\frac{\pi}{3} + \theta\right) - 1. \quad (20)$$

A similar procedure is used for calculating the duty ratios of the selected voltage vectors in all the other triangles.

To achieve the minimal number of switches changing between two adjacent states, a seven-segment switching sequence (as in table III) is adopted in SVM.

TABLE III SEVEN SEGMENT SWITCHING SEQUENCE IN TRIANGLE 3

	Segment	Vector	State
E-Null 1	1st	V_1	ONN
E-Active 1	2nd	V_{13}	PNN
E-Active 2	3rd	V_7	PON
E-Null 2	4th	V_1	POO
E-Active 2	5th	V_7	PON
E-Active 1	6th	V_{13}	PNN
E-Null 1	7th	V_1	ONN

TABLE IV PERMISSIBLE UST AND LST STATES

Upper Shoot Through states	Lower Shoot Through states
UNN	PLO
UON	POL
OUN	PPL
NUN	LPO
NUO	OPL
NOU	LPP
NNU	LOP
UNO	OLP
ONU	PLP

In order to introduce shoot-through states, it is necessary to determine where the UST and LST states can be inserted, and on which phase, in order that the

normalized volt–second area applied to the load is unchanged from the standard NPC case discussed above. Note that when any phase has UST applied, the positive rail (P) is at the same potential as the dc mid-point (O). Similarly, during LST, the negative rail (N) is at the same potential as the dc mid-point (O). Consequently, it is only possible to use the UST state on a given phase when it is connected to O and the other two phases are connected either to O or N in order to get the correct line-to-line voltages. Similarly, an LST state can only be used when the other two phases are O or P. Therefore, the permissible shoot-through states are as shown in Table IV where "U" and "L" represent UST and LST states in a phase leg, respectively. Fig. 5(a) shows the seven-segment PWM switching sequences for modulating a traditional NPC inverter and an REC Z-source NPC inverter when the reference vector, $\vec{V}$ref is in triangle 3 of the vector diagram shown in Fig. 4.

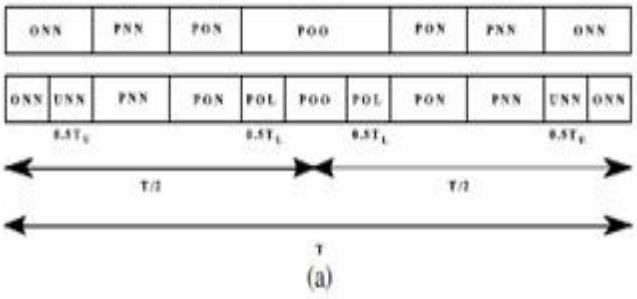


FIG. 5(a) Modulation of traditional NPC and Z-source NPC when the reference vector is in triangle 3on the three level vector diagram shown in Fig.4.

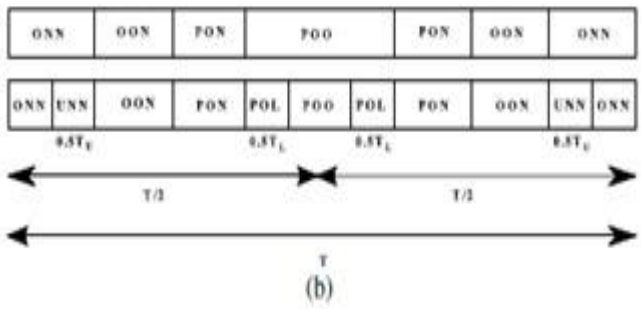


FIG .5(b) Modulation of traditional NPC and Z-source NPC when the reference vector is in triangle (4) on the three level vector diagram shown in Fig.4.

Comparing the sequences shown in Fig. 5(a), it is observed that the only difference between them is the insertion of a UST state in phase A to the left of the E-active state {PNN} and the insertion of an LST state in phase C to the right of the E-active state {PON}, respectively, within half switching period, T/2. The process is reversed in the remaining half switching period. The phase Applying the same analysis and moving on to the second transition ({PNN} to {PON}), where phase B switches from the "N" state to the "O" state, no shoot-through state is inserted (note that it is not possible to introduce UST or LST for the {PON} state for the reasons discussed earlier).Moving forward again to the third transition ({PON} to {POO}) where phase C switches from the "N" state to the "O" state, an LST state is inserted since the switching of devices {Qc1,Qc2,Qc_1,Qc_2} from {OFF, OFF, ON, ON} through {OFF, ON, ON, ON} to {OFF, ON, ON, OFF} will not affect phases A and B, which remain clamped to points P and O.

TABLE V SWITCHING SEQUENCES AND INSERTION OF SHOOT –THROUGH STATES IN TRIANGLES 2-4

Triangle	Switching Sequence
2a	{ONN}→{UNN}→{ONN}→{PON}→{POL}→{POO}
2b	{PPO}→{PPL}→{POO}→{PON}→{UON}→{OON}
3	{ONN}→{UNN}→{PNN}→{PON}→{POL}→{POO}
4	{OON}→{UON}→{PON}→{PPN}→{PPL} → {PPO}

The previous methodologies is applied to another distinct triangle, triangle 2a, a similar state sequence is derived and shown in Fig. 5(b). From the above, it is noted that in all triangles, the UST (or LST) states are inserted at the "E-Null" to "E-Active" state transitions with no shoot through states inserted at the "E-Active" to "E-Active" state transitions. Another feature noted with the ULST modulation scheme is that the UST and LST states are introduced for only half of the total shoot-through duration of T_{ULST}, unlike the FST modulation scheme, where the Z-source network is shorted for the full shoot-through duration. Therefore, to produce the same boost factor for the ULST and FST schemes, we need to set $T_{ULST}/T = 2T_{FST}/T$, where T_{FST} is the FST duration. The available shoot-through period is limited by the E-null period that is determined by the modulation index.

$$\frac{T_{ULST}}{2T} = \frac{T_{FST}}{T} = \frac{T_U}{T} = \frac{T_L}{T} = 1 - M. \qquad (21)$$

Table V gives a summary of the above discussions when the reference vector is in the various triangles of sector 1. However, it should be noted that in triangle 1, no shoot-through states are inserted because this corresponds to a low modulation index.

PROPOSED SVPWM SCHEME FOR Z-T NPC MLI

For a Z source NPC-MLI the conventional Z source SVPWM scheme uses 54 ST-states. The new proposed SVPWM scheme uses only 24 ST-states in addition to maintaining the capacitor balancing along with 27 regular switching states [3-Zero vector (ZV),12-small vector (SV),6- medium vector (MV) and 6 large vector (LV)]. Basically the MLI Z-source SVPWM schemes differ from MLI, only by adding the ST switching states. This is because, Z-Source NPC-MLI needs ST vectors to charge the inductors present in Z-network.

V. SIMULATION RESULTS

In this simulation platform, a standalone three-phase induction motor was used to verify the theoretical findings. To demonstrate the boosting ability of the REC Z-source NPC inverter, first, a modulation index, M of 0.825. The inverter dc-link voltage is obviously not boosted and the peak value of the output line-to-line voltage is maintained at almost 400V by the dc source. High-quality sinusoidal line currents are also observed.

TABLE VI COMPARISON OF ULST AND FST STRATEGIES

Parameters	FST Strategy	ULST Strategy
Total harmonic distortion	29.27%	28.39%
Commutation count	4	2
Switching loss	High	Low

The simulation results show that the REC Z-source NPC inverter, with the proposed SVM algorithm, is able to boost the output line-to-line voltage to a value higher than the available dc supply voltage with sinusoidal output currents.

To show the improved harmonic performance of the ULST strategy over the FST strategy, simulations using the FST strategy were also carried out with the same parameters as those of the ULST strategy (except that $T_{FST}/T = 0.175 = 0.35/2$) and the results shown in Fig.7.2 and Fig.7.3. Table V gives a comparison of the performances of the ULST strategy, non minimal loss FST, and the minimal loss FST strategies. Also, to show that the UST and LST states do not introduce any significant harmonic distortion to the output line-to-line voltage, the same dc-link voltage was used for the non boost mode (i.e., 2E = 120 V, $T_{ULST}/T = 0$) and the boost mode (2E = 120/1.53 V, $T_{ULST}/T = 0.35$) and their harmonic performances compared as shown in Fig. 9

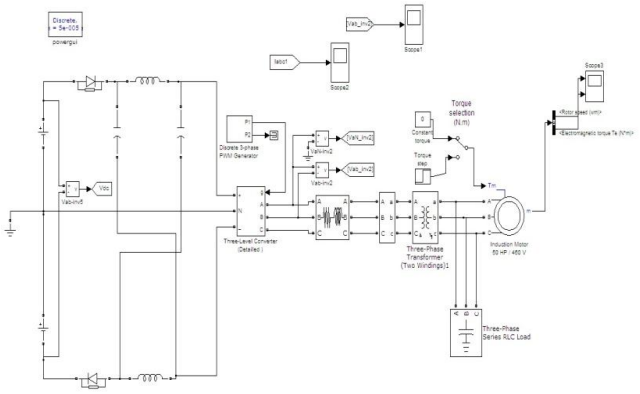


Fig.6.1.Simulink model for Carrier UST based Induction Motor.

The MATLAB/Simulink model of proposed Z-source REC three level Neutral point clamped inverter with carrier UST state is shown in the figure 5.1. In this, the input of the three level converter is a diode clamped multilevel inverter. Typically m-level inverter consists of m-levels on the phase voltage.

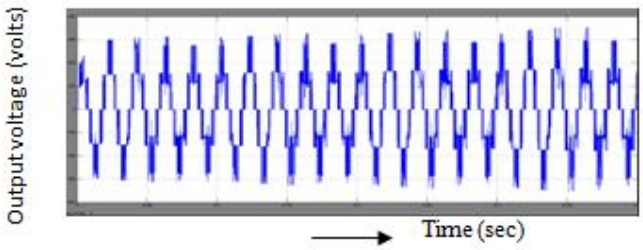


Fig.6.2 (a) Three Phase Voltages Vab,Vbc,Vca & phase to neutral voltage Van

The waveforms of phase to phase voltage V_{ab} (V) is shown in the above figure 6.2(a).The Output of the line voltage results three-level stair case.

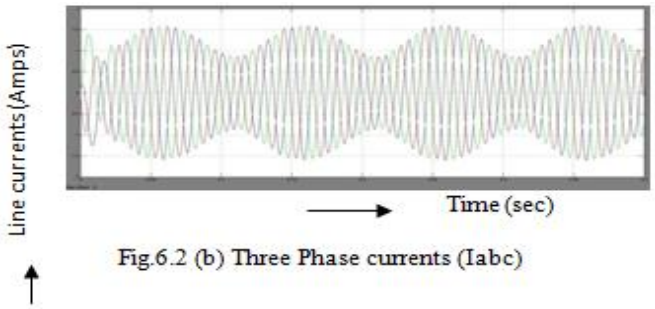


Fig.6.2 (b) Three Phase currents (Iabc)

The waveforms of a three phase currents I_{abc}(p.u) shown in above figure 6.2(b) and the enhanced three phase current waveforms obtained is nearer to sinusoidal with less harmonic content

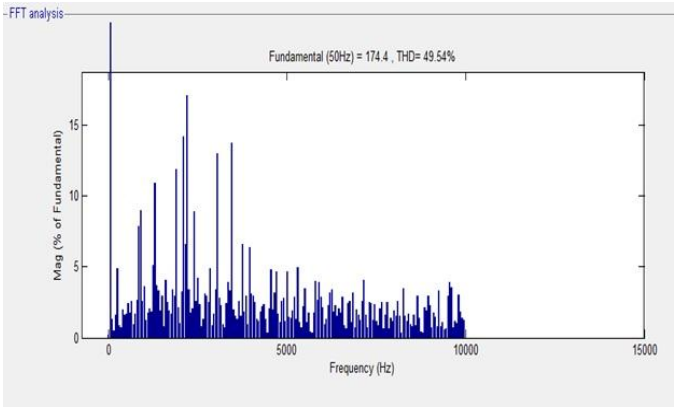


Fig.6.2(c) Voltage THD in %

Fig.6.2 Simulated waveforms of REC Z-source NPC inverter using Carrier UST strategy

Fig 6.2(c) shows the THD of a three level inverter with insertion of carrier UST switching state. The total harmonic distortion value from the FFT analysis obtained is 45.90%.

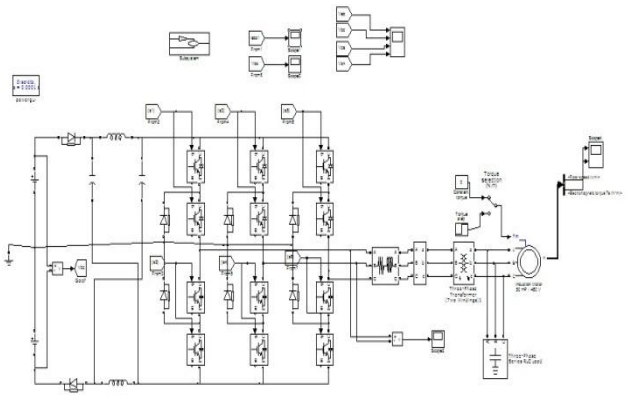


Fig.7.1 Simulink model for FST,ULST based Induction Motor.

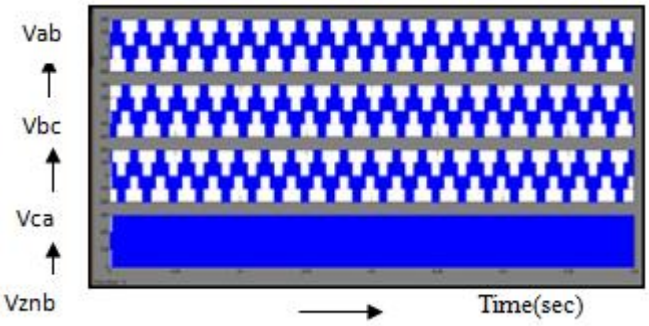


Fig.7.2 (a) Three Phase Voltages Vab,Vbc,Vca & phase to neutral voltage Van(volts)

The obtained three phase voltages is shown in the below figure 7.2(a). The waveforms shows the V_{ab}, V_{bc} , V_{ca} , V_{zn} and from the output waveforms, a 3-level stair case enhanced waveforms obtained .

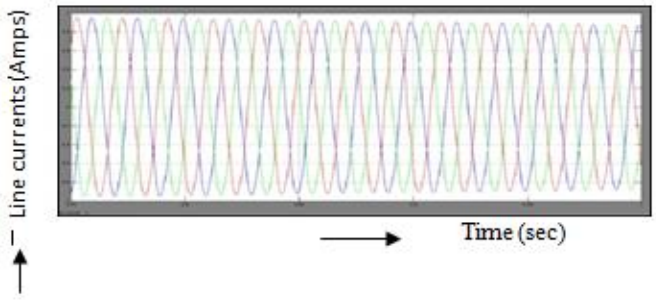


Fig.7.2 (b) Three Phase currents (Iabc)

The Full shoot through obtained current waveforms is shown in the above figure 7.2(b). From the waveforms, the obtained three phase currents are sinusoidal and also got enhanced quality current waveforms.

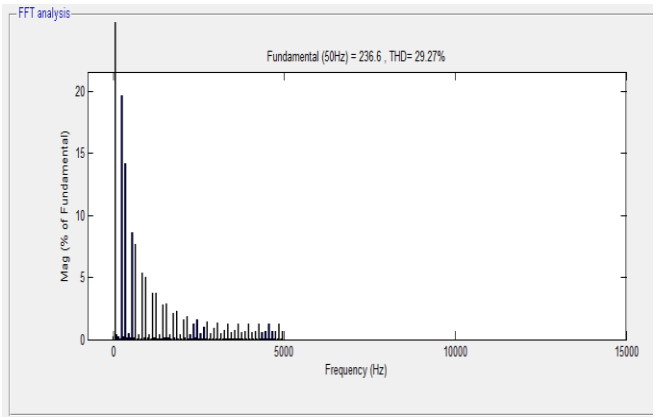


Fig 7.2(c) Voltage THD in %

Fig.7.2 Simulated waveforms of REC Z-source NPC inverter using Carrier UST strategy.

The simulation results for the full through switching state is presented above and the the total harmonic distortion is reduced as shown in the figure 7.2(c) which is a shoot through state and in this state the upper and lower switches in the phase leg are triggered. In this full shoot through state, the harmonic distortion values are greatly reduced in this and the obtained value is 29.27%.

Fig.8.1 Simulink model for ULST based Induction Motor

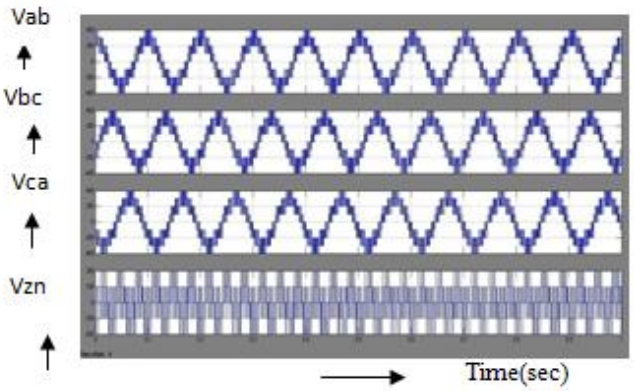


Fig.8.2 (a) Three Phase Voltages Vab,Vbc,Vca & phase to neutral voltage Van.

The output of the line-to-line voltage results a three level stair case waveforms.

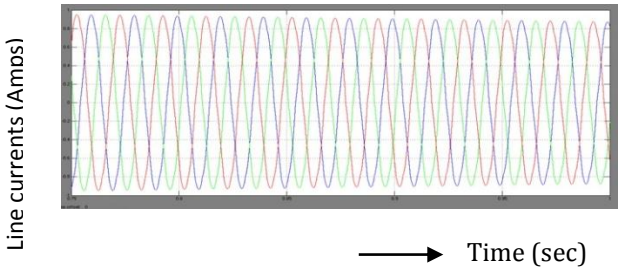


Fig.8.2 (b) Three Phase Currents (Iabc)

The upper lower shoot through obtained current waveforms is shown in the above figure 8.2(b). From the waveforms, the obtained three phase currents are sinusoidal and also got enhanced quality current waveforms.

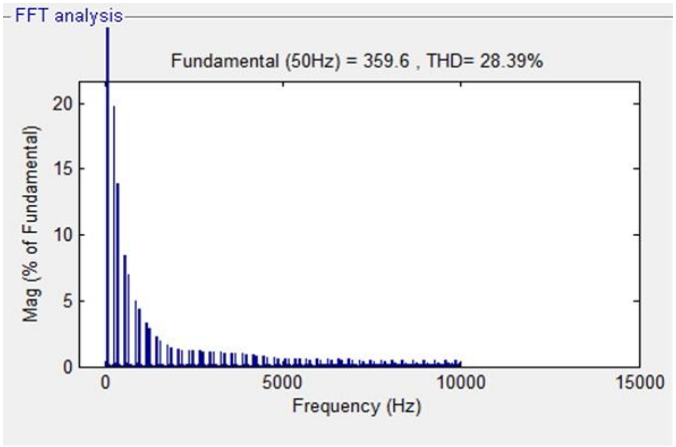


Fig.8.2(c) Voltage THD in %

Fig.8.2 Simulated waveforms of REC Z-source NPC inverter using Carrier UST strategy.

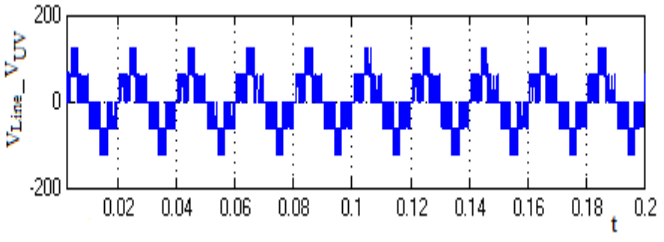
The simulation results with the combination of upper and lower shoot through switching state is presented above figure 8.2(c). The harmonic distortion values are greatly reduced in this and the obtained value using this strategy is 28.39%.

The total harmonic distortion (THD) of the output line-to-line voltage is compared to that of the proposed SVM strategy in Table VI.

TABLE VI COMPARISON OF THD OF THE PROPOSED SVM AND CARRIER-BASED PWM WITH ZERO-SEQUENCE VOLTAGE INJECTION.

Mode	Proposed SVM	Optimised carrier-based PWM
Non boost Mode	49.54%	37.47%
ULST Mode	28.39%	36.81%

From Table VI, it can be concluded that the harmonic performance of the proposed SVM strategy is comparable to the carrier-based PWM with zero-sequence voltage injection strategy described in [20] and hence is a competitive alternative for modulating the Z-source NPC inverter.



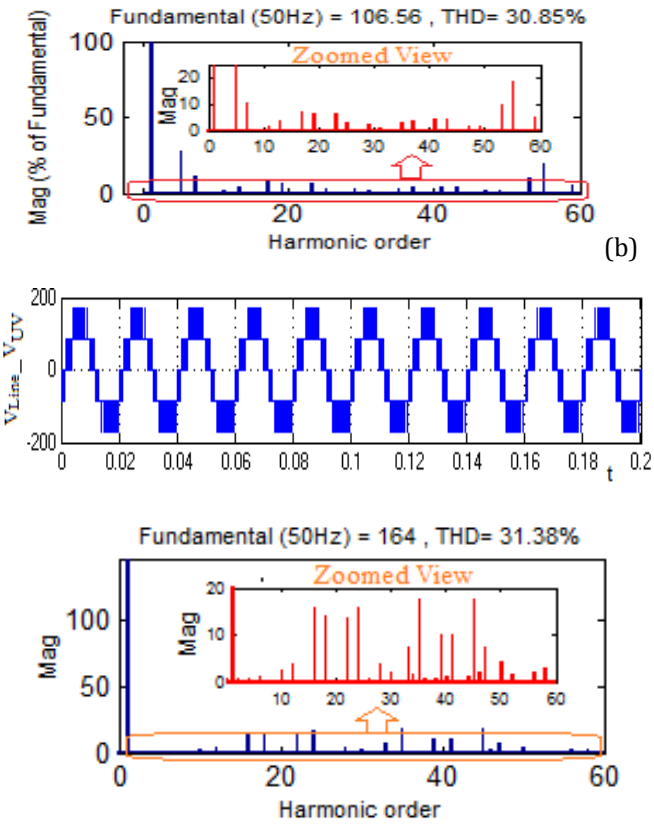


Fig.9. THD of Z-T NPC MLI

CONCLUSION

A novel Z-T NPC MLI is implemented using the new SVPWM scheme and operated in the entire modulation region both in shoot through mode and non-shoot through mode. This proposed SVPWM scheme uses redundant technique, which provides the equal switching stress to all the phases which improves the performance of the inverter for long operations.

In this paper, the simulation of three level multilevel inverter is carried out in MATLAB/ Simulink, to identify the suitable level inverter which has comparatively less total harmonic distortion in its output. The total harmonic performance of ULST and FST strategies with the same dc-link voltage. A comparative study is done for better configuration of multilevel inverter. A modified SVM for an REC Z-source NPC inverter is presented. The insertion of the shoot through states was such that the number of device commutations was kept at a minimum of six per sampling period, similar to that needed by a traditional NPC inverter.

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