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Interleaved Buck Converter with Fuzzy PI control Technique having Lower Conversion Ratio

Vikas K Bhushan[1], Revathy Anil[2], Greeshma Thankam Philip[3]

[1,2] *PG Scholar, EEE Dept., Believers Church Caarmel Engineering College, Kerala, India*
[3] *Assistant Professor, EEE Dept., Believers Church Caarmel Engineering College, Kerala, India*

Abstract - *In conventional step-down converter, the conversion ratio or the duty cycle is greater than 40% which leads to lower conversion ratio, having discontinuous current and high electromagnetic interference. In order to minimize these above mentioned disadvantages in conventional interleaved converter, a new topology based on AI is introduced in this paper. Here the proposed converter is similar to a conventional one but here two switches are placed in series with the aid of a coupling capacitor which helps to reduce the voltage stress during operation across all the switches in the converter. This allows the converter to operate under lower conversion ratio at higher frequencies. The other features of proposed interleaved type buck converter are that as compared with conventional buck converter, it has higher stepdown conversion ratio and a reduced output current ripple. The proposed IBC works in closed loop control with fuzzy accompanied by PI which helps to regulate the desired output values at most accurate. The output value is thoroughly verified by the controller unit through a feedback from the output of proposed converter and if there is a change in desired value, the system precisely controls the duty cycle in the converter. The MATLAB software is used to carry out simulations in which the Simulink model were discussed in detail.*

Key Words: Interleaved Buck Converter, Fuzzy Logic Controller (FLC), Step-down Conversion, Duty Cycle, MATLAB…

1. INTRODUCTION

The buck converter is a DC-DC converter that converts a high voltage to a low voltage. If the power conversion efficiency is high, it extends battery life and reduces heat. The buck converter can be used in lots of practical applications such as power supply for devices such as battery chargers, solar power regulators, microprocessors and so on. It is achieved by increasing the frequency of switching. But, the semiconductor losses increased due to the increase in switching frequency also ripple current. The conventional buck converter was used widely for dc-dc conversion at step-down level. The main drawback of the conventional buck converter is the electromagnetic interference (EMI) in the system due to discontinuous current supply. The electromagnetic interference can be reduced if and only if the current flowing through the converter is made continuous which also helps in reducing current stress in the capacitor which is coupled in the input level. As discussed in [1], the converter should operate at higher frequencies for better dynamics and higher power density. But the losses during turn on, turn off etc. that is termed as switching losses increases rapidly with increase in switching frequency. It also deteriorates the efficiency further more. Also it will have a very short duty cycle in cases where output voltage is very low as compared to high input voltage.

According to M. Ilic and D. Maksimovic in [2], an IBC is implemented with zero current transition. The main advantage of this paper is that there is a reduction in diode reverse recovery loss. A low switch voltage stress in interleaved converter with a novel transformer-less topology is discussed by C.T. Pan, C.-F. Chuang, and C.-C. Chu in [3]. This paper consists of two input capacitors with the aid of a voltage divider to reduce voltage stress which are charged in series and discharges in parallel. But due to the increase in number of components, system gets embroiled and results in increasing the interference which was the main downside of this paper. An interleaved buck converter with the aid of a snubber circuit is introduced in [4] consisting a single-capacitor turn-off method. During turn off, the switching loss is reduced and the inductor which is coupled act as two output inductors. But high current stress is affected to all elements due to discontinuous conduction in the circuit which results in high conduction losses and the voltages across the terminals of all power electronic devices have the voltage input Vin of the converter. As discussed in [5], with the aid of zero-voltage switching, all switches are turned ON or popularly known as ZVS which consist of an active-clamp circuit with interleaved converter having a high buck conversion ratio. But, the cost increases significantly as the converter requires additional elements such as switches and other semiconductors in order to obtain the above mentioned advantages. As discussed in [6] they introduced zero current transition based interleaved stepdown converter which is designed to reduce diode reverse recovery losses also known as ZCT based interleaved buck converter. The only difference from conventional IBC is that it contains an additional inductor. However, the converter is having high current stress due to the complementary way of current flow in the output path in each module. Also the proposed one is having the main drawbacks of the conventional interleaved structure. As discussed in [7], they introduced two extra phase windings, which extends the duty cycle of the same. Due to the leakage inductance voltage spike were caused and to reduce its effects, a clamp circuit has been implemented. Thus, the complexity is increased.

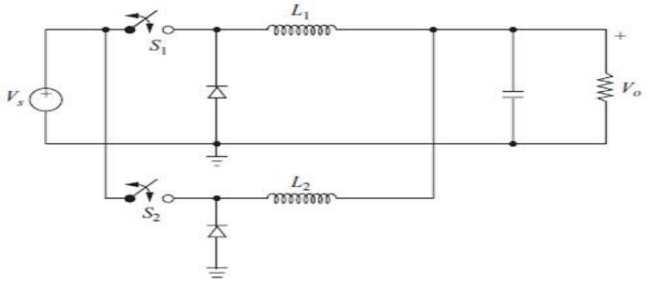

Fig -1: Conventional IBC

In an interleaved converter, the current which is shared between the phases must be balanced. Any imbalance can cause one phase to operate in DCM (discontinuous conduction mode) and the other to operate in CCM which can be due to change in duty ratio. According to H. Mao [8], current sharing comparison study is carried out between non-isolated and isolated IBCs. In paper published by J. A. Oliver, P. Zumel, O. Garcia [9], interleaved structure with the aid of passive components were analyzed results in loss reduction of these components. The design of the passive elements and the necessary relation in the phases of interleaved stepdown converter should be given.

Usually the gate signals of the conventional interleaved converters are provided with pulse width modulation. According to J. A. A. Qahouq, J. Luo and I. Batarsech in [10], the views on hysteretic controller which provides the pulses with N number of phases is explained deliberately. In Fig. 2 pulse generation with control circuit is observed which is suggested in [10], for phases in Fig. 2 and Fig. 3 respectively.

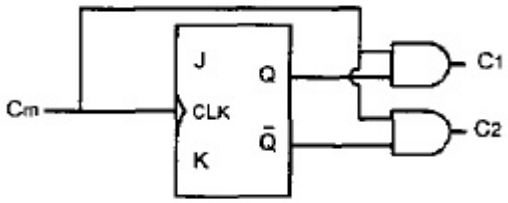

Fig -2: Pulse generation circuit for two interleaved phases

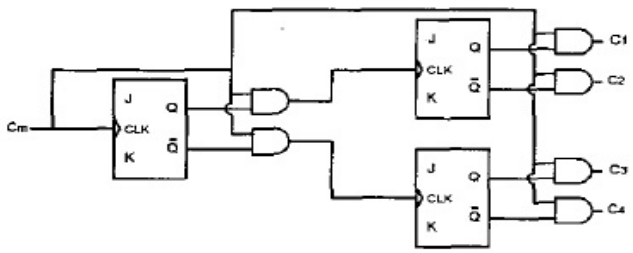

Fig -3: Pulse generation circuit for four interleaved phases

An IBC with ongoing current is established into this paper. To decrease the semiconductor voltage stress the proposed converter fundamentally consists of two input switches. The proposed one is having continuous current at the input side and has buck conversion ratio less than 0.5 as compared to the conventional interleaved buck converter. Also due to this interleaved structure of proposed converter, the output current ripple reduces. Here One Cycle Control technique is employed.

The content of this paper is arranged in the following order as the circuit configuration is in Section II, the converter operation is in Section III, strategy employed to control the converter is described in Section IV. The Section V consist of the simulation along with the waveforms and lastly, the conclusion in Section VI.

2. CONFIGURATION OF CIRCUIT

Fig.4 shows the designed IBC with lower switching losses and ripple current and the system consists of two freewheeling diodes D_1 and D_2, two switches Q_1 and Q_2 which are triggered apart of 180 degrees, two inductors L_1 and L_2, a coupling capacitor C_B and capacitor C_o as output. The voltage stress was reduced due to the series arrangement of switches.

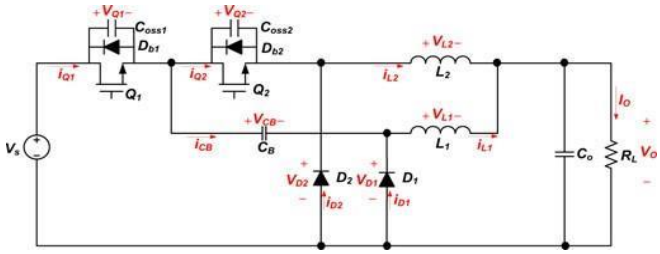

Fig -4: Proposed IBC

The conventional IBC has low on-time during high step-down value and also during high frequency applications. Thus, efficiency is low when operated at higher frequency. The duty ratio of the conventional interleaved buck converter and proposed buck converter is equal to D. The conventional IBC has voltage stress at the switch side of input whereas the voltage stress is shown in above figure i.e. Fig.4 is V_{in} / (2-D) which is less as compared with previous mentioned.

3. OPERATION OF PROPOSED CONVERTER

At initial condition, the switches Q_1 and Q_2 will be at OFF and diodes D_1 and D_2 are forward biased. The capacitor is charged. The converter operates for duty cycle between 0 and 1 has been explained into two parts i.e. operation at D less than 0.5 and operation of D greater than or equal to 0.5.

3.1 Operation for D less than 0.5

Mode1 [t_0 –t_1]: The first mode starts when the first semiconductor switch Q_1 is turned ON at t_0. Now the current I_{L1}, flows through Q_1, C_B, and L_1. V_{CB} gets charged and the current of L_2, freewheels through D_2. At this point, the current through inductor L_1 increases linearly with time and that of L_2 decreases linearly. At Q_2, input voltage will be the terminal voltage and at D_1, the terminal voltage is equal to the difference of V_S and V_{CB}.

Mode 2 [t_1 –t_2]: At t_1 when Q_1 is turned OFF Mode 2 begins. Then, through D_1 and D_2, $i_{L1}(t)$ and $i_{L2}(t)$ freewheels and

$V_{L1}(t)$ and $V_{L2}(t)$ becomes $-V_O$. Hence, current through both inductors decreases linearly. The voltage at the Q_1 terminal is the result of difference between V_S and V_{CB} and voltage across Q_2 becomes the voltage across the coupling capacitor C_B

Mode 3 [t_2 –t_3]: The third mode of operation starts when diode D_2 is turned OFF and the switch Q_2 is turned ON at t_2 on the same time. Then, inductor current of L_1, which is in series with the semiconductor switch Q_1 that is $i_{L1}(t)$ freewheels through diode D_1 and inductor current at L_2 $i_{L2}(t)$ flows through diode, coupling capacitor, switch, and inductor i.e. through D_1-C_B-Q_2-L_2. Thus V_{CB} is discharged. $V_{L2}(t)$ is the difference between V_{CB} and V_O. Thus $i_{L2}(t)$ linearly increases.

Mode 4 [t_3 –t_4]: Mode 4 begins at t_3 when Q_2 is OFF and operation is the same as that of mode 2.

At steady state, under the operating condition of $D \leq 0.5$ voltage stress except for Q_2 is determined by V_{CB}. The voltage across the coupling capacitor will be the voltage across switch Q_2 during before turn-on or after turn-off but the maximum value would be the input voltage and due to these results, the discharging of coupling capacitor C_B is reduced to a critical low value and the switching losses thus can be minimized. The conduction losses and reverse recovery characteristics can be upgraded using schottky diodes for D_1 and D_2.

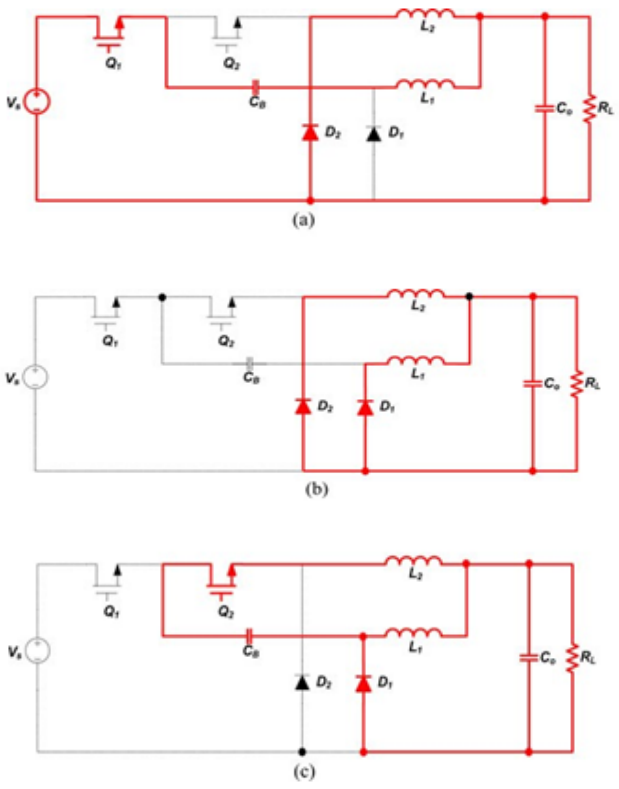

Fig -5: Operating Circuits when duty cycle is less than 0.5 (a) mode1 (b) mode2 (c)mode 3

3.2 Operation for D less than 0.5

Mode 1 [t_0–t_1]: This mode begins when switch Q_1 turned ON and switch Q_2 in on-state at t_0, the current flows through the switch Q_1, coupling capacitor C_B, and inductor L_1 and the coupling capacitor get charged. Current of inductor L_2 flows through the switches Q_1, Q_2, and through inductor L_2. The inductor voltage is positive.

Mode 2 [t_1 –t_2]: When the switch Q_2 is turned OFF at t_1, Mode 2 begins. Then, current at inductor L1 flows through the switch Q_1, coupling capacitor C_B, and inductor L_1 and $i_{L2}(t)$ freewheels through diode D_2. The operation is the same as mode1 of $D \leq 0.5$.

Mode 3 [t_2 –t_3]: The operation is the same with mode 1 and it begins when mosfet switch Q_2 is turned ON at t_2.

Mode 4 [t_3 –t_4]: This mode begins when Q_1 is turned OFF at t_3. Now through D_1, $i_{L1}(t)$ freewheels and through D_1, C_B, Q_2 and L_2, $i_{L2}(t)$ flows and V_{CB} is discharged. The operation during this mode is the same with mode 3 in 3.1

The proposed interleaved step-down converter operating with duty ratio greater than 0.5 under steady state operating condition is described. The voltage stress of semiconductor switch Q_1 and diode D_1 is determined by Coupling capacitor voltage, but the voltage stress of semiconductor switch Q_2 and the diode is achieved by voltage at input level. Switches Q_1 and Q_2 experience high current stress in this case.

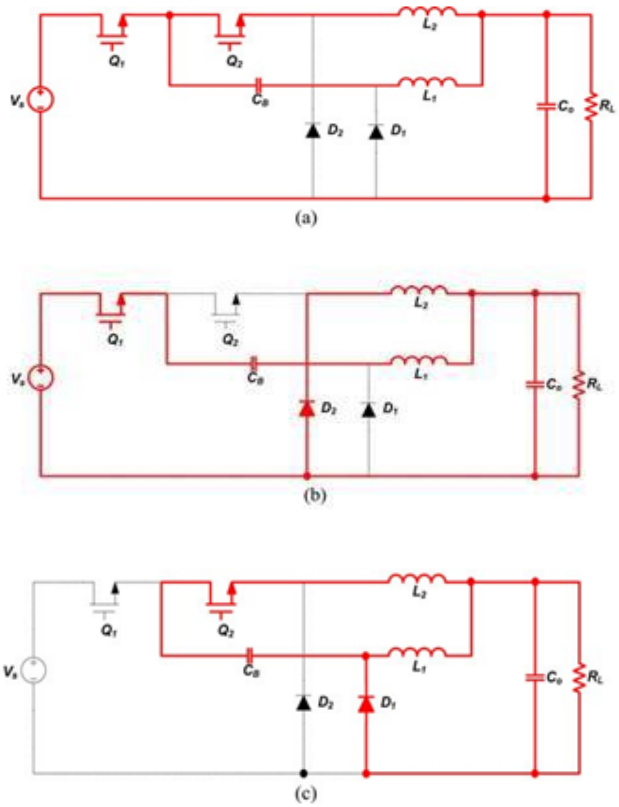

Fig -6: Operation of Circuits when D greater than 0.5. (a)mode1 (b)mode2 (c)mode 3

4. CONTROL STRATEGY

The simplest method to trigger a switch in a converter is by providing current pulses with open-loop control. But output is independent of load variation, i.e., appropriate adjustments are not able to made by the control system. To overcome these disadvantages, closed-loop control scheme was introduced. This scheme provides adjustments in the duty ratio. Pulse Width Modulation (PWM) is used in this scheme. The difference between the reference value and the actual value is reduced. This has a slow response time; a transient over-shoot occurs. In order to obtain load regulation a PI controller is added along with the fuzzy logic. Since the fuzzification is the sub category of artificial intelligence, it has the advantages such as simple to design and does not require the knowledge of an exact model. According to the basic concept, the fuzzy logic control is having two input variables which are named as Error and Change in Error i.e. E and CE respectively and for every controller there should be an output. Here the output is the duty cycle which is denoted as D. Out of the two output variable in the fuzzy logic controller, by taking the variable E which is the input set as the first one and it is transformed in terms subsets which are represented as NB, NS, ZE, PS and PB which stands for negative big, negative small, zero, positive small and positive big respectively. The detailed graphed membership functions for the input variable E which stands for error in the fuzzy logic subsets are shown in Figure7.

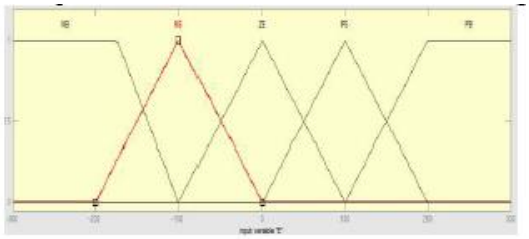

Fig -7: Input variable E's membership functions.

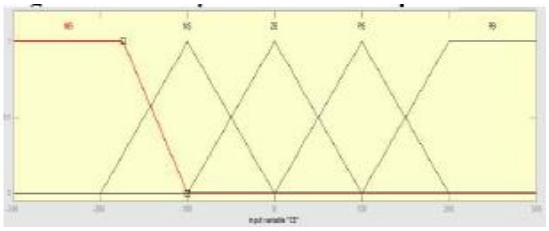

Fig -8: Input variable CE's membership functions

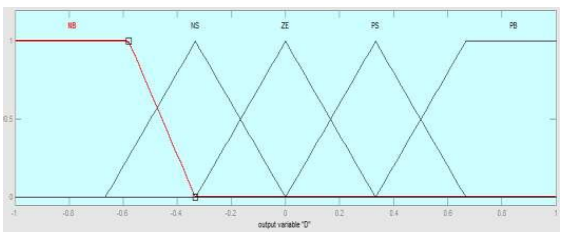

Fig -9: Input variable D's membership functions

Now the set of the CE is taken as the second input to the fuzzy logic controller which is the change in error and classified into five subsets which are NB, NS, ZE, PS and PB which are negative big, negative small, zero, positive small and positive big respectively. Here the second input variable CE or change in error is also a membership functions for the input side and is shown in figure8. Lastly the justification subset which is used to justify for the output variable which is the duty ratio, D is given in Figure9. The fuzzy logic controller works on a rule base which is created in figure 10 with input variables Error and Change of Error as inputs while D subset as the output. The fuzzy rule matrix table is given below.

E / CE	NB	NS	ZE	PS	PB
NB	NB	NB	NB	NS	NS
NS	NB	NS	NS	NS	PS
ZE	NB	NS	ZE	PS	PB
PS	NS	PS	PS	PS	PB
PB	PS	PS	PB	PB	PB

Fig -10: fuzzy rules

5. SIMULATION

The Simulink model using MATLAB software of proposed interleaved buck converter with lower duty cycle is given in Fig. 10. Here the voltage applied is 200V to the converter and an output of 24V is obtained with a switching frequency of 100 kHz (chosen). The parameter values for the simulation is listed in Table I.

Table -1: Parameter Values

Parameters	Values
Input Voltage	200 V
Output Voltage	24 V
Switching Frequency	100kHz
L_1 and L_2	100µH
L_o	5 µH
C_o	1 µH

Here a voltage of 200V is applied at the input side. The output voltage waveform which is termed as VO and the output current, termed as I_0 It can be viewed from the waveforms that a 24V output has been obtained. Also, the output ripple current has been greatly reduced. The above mentioned can be seen from waveforms in figures 12 and 13 respectively The inductor current waveforms I_{L0}, I_{L1} and I_{L2}can be obtained in Fig. 14. Fig. 15 shows the voltage and current stress experienced by the switches and Fig. 16 shows the voltage and current stress experience by the diodes.

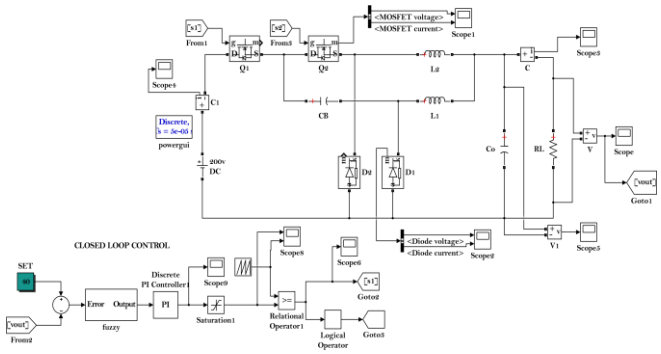

Fig -11: Simulink Model

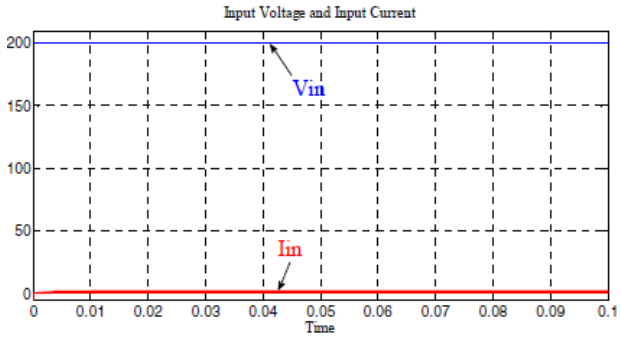

Fig -12: Input voltage and input current waveform

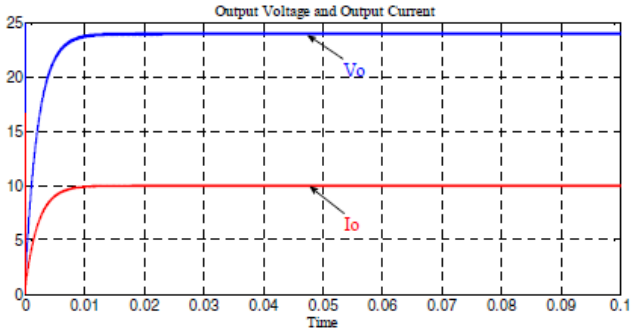

Fig -13: Output voltage and output current waveform

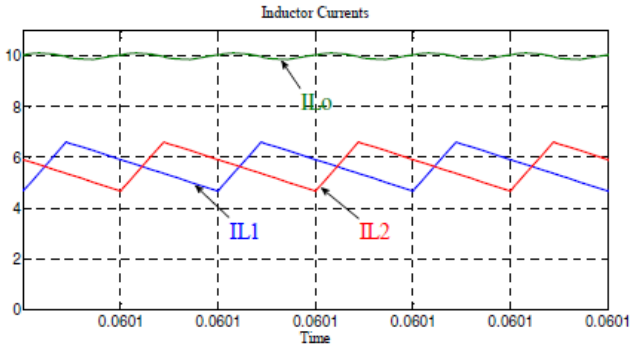

Fig -14: Inductor current waveform

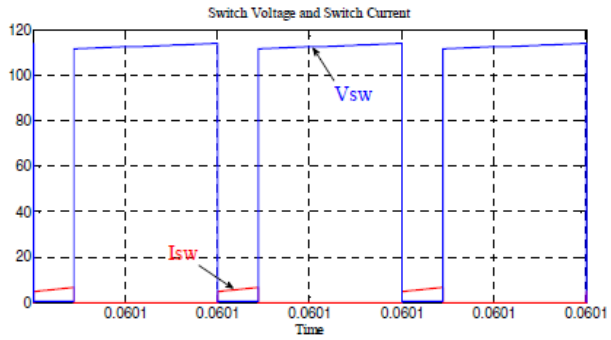

Fig -15: Voltage and current waveform of switches

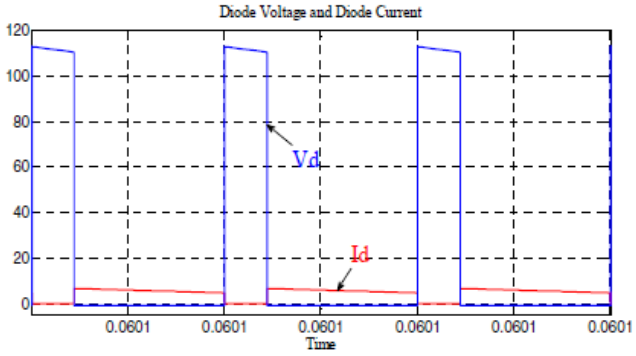

Fig -16: Diode voltage and current waveform

3. CONCLUSION

In this paper, the main features of the proposed interleaved buck converter have been discussed. Mainly the switching losses are reduced considerably due to the interleaved structure of the proposed converter. Also, the buck conversion ratio has been improved. The output current has low ripple. MATLAB software is used to execute the simulation

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