

Methods for improved efficiency in dc-dc buck converter

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Abstract - Switching mode DC/DC converters are crucial building blocks in portable devices and therefore their power efficiency, accuracy and cost are the major issues. Switching converters gained popularity in powering portable devices because of their high efficiency, compact sizes and high current delivery capability. However, such portable devices for most of the time operate at light loads and are only required to deliver high current for short periods, while conventional buck converter suffers from low efficiency during light load condition due to the switching losses that do not scale with load current. In this research, various techniques for efficiency improvement of buck converter is presented.

Key Words: DC/DC Converter, Buck, SMPS, Compensation Network, VMC, CMC, ESR, Pulse Width Modulation (PWM), PMIC (Power Management IC)

1. INTRODUCTION

Employing DC/DC converters can be viewed as a method to generate multiple voltage levels from a single DC supply voltage to feed the different sub-circuits in the device. This method of generating multiple voltage levels from a single battery source can reduce the device area considerably. While on the other hand DC voltage directly provided by battery or rectifier, besides containing high voltage ripples also is not constant enough, thus it is not applicable for most devices. DC/DC regulators are employed to attenuate the ripples regardless of change in the load current or input voltage [1].

Due to ever increasing demand from power systems has placed power consumption as the primary concern. To keep up with these demands, engineers have dedicated immense and numerous work towards developing efficient conversion techniques. However, the efficiency is not always maximized, but varies according to the size of load. Hence improving light-load efficiency is critical for portable devices.

1.1 Switched Mode Power Supply (SMPS)

Switching-mode power supply which is also called as switching-mode DC to DC converter is a type of power supply which uses switches (usually in the form of transistor) and low loss components such as inductors, capacitors and transformers for regulating output voltage [2]. The circuit of SMPS consists of two main parts: power stage and control part as shown in fig 1. Nowadays most of the work is done on control part for better regulation of output voltage, whereas the power part has not undergone many changes. Generally

MOSFET is used as a power switch in SMPS for stabilizing output voltage. The switches are not conducted continuously and they operate under specific frequency, therefore they are useful for conservation of battery life and reduction of the power loss in the circuit.

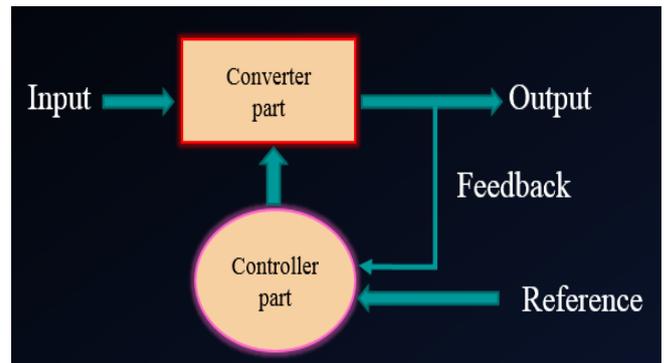


Fig -1: Block diagram of SMPS

1.2 High Efficiency

Efficiency is the most critical and important parameter for any power supply. A lot of work has been published in the field of improving efficiency. Since the efficiency of buck converter drops both at light load and at heavy load as shown in fig 2, the research is divided into two directions depending on different applications. Applications such as battery-powered portable devices need to be designed for high efficiency over entire load ranges extended from light load to heavy load, and especially at the light load range, since they operate at this region most of the time. This paper is targeting at these applications and working on improving light-load efficiency.

2. TECHNIQUES AND CONTROL SCHEMES

There are various kinds of techniques for improving efficiency of buck converter. Among all these techniques, soft switching techniques, especially zero-voltage-switching (ZVS) and zero-current-switching (ZCS) are very popular in high power applications. In ZCS technique, an inductor is placed in series with converter main switch or main diode to provide soft switching condition at switch turn-on instant. acronyms the first time they are used in the text, even after they have

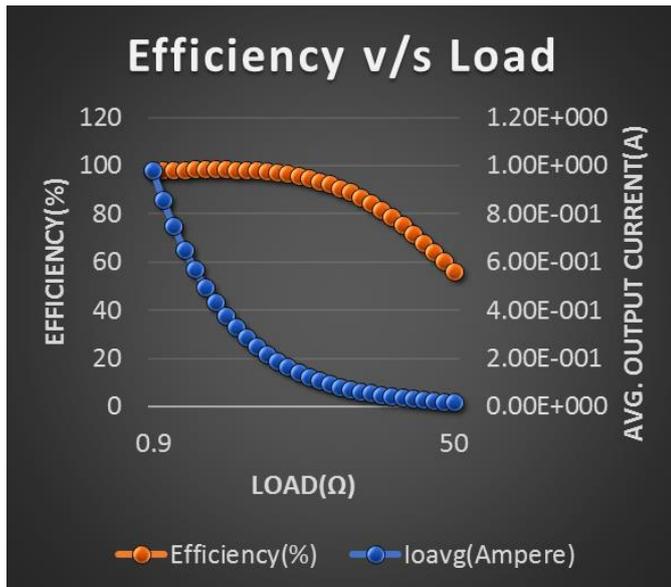


Fig -2: Efficiency vs Load

Before switch turn-off instant, an auxiliary switch is turned on and the main switch current is reduced to zero. In ZVS technique, a capacitor is placed in parallel with the main switch to provide soft switching condition for switch turn-off [3]-[5]. In this technique, soft switching condition for switch turn-on is achieved by an auxiliary switch, which discharges the snubber capacitor across the main switch. Soft-switching techniques typically increase the current and/or voltage stresses in the semiconductor devices. ZVS techniques typically increase the voltage stress of the active switches, and ZCS techniques increase current stresses. Furthermore, the auxiliary large and lossy inductor and capacitor make these techniques poor candidates for on-chip implementation applications.

To improve the output transient response of buck converter, numerous control topologies are proposed for different applications. Faster recovery time and/or smaller voltage overshoot/undershoot, as well as simpler implementations and smaller sizes are targeted. Traditional control techniques, such as pulse width modulation (PWM) and pulse frequency modulation (PFM), still have margin for improvement. For example, [18] propose a pseudo-Type III compensation for PWM voltage-mode buck converter, which mimics the frequency response of a Type III compensator. Type III compensator provides two zeroes and two poles by adding large value resistors and capacitors to stable the loop, which is area consuming. The pseudo-Type III compensation in [6] is able to be implemented without resistors and capacitors, thus tremendously reduces the chip area and power consumption. Hysteretic control techniques are also popular due to advantages in their simplicity, immediate response to a line/load transient and unconditional stability under all operation conditions. Their main disadvantages are switching frequency varies with design parameters, and the inductor current may go beyond the current limit of the power switches during large signal transient response [7]-[9].

Although analog controllers are still the mainstream control schemes, digital control has gained popularity recent years due to its robustness to noise, lower sensitivity to parameter variations and programmability along with its ability to implement sophisticated control schemes [10]-[11]. The main concern in digital control is how to match the dynamic performance of their analog counterparts [11]-[14]. ADC which digitizes the error signal and digital PWM generator (DPWM) are the main building blocks and the most challenging circuits to design digital control [15]-[19].

3. EFFICIENCY IMPROVING IN LIGHT LOAD CONDITIONS

3.1 PFM

The most frequently used method to improve light-load efficiency is to employ pulse frequency modulation (PFM) control mode [43], [21]-[29]. Since switching loss is proportional to switching frequency, by scaling down the switching frequency together with load current, PFM mode is able to reduce the switching losses, and maintains high light-load efficiency. The main problem with PFM mode is the varying switching frequency causes more severe Electronic magnetic interference (EMI), making it unsuitable for noise-sensitive RF circuits in portable devices.

3.2 Pulse Skipping Mode

Another prevailing method in industry is pulse skipping modulation (PSM) [30]-[32]. In PSM mode, control signal will skip some clock cycles as the load decreases. The equivalent switching frequency is reduced, resulting in increased light-load efficiency.

3.3 Burst Mode

Burst mode technique is also commonly used in improving light-load efficiency [33]. When configured for this mode and during light load, the converter will alternate between ON and OFF state. During ON state, the controller bursts out a few pulses to maintain the charge voltage on the output capacitor. During OFF state, it turns off the converter and goes into sleep mode with most of internal circuits shut down. One drawback of burst mode is an additional low frequency ripple added on the output voltage during ON state.

3.4 Mode-Hopping

In mode-hopping technique, the buck converter operates in both synchronous and asynchronous modes. Under medium to heavy load conditions, it operates in synchronous mode. Under light load condition, it operates in asynchronous mode. However, conduction losses are not the dominant power loss under light load condition, thus the efficiency improvement by this technique itself is limited.

3.5 Gate Drive Technique

In [42], [34]-[35], a gate drive technique was presented whereby the gate voltage swing statically reduced or dynamically scales with load current such that the gate drive loss reduces at light load. The main problem with this technique is that it only reduces the gate-drive loss, but not the switching loss due to switch the switching node.

3.6 Other Techniques

There are several other techniques to get power loss reduction at light load condition, such as width controlling technique [20], [33]-[36], dead-time controlling technique [37]-[41].

4. PROBLEM STATEMENT

DC-DC Buck Converter faces low efficiency during light load conditions.

4. CONCLUSION

Hence various techniques to improve efficiency during light load conditions have been studied.

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