

Decimator Filter For Hearing Aid Application Based On FPGA

Miss. Tejal V. Rahate¹, Dr. S. A. Ladhake², Prof. U. S. Ghate³

¹M.E. Student Sipna College of Engineering and Technology Amravati, India

²Principal Sipna College of Engineering and Technology Amravati, India

³Assistant Professor Sipna College of Engineering and Technology Amravati, India

Abstract - The design of decimator filter requires a set of filters for hearing aid applications that gives reasonable signal for the concerned type of hearing loss. Using a variable bandwidth filter, helps a person with hearing loss to listen and communicate by making sounds audible and clearer. The design of variable bandwidth filter is carried out for a set of selected bandwidths. Each of these bands is frequency shifted and provided with sufficient magnitude gain, such that, the different bands combine to give a frequency response that closely matches with audiogram. The technique employed for the design of the filter is Canonic Signed Digit (CSD) representation. The higher sampling rate of the signal is decimated to low sampling rate by implementing the filter using the multi rate approach. The two FPGA devices can be used Spartan-3E and Virtex 2Pro. Furthermore, multi rate filtering method is used to attain high-resolution. It may reduce the complexity of the circuit and also the overall power consumed.

Key Words: Decimation filter, CIC filter, FIR Filter, FPGA, Half Band filter, MATLAB, Xilinx.

1. INTRODUCTION

A Field Programmable Gate Arrays or FPGAs are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs). It is an integrated circuit that can be programmed or reprogrammed to the required functionality or application after manufacturing. Important characteristics of field-programmable gate arrays include lower complexity, higher speed, programmable functions and volume designs. Nowadays, FPGAs as cost-effective integrated tools have many applications in the field of communication and a growing range of other areas. Using FPGAs for hardware acceleration in software defined radios (SDR) offers extensive processing power to realize promised portability of waveforms and re-configurability. The decimation filter (decimator) is one of the basic building blocks of a sampling rate conversion system. The decimation filter performs two types of operations: low-pass filtering as well as down sampling. The filter converts low resolution high bit-rate data to high resolution low frequency data. It has been widely used in such applications as speech processing, radar systems, antenna systems and communication systems. Considerable attention has been focused in the last few years on the design of high efficiency decimation filters. The decimation process requires a low-pass filter of high quality and a sampling rate converter that helps to reduce the sampling frequency to a low level. A hearing aid is helpful for the people having hearing loss to hear more precisely in both quiet and whirring situations.

It helps a person with hearing loss to listen and communicate by making sounds audible and clearer. The minimum frequency of a person hearing is usually considered to be 20 Hz whereas the maximum limit is 20 kHz, but the ear is more sensible to audio from 1 KHz to 4 KHz. Thus, it is beneficial to design a deaf aid application that operates in the desired range of frequency and makes use of oversampling concept. Furthermore, multi rate filtering method is used to attain high-resolution. It can reduce the complexity of the circuit and also the overall power consumed. There are two important parameters which effects hearing. One is loudness that is the intensity of sound and the other one is pitch, which is the frequency of the fundamental component in the sound.

In 1981, Eugene Hogenauer invented a new class of economical digital filters for decimation and interpolation (converting the sampling rate from low to high) called a cascaded integrator comb (CIC) filter. This filter was composed of an integrator part and comb part. It then has experienced some modifications towards improvements in power consumption and frequency response. This filter is a combination of digital integrator and digital differentiator stages, which can perform the operation of digital low pass filtering and decimation at the same time. In this paper, we analyze the decimation filter using MATLAB and then performing stimulation with Xilinx ISE or Quartus II.

2. LITERATURE REVIEW

From the last few years, there has been a vast growth in the field of VLSI, Optimized decimation filters for wireless communication receivers based on FPGA is use by Vennached Karunakeroud [1], concluded poly phase required more area in comparison with CIC based filter and for both the decimation and interpolation, CIC filters are used multi-rate digital signal processing. Number of signal processing algorithm have been developed by Siddharth Raghuvanshi [2], which allow the user to focusing on real time signals such as speech to convert the signal with desired quality. The digital hearing aids are performed on Application Specific Integrated Circuit (ASIC), not only the efficiency and complexity of Hearing aid increases but also required more space and because implementation of hearing aid in digital is not interesting task and more power consuming also on ASIC. Stephen Colaco explains the decimator filter for audio application using canonic signed digit (CSD) representation. The use of the CSD multiplier design results in a multiplier less solution to digital filters, where the complexity of design is a function of the number of non-zero digits in the filter coefficients. This method has less power consumption as well as reducing the cost. R. Mehra [4] gives an easy way to

measure high speed CIC decimator for wireless applications using software defined radios. Expensive anti-aliasing analog filters are getting reduces and performing different types of signals with different sampling rates. For the operation of additions/subtractions, the Cascaded Integrator comb used decimation filter which performed sample rate conversion (SRC). L. Singh [5] In this paper, FPGA's possess a very attractive solution for more flexibility, time-to-market, performance and cost. Vivek Venugopal [6] performed the filtering at a high rate and also implemented the decimation filter with the help of canonic signed digit (CSD) way. Oversampling concept is used as well as sigma delta analog to digital converters is done in hearing aid application. Abdul Rehman Buzdar [7] used a various digital signal processing technique in hearing aid such as Wavelet Transforms, uniform and non-uniform filter bank and Fast Fourier Transform (FFT). In uniform filter banks all the filters have equal bandwidth and use a input signal sampled at the same frequency, actually it is a group of band pass as well as high pass filter. In this paper, it achieved acceleration and also implementing echo cancellation, noise reduction adaptive filtering to make hearing aid work better. Divya Naga Padmini P represents different ways of realizing half-band FIR low pass filter and provides comparison of critical path delay and clock frequencies for direct form, transposed form and DA (Distributed Arithmetic) type of architectures, In this paper, because of using multipliers which gives rise to few demerits in terms of increase in area and increase in the delay which ultimately results in less performance. To resolve this issue, DAA (Distributed Arithmetic Architecture) is used which is a popular method for implementing digital FIR filters on FPGAs through which delay can be reduced and multiplier less realization can be achieved. Vishal Awasthi explains data rate conversion as well as filtering. In this paper, it consists of three class of filters FIR, IIR and CIC filters. IIR filters are simpler in structure but do not satisfy linear phase requirements which are required in time sensitive features like a video or a speech. FIR filters have a well defined frequency response but they require lot of hardware to store the filter coefficients. CIC filters don't have this drawback they are coefficient less so hardware requirement is much reduced but as they don't have well defined frequency response. So another structure is proposed which takes advantage of good feature of both the structures and thus have a cascade of CIC and FIR filters.

3. PROPOSED WORK

The CIC Filter: Completely in the canal is the one of the type of hearing aid. In the structure of CIC, the sampling rate is converted from low to high is called a cascaded integrator comb (CIC) filter. The comb filters do not need any multipliers and hence includes simple functions that are desirable at high frequencies. The response of the comb filter is a low pass filter with a distinct cutoff. Due to all the above reasons, comb filters are employed for the initial stage of decimation. To reduce the sampling frequency, a series of comb filters is connected, which will be used as the input to the subsequent stages. CIC filters achieve sampling rate decrease (decimation) and sampling rate increase (interpolation) without using multipliers. The CIC filter first

performs the averaging operation then follows it with the decimation. These filters require no multiplier and use limited storage that's why they are designated cascaded integrator comb filters because their structure consists of an integrator section operating at the high sampling rate and a comb section operating at the low sampling rate. Using, CIC filters, the amount of pass band aliasing or imaging error can be brought within prescribed bounds by increasing the number of stages in the filter. However, the width of the pass band and the frequency characteristics outside the pass band are severely limited. The block diagram of decimation filter is as follows:

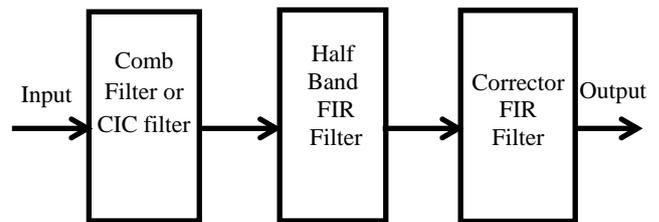


Fig 1: Block diagram of decimation filter

- Design half band FIR filter: Half-band filter is a fundamental building block in multi rate signal processing. Half-band filters are mostly used for their efficiency in multi-rate applications. A half-band filter is a low pass filter that reduces the maximum bandwidth of sampled data by an approximate factor of 2 (one octave). When multiple octaves of reduction are needed, a cascade of half-band filters is common. And when the goal is down sampling, each half-band filter needs to compute only half as many output samples as input samples. The FIR half band filter is simple to design, hardware cost effective and has moderate coefficient sensitivity. Half band filters have two important characteristics, the pass band and stop band ripples must be the same, and the pass band-edge and stop band-edge frequencies are equidistant from the half band frequency.
- Using Corrector Filter: Corrector filter is used for removing the unwanted signals. Digital filters with finite-duration impulse response (all-zero, or FIR filters) have the advantages are exactly linear phase, always stable as well as the filter startup transients have finite duration.
- MATLAB based simulation: At a time of designing or creating a decimation filter, firstly decided which type of filters will be used for perfect getting output as well as where decimation will occur. For implementing the proposed structure and design flow for decimator filter implementation are as follows:
 1. Define the filter specifications such as order, filter design, cut-off frequency, differential delay, pass band ripple and sampling frequency.
 2. Calculate the filter coefficient and stimulate in MATLAB environment and then model Simulink performed.

- Getting VHDL code and after that simulation in Model sim, finally implementation will done.

Simulation: On the basis of the simulation results the whole system may be implementing in software using the Xilinx or Quartus II. Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for analysis, stimulate a design's reaction to different stimuli, perform timing analysis and configure the target device with the programmer. Quartus II is programmable logic device design software produced by Altera, before Altera was acquired by Intel and the tool was renamed to Intel Quartus Quartus II enables analysis as well as synthesis of HDL designs, which enables the developer to compile their designs, perform timing analysis, stimulate a design's reaction to different stimuli, and configure the target device with the programmer.

4. APPLICATIONS

- Used in Military, Forensic area etc.
- For amplify the signal and also reduce the sampling frequency to a low level.
- A hearing aid is helpful for the people having hearing loss to hear more precisely in both quiet and whirring situations.

5. CONCLUSION

As we proposed a system to an efficient method for the design of digital filters suitable for digital hearing aid. The higher sampling rate of the signal is decimated to low sampling rate by implementing the filter using the multi rate approach. The decimation filter gives better results in terms of speed, timing analysis, efficiency and resource utilization etc. Specifications of decimator filter such as ripple factor, number of stages, pass band frequency, cut off frequency, Differential delay etc. will finding on the bases of filters after simulation. Cascading several multi rate stages increases the design efficiency, which reduces the total number of coefficients and in turn results in hardware savings and also less power consumptions.

REFERENCES

- V. Karunakergoud, D. Kavitha, S. Swetha "Wide Band Rate Conversion using CIC Filters for Wireless Communication Receivers", International Journal of Recent Development in Engineering and Technology(IJRDET) Vol.3, pp. 144-150, September 2014.
- Siddharth Raghuvanshi1 , Subodh Goyal "Development of Digital Signal Processing Platform for Digital Hearing Aid", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 3, Issue 2, February 2014

- Stephen Colaco. "Design and Implementation of a Decimation Filter For High Performance Audio Applications", 2007 14th IEEE International Conference on Electronics Circuits and Systems,12/2007.
- R. Mehra, R. Arora "FPGA Based Design of High- Speed CIC Decimation for Wireless Applications", International Journal of Advanced Computer Science and Application (IJACSA), Vol.2, no.5, pp. 59-62,2011.
- R. Mehra, L. Singh "FPGA Based Speed Efficient Decimator using Distributed Arithmetic Algorithm0 (IJCA)", Vol. 80, no. 11, pp. 37-40, October 2013.
- Venugopal V and Abed, Khalid.H. "Design and implementation of a decimation filter for hearing aidapplications", Proceedings IEEE Southeast Con, pp.111 - 115, April 2005.
- Abdul Rehman Buzdar, Azhar Latif, Ligu Sun, Abdullah Buzdar, "FPGA Prototype Implementation of Digital Hearing Aid from Software to Complete Hardware Design", (IJACSA) International Journal of Advanced Computer Science and Applications, Vol. 7, No. 1, 2016
- Divya Naga Padmini P, "High Speed and Multiplier less Implementation of Half-Band Filter", International Journal of Engineering Research & Technology (IJERT) Vol. 4 Issue 02, February-2015.
- Vishal Awasthi, "Analysis of Cascaded Integrator Comb (CIC) Decimation Filter in Efficient Compensation", International Journal of Electronics Engineering, 3 (2), 2011, pp. 203- 208.

BIOGRAPHIES



Miss. Tejal V. Rahate B.E.(Electronics and Telecommunication), H.V.P.M's College Of Engineering And Technology, Amravati, Sant Gadge Baba University, Amravati, India.

M.E. Student (Digital Electronics), Sipna College of Engineering and Technology,

Amravati, Sant Gadge Baba University, Amravati, India.