

# A NEW HIGH SPEED WIDE FAN IN CARRY LOOK AHEAD ADDER DESIGN USING MANCHESTER CARRY CHAIN

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**Abstract** - A Carry-Look ahead Adder (CLA) is a type of adder used in digital logic. A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits. The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. In this project, a new 8-bit carry chain adder block in multi output domino CMOS logic is proposed and using this carry chain block a 64 bit carry look ahead adder is implemented in 22nm strained silicon technology (PTM MOSFET Models) with a supply voltage of 0.8V. The even and odd carries of this adder are computed in parallel by two independent 4-bit carry chains. Implementation of wider adders (8-bit, 16-bit, 32-bit, 64-bit) based on the use of the proposed 8-bit adder module shows significant operating speed improvement compared to their corresponding adders based on the standard 4-bit MCC adder module.

(domino) CLA adder architecture with a regular, fast, and simple structure adequate for implementation in VLSI [9], [10]. The recursive properties of the carries in MCC have enabled the development of multi output domino gates, which have shown area-speed improvements with respect to single-output gates.

## 2. CLA DESIGN USING STATIC CMOS TECHNOLOGY

Carry look ahead logic uses the concepts of generating and propagating carries and the concept is shown in Table-1. To reduce the computation time, there are faster ways to add two binary numbers by using carry look ahead adders. These adders work by creating two signals P and G known to be carry propagator and carry generator respectively. The block diagram of the 4-bit carry look ahead adder is shown in figure-1

Table -1: Truth Table for Full Adder

| INPUTS |   |     | OUTPUTS |       | REMARKS             |
|--------|---|-----|---------|-------|---------------------|
| A      | B | Cin | SUM     | CARRY |                     |
| 0      | 0 | 0   | 0       | 0     | No carry generation |
| 0      | 0 | 1   | 1       | 0     |                     |
| 0      | 1 | 0   | 1       | 0     |                     |
| 0      | 1 | 1   | 0       | 1     | Carry propagation   |
| 1      | 0 | 0   | 1       | 0     |                     |
| 1      | 0 | 1   | 0       | 1     | Carry generation    |
| 1      | 1 | 0   | 0       | 1     |                     |
| 1      | 1 | 1   | 1       | 1     |                     |

**Key Words:** CLA, High speed adder, MOSFET, MCC, VLSI

## 1. INTRODUCTION

Addition is probably the most commonly used arithmetic operation, being often also the speed-limiting element to make faster VLSI microprocessors. As the demand for higher performance processors with increased sophistication grows, there is a continuing need to improve the performance and to reduce the area overhead while increasing the functionality of the arithmetic units contained within them. Carry look ahead (CLA) principle remains the dominant method in implementing fast adders. CMOS technology is widely used due to the overall merits in terms of speed, noise margin, power dissipation and fabrication cost. In this project, an efficient implementation of an 8-bit Manchester carry chain (MCC) adder in multi output domino CMOS logic is proposed. The carries of this adder are computed in parallel by two independent 4-bit carry chains. Due to its limited carry chain length, the use of the proposed 8-bit adder module for the implementation of wider adders leads to significant operating speed improvement compared to the corresponding adders based on the standard 4-bit MCC adder module. The CLA algorithm was first introduced in [8], and several variants have been developed. The Manchester carry chain (MCC) is the most common dynamic

INCLUSIVE OR, EXCLUSIVE OR, and NOT logical operations, respectively. In binary addition, the computation of the carry signals is based on the following recursive formula:

$$C_i = G_i + P_i.C_{i-1} \quad (1)$$

where  $G_i = A_i \cdot B_i$  is the carry generate signal (G) and the carry propagate signal is given by

$$p_i = A_i \oplus B_i \quad (2)$$

The sum bits of the conventional adders are given by

$$S_i = P_i \oplus C_{i-1} \quad (3)$$

where  $C_{-1}$  is the input carry( $C_{in}$ ).

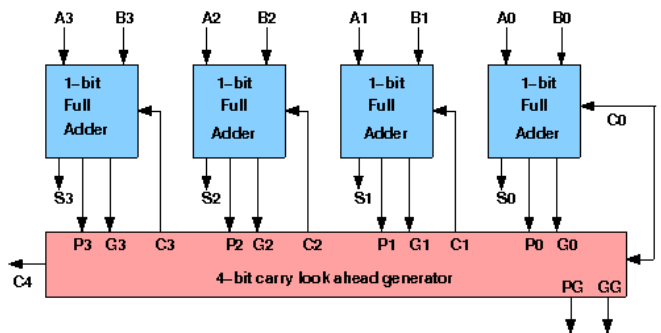
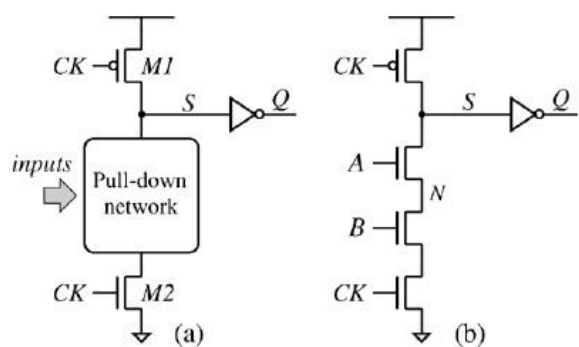


Fig -1: Block diagram of 4-bit carry look ahead adder

### 3. 64-BIT CLA DESIGN USING DOMINO CMOS TECHNOLOGY

Dynamic CMOS logic circuits are widely employed in high-performance VLSI chips in pursuing very high system performance. The largest difference between static and dynamic logic is that in dynamic logic, a clock signal is used to evaluate combinational logic. The feature of high speed and less area overhead of these logic circuits compared to other logic styles make them a popular choice in the design of high speed circuits [11][12][13]. Basically, it is an extension to dynamic CMOS logic in a sense that, a dynamic CMOS logic circuit followed by a static CMOS inverter makes it a domino logic circuit. Domino logic circuits are more widely used than their dynamic counterparts as the former can be easily cascaded. The high interest in domino circuits can be attributed to the fact that implementing a logic function with the help of domino logic requires less number of transistors compared to their static counterparts. Less number of transistors directly translates to lesser silicon area which effectively means that the manufacturing cost is lowered. Domino gates have faster switching speeds compared to static CMOS gates due to reduction in load capacitance. The main limitation of domino logic is less noise immunity. Therefore to improve the noise immunity of the domino circuit, a keeper circuitry must be added at the pull up network. The architecture of domino logic circuit is shown in figure 2



Domino logic gate. (a) Circuit schematic. (b) Two-input AND gate.

Fig -2: Architecture of Domino logic circuit

### 4. MANCHESTER CARRY CHAIN CARRY LOOK AHEAD ADDER

The advancement in semiconductor technology along with the shrinking device size has allowed for placement of billions of transistors in a single chip [14]. Since addition is the most commonly used arithmetic operation, adders are very important functional blocks in a VLSI processor. Improving the speed of adders will directly improve the speed of the processors because adders are one of the speed limiting circuits in the processors. The carry look ahead adders are attractive candidates for high speed addition since the carry delay can be improved by calculating each stage in parallel. Due to the simple structure and high speed, MCC adder is the most widely used domino carry look ahead adder architecture used in VLSI processors.[15],[16]. The major challenge in designing a dynamic CMOS circuit is the transistor sizing. The other limitations of domino logic circuits are charge sharing, noise immunity, leakage current and environmental and semiconductor process variations. The delay of combinational logic circuits can be minimized by varying the size of the transistors in the circuit. The size of the transistor can be varied by varying the width of the MOSFETs since the gate lengths of the MOSFETs used in a digital circuits are same [17]. The delay of the combinational logic circuits can be minimized by increasing the sizes of the certain transistors. As the CMOS technology advances, the power supply voltage ( $V_{DD}$ ) and threshold voltage  $V_{TH}$  of the transistors in dynamic (domino) circuits are decreasing [18]. The performance of the digital circuits degrades severely if the supply voltage decreases without the corresponding reduction in threshold voltage since the circuit speed depends on the over drive voltage  $V_{GS} - V_{TH}$ . In this chapter, a 64 bit MCC adder is implemented using 22nm technology with a supply voltage of 0.8V. This adder employs domino logic circuits for implementing the carry generate and carry propagate circuits but the sum circuits are implemented using static CMOS technology in order to reduce the area. In practice, the length of the carry look ahead adder is limited to four in order to reduce the number of transistors connected in series. In this MCC [19]-[24] adder, the generate and propagate circuits are implemented using domino logic and to generate the sum signals the domino chain is terminated and the sum circuits are implemented using static CMOS XOR gates.

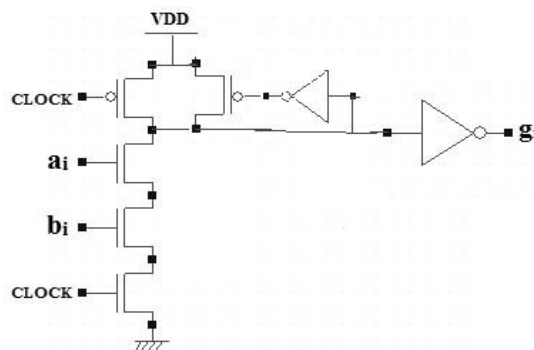


Fig -3: Domino implementation of carry generate circuit

### 5. NEW HIGH SPEED MCC BASED CARRY LOOK AHEAD ADDER

Let  $A = A_{n-1} A_{n-2} \dots A_1 A_0$  and  $B = B_{n-1} B_{n-2} \dots B_1 B_0$  represent two n-bit binary numbers to be added and their sum is represented by  $S = S_{n-1} S_{n-2} \dots S_1 S_0$ . The expression for carry signal in binary addition is given by

$$C_i = g_i + z_i \cdot C_{i-1} \tag{1}$$

where  $g_i = A_i \cdot B_i$  is the carry generate signal and the carry propagate signal is  $z_i = p_i = a_i \oplus b_i$

The sum bits of the conventional adders are given by  $S_i = p_i \oplus C_{i-1}$ , where  $C_{-1}$  is the input carry. The Manchester carry chain adder computes all the carries according to the equation

$$C_i = g_i + z_i \cdot g_{i-1} + z_i \cdot z_{i-1} \cdot g_{i-2} + \dots + z_i \cdot z_{i-1} \cdot \dots \cdot z_1 \cdot g_0 + z_i \cdot z_{i-1} \cdot \dots \cdot z_0 \cdot C_{-1} \tag{2}$$

In practice, the length of the carry look ahead adder is limited to four in order to reduce the number of transistors connected in series. In this MCC [18]-[24] adder, the generate and propagate circuits are implemented using domino logic and to generate the sum signals the domino chain is terminated and the sum circuits are implemented using static CMOS XOR gates. The MCC generates even and odd carries according to the relation (3)

The equations for the Even carries are given by [25]

$$\begin{aligned} h_0 &= g_0 + C_{-1} \\ h_2 &= G_2 + P_2 G_0 \\ h_4 &= G_4 + P_4 G_2 + P_4 P_2 G_0 \\ h_6 &= G_6 + P_6 G_4 + P_6 P_4 G_2 + P_6 P_4 P_2 G_0 \end{aligned} \tag{3-a}$$

The equations for the Odd carries are given by [25]

$$\begin{aligned} h_1 &= G_1 + P_1 C_{-1} \\ h_3 &= G_3 + P_3 G_1 + P_3 P_1 C_{-1} \\ h_5 &= G_5 + P_5 G_3 + P_5 P_3 G_1 + P_5 P_3 P_1 C_{-1} \\ h_7 &= G_7 + P_7 G_5 + P_7 P_5 G_3 + P_7 P_5 P_3 G_1 + P_7 P_5 P_3 P_1 C_{-1} \end{aligned} \tag{3-b}$$

where  $G_i = g_i + g_{i-1}$  and  $P_i = p_i \cdot p_{i-1} \cdot \dots \cdot p_1$ ,  $t_i = a_i + b_i$  and also  $g_{-1} = C_{-1}$  and  $t_{-1} = 1$ .

The sum bits can be calculated as follows

$$S_i = h_i \oplus p_i + h_{i-1} \cdot (p_i \oplus t_{i-1}) \text{ for } i > 0 \tag{4}$$

$$S_0 = p_0 \oplus C_{-1} \text{ for } i = 0$$

### CONCLUSIONS:

The MCC is an efficient and widely accepted design approach to construct CLA adders. In this report, we have presented a new Manchester design style that is based on two independent carry chains. Each chain computes, in parallel with the other, half of the carries. In this way, the speed performance is significantly improved with respect to that of the standard MCC topology. The proposed design technique has been applied for the implementation of 8-, 16-, 32-, and 64-bit adders in multi output domino logic, and the simulation results verified its efficiency. The simulation results, for the carry propagation delays, are presented in Table- 2. The PROPOSED design provides a performance improvement of 12.28% over the CONVENTIONAL design for the 8-bit adder. In this project, a 64 bit MCC adder is implemented using 22nm technology with a supply voltage of 0.8V. This adder employs domino logic circuits for implementing the carry generate and propagate circuits but the sum circuits are implemented using static CMOS technology in order to reduce the area. The proposed adder design has around 50% area overhead compared to the conventional MCC adder circuit design. The proposed circuit reduces the delay by increasing the area.

### REFERENCES

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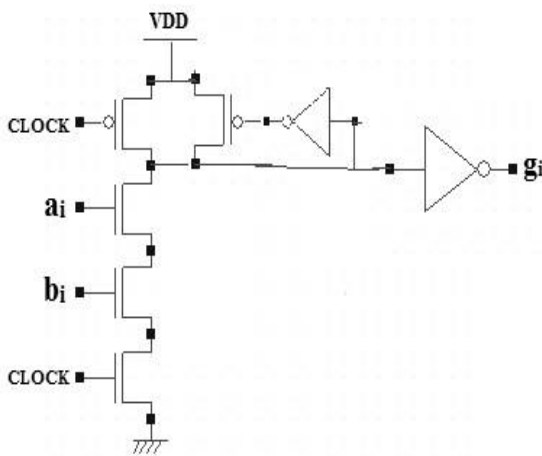


Fig -4: Domino implementation of carry generate circuit

Table -2: Performance Comparison of adders

| Type of Adder    | No. of bits | Delay for sum in Pico seconds | Delay for carry in Pico seconds | No of transistors required |
|------------------|-------------|-------------------------------|---------------------------------|----------------------------|
| Static           | 8           | 136.10                        | 126.70                          | 292                        |
| Domino           | 8           | 196.41                        | 147.84                          | 364                        |
| Conventional MCC | 8           | 102.05                        | 99.04                           | 300                        |
| Proposed MCC     | 8           | 98.84                         | 86.87                           | 582                        |

