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CLOUD RADAR DATA ACQUISITION PROCESSING USING KINTEX-7

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Abstract – *The paper describes different implementations for Digital receiver using filters. It also describes the various unique challenges associated with the design of a multi-channel wideband receiver. For radar data processing the digital Intermediate Frequency (IF) signals are down converted using filters. Parameters of radar signal are measured with high precision and accuracy using wideband digital receiver. The paper put forwards the use of different methods and their complications regarding memory. The major focus of the paper is to design a system having Solid state transmitter compatibility.*

Key Words: **Digital receiver**, **Intermediate Frequency**, **Solid state transmitter, multi-channel wideband receiver**, **Down Converted.**

1. INTRODUCTION

Radar is abbreviation of word Radio Detection and Ranging. Radar uses radio waves for detection of range, distance and angle of any object. The radar can basically contain a transmitter and receiver antennas. There are different types of radars differentiated as ground based radars, space borne radars and air borne radars. These radars operate at different frequency bands. In order to determine reflections different polarizations are preferred such as horizontal, vertical, circular as well as linear. Cloud radars are used to determine cloud boundaries and to estimate clouds properties, such as particle size and mass content, which aids in understanding how clouds reflect, absorb and transform radiant energy passing though the atmosphere. Cloud radars are basically used to determine the exact features of clouds such as density of clouds, moisture present in the clouds, direction of movement of clouds and velocity at which the cloud is moving. [11]

2. IMPLEMENTING DIGITAL RECEIVER USING MATLAB CODE

Generic IF Digital receiver used in cloud radars comprises of RF receiver, a mixer that translates RF signal to IF signal which is also fed up with a signal from local oscillator. Further the signal is converted from analog to digital signal using Analog to Digital Converter (ADC). The signal is down converted using Digital Down Converter (DDC) which mainly consist of set of filters as shown in Fig-1 describes block diagram of DDC with Cascaded Integrator Comb Filter (CIC), Compensating filters (CFIR) and Programmable filters (PFIR). A Matlab code is written for DDC block to obtain the decimated output.

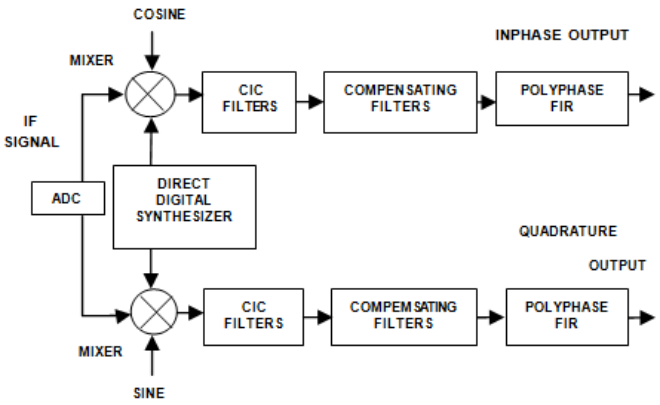

Fig -1: Block Diagram of DDC with CIC, CFIR and PFIR

Direct Digital Synthesizer (DDS) present in the DDC block generates arbitrary waveform from fixed frequency signal. Mixer output is achieved by mixing the signal with DDS to shift the signal spectrum from selected carrier frequency to baseband frequency. With the two complementary structures involved CIC can easily perform decimation as well as interpolation. CFIR cascaded eliminates the passband droop. The third stage of decimation is carried out by PFIR obtaining inphase and quadrature phase output. Using the Matlab implementation the number of taps obtained is determined as 130%. Increased number of taps increases the memory used. Thus in order to decrease the use of memory VHDL code is dumped into Kintex-7 board. [1]

3. PROPOSED METHODOLOGY

The KC705 evaluation board for the Kintex-7 FPGA provides a hardware environment for developing and evaluating designs targeting the Kintex-7. The KC705 board supports three of the five 7 series FPGA configuration modes such as Master Serial Peripheral Interface (SPI) flash memory using the onboard Quad SPI flash memory, Master Byte Peripheral Interface (BPI) flash memory using the onboard Linear BPI flash memory and Joint Test Action Group (JTAG) using a standard-A to micro-B USB cable for connecting the host computer to the KC705 board configuration port. Fig-2 shows the Kintex-7 system board. JTAG cable connector is used to dump the data to the Kintex-7 board. FPGA Mezzanine Card (FMC) is connected to the Low Pin Count (LPC) connector in Kintex-7 board.

Fig -2: Kintex-7 System Board

The Kintex-7 board uses a 2.5V LVDS differential 200MHz oscillator. It is obvious that the design philosophy for the digital receiver must capitalize on using the multi-channel high clock rate versions of filter design. After every processing stage of a decimation filter, the sample rate decreases. This leads to decrease in the memory and thus reduces the taps used. [8]

4. RESULTS

4.1 Output of DDC with CIC, CFIR and PFIR Filters

Matlab is written for DDC with the filters such as CIC, CFIR and PFIR decimating at 64, 2 and 2 respectively. FIR rate converter System object is created to resample the final output. A DSP System Toolbox System object is used to simulate the steady-state behavior of a fixed-point GSM DDC. Spectrum analyzers are used to generate the desired output from the code. Fig-2 shows the NCO Output.

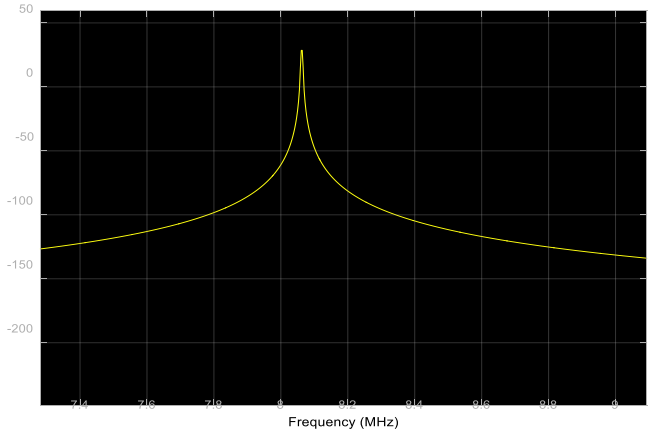

Fig -2: NCO Output

The Time Scope and Spectrum Analyzer System objects enable you to analyze the various stages of a DDC. Numerically Controlled Oscillator (NCO) Output and desired Decimated output is generated. Two Spectrum Analyzer System objects is created and configured to plot the power spectrum of the NCO output and of the compensated CIC decimator output. Fig-3 shows the Decimated Output.

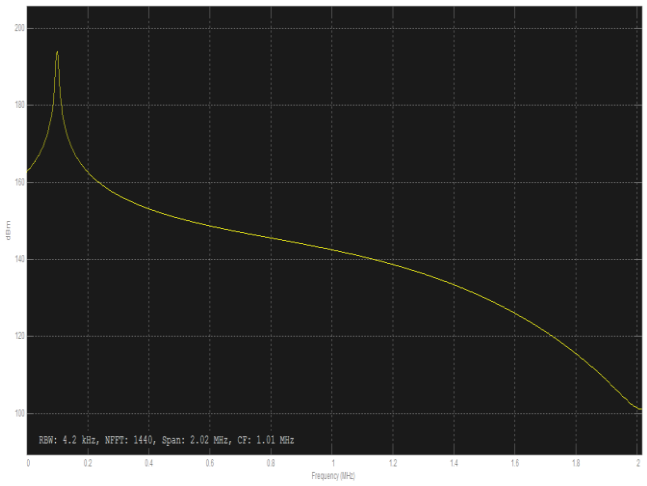

Fig -3: Decimated Output

4.2 Output of DDC using Kintex-7 FPGA

Kintex-7 evaluation board is fed with the VHDL code generated using Xilinx ISE 14.3. The output is analysed in spectrum analyser. Fig-3 shows the output for DDC using Kintex-7

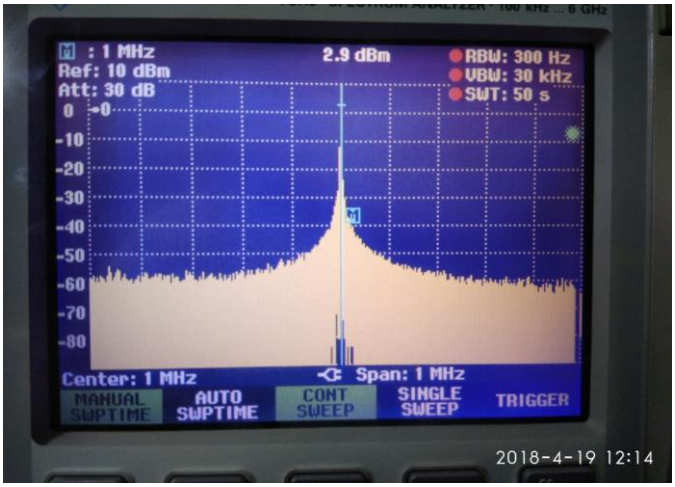

Fig -3: Output for DDC using Kintex-7

3. CONCLUSION

Cloud radar uses digital receiver for the receiving the transmitted data. This digital receiver mainly consists of various set of filters such as CIC, CFIR and PFIR. CIC filters used can eliminate the multiplication operation. It also eliminates the use of memory module but the major drawback of CIC filter is the passband droop. This passband droop can be reduced using CFIR along with CIC filters. Operation of the receiver is verified using various different codes. When verified using Matlab code we can estimate that the number of taps are increased to about 130%. Increased number of taps can ultimately increase the use of memory. Thus similar procedure is verified using hardware kit Kintex-7. This Kintex-7 board is dumped with VHDL codes reducing the number of taps to 8%.

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