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To Design 16 bit Synchronous Microprocessor using VHDL on FPGA

Abhilash Wanjari[1], Nihal Bisen[2], Mohan Chaudhari[3], Sujay Rajak[4], S.P Washimkar[5]

[1,2,3,4] *Student & department of electronic and telecommunication, Pce Nagpur,Maharashtra ,India*
[5]*Assistant professor & department of electronic and telecommunication , Pce Nagpur, Maharashtra, India*

Abstract - *The project aims at designing a 16 bit synchronous microprocessor using vhdl and the implementation of its components in FPGA (Field Programmable Gate Array).The project gives description of design and simulation of the modules like the ALU(Arithmetic and logic unit), ROM(Read only memory), RAM(Random Access Memory), Instruction Fetch, Instruction Decode, control Unit. The microprocessor can perform Arithmetic instruction, logical instruction, load and store. After simulation, schematics generation and timing analysis is carried out in Xilinx ISE simulator. The individual modules are implemented and tested in.*

***Key-Words:* - Microprocessors, FPGA, VHDL,ISE,HDL**

1. INTRODUCTION

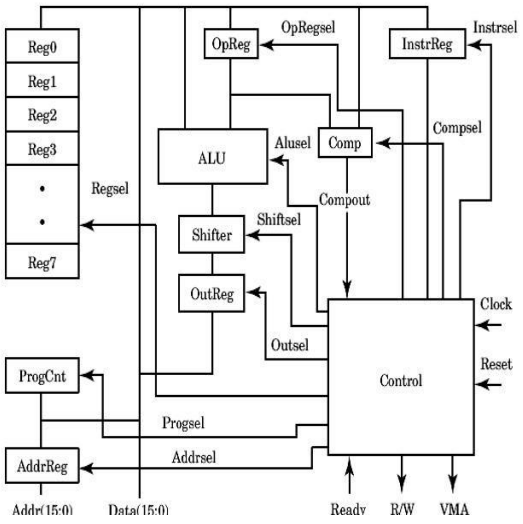
16 bit microprocessor contains quantity of essential modules which is together composed the processor. The processor using 16 bit data bus for communicate from various blocks like General purpose registers, Arithmetic logic unit, CU (control unit), memory, comparator, program counter, address register, instruction register and shift register. With the development into integrated circuit technology the strength of the processor get increased tremendously. Microprocessors are extensively used into the embedded sector rooted on general purpose application and special purpose application. Microprocessors are used in instruments to make it intelligent using behavioral encoding. The CPU design by various sections which is beneficial in performing diffrent functions.

A system computer architecture from associating certain flexibility to software by high execution of hardware through processing by a very versatile high-speed compute texture as field-programmable gate arrays (FPGAs). The task by re configurable processor into embedded system creation microprocessor-based products either systems. The target by plan was to make a 16 bit micro- processor usage VHDL language. It is a too zestful project. VHDL language is a general purpose language also present language get various features. The major purpose by these project is until gland each of these aspect side by side to design a mini CPU, calibrate that functionality this can be make by synthesis.

1.1Block diagram of processor:

A microprocessor is programmable tool it Take in digital data inputs, procedure that according from the instruction stored into that memory and supply effect as output. that may be look as a programmable logic device it may be used to command a growth either until turn on/off devices. The Microprocessor may be look when a data processing unit either an computing unit by a computer. This has computing and decision-making ability identical to the central processing unit by a computer. Presently, the microprocessor is entity used into a wide spectrum to yield called microprocessor-based products either systems. The target by plan was to make a 16 bit micro- processor usage VHDL language. It is a too zestful project. VHDL language is a general purpose language also present language get various features. The major purpose by these project is until gland each of these aspect side by side to design a mini CPU, calibrate that functionality this can be make by synthesis.

The fig.1.shows the block diagram of easy 16 bit microprocessor. The processor catch a mark by essential pieces. There is an register array by eight 16 bit registers, there is an arithmetic and logic unit, a shifter, a program counter, an instruction register, a comparator, an address register, and a control unit. Each of these blocks connected via a generic 16 bit tristate data bus [5]. This have 16 bit address bus.



A. Alu

The control block supply each of the control signals by adjust data traffic instead of the CPU. The control block is a too large state machine in order that contains a lap of states instead of each instruction *ALU*

The Prime VHDL component part is the Arithmetic and logic unit or ALU. The ALU is the basic building block by the central processing unit from a computer. Depend into where the ALU is designed that manage make the CPU much effective. that execute a deal of arithmetic and logical

operations similar similarly add and subtract and some logical manipulation such as AND, OR, and XOR.

B. Comparator

The comparator match two values also returns a „1" or „0" depend at the sample by comparison.The compare method is chosen through the significance of input port sel. through input a and b are similar set the value eq since port sel. through ports a and b go through the common value, the port output returns „1" and if only the values are not equal, certainly output returns „0".

C. Control

The control section supplies the essential signal to texture the data flow properly via the CPU also perform the required functions. Into the program the architecture contains a state machine so causes each convenient signal tariff to update rooted towards the present state also input signals also making a next state instead of the state machine. The command get a some inputs also a lot by outputs.

Perform each of the states instead of an instruction executions the essential moves from complete the instruction.

D. Register

The register section is applied instead of the address register also the instruction register. These registers are applied from hold at the input data on a increase edge by the clock input also drive output with the hold data.This contains three ports. Port is the input port also q is the output port. Port clk (clock) controls as the data is picked into the register entity. When a flourish edge happens towards input clock, the tariff by input a is fixed since output q. This also accept 1 nanosecond obstacle to remove delta obstacle problems till simulation.

E. Register Array

The reg array block is used until through the set of registers inside the CPU in order to used, To store intermediate tariff during instruction. From write a location into the reg array elected input sel (select) from the location since to be written , input data through the data until be written , also set a increase edge in the input clk (clock). since read a location by reg array, set input sel until the location towards get read and set input en to a „1"; the data is output on port q.

F. Shift

The next device to be described is the shift. The shift block is used to perform shifting and rotation operations within the CP It has a 16 bit input bus, and a 16 bit output bus and a select input that

Determines which shift operation to perform. The shift entity can perform a shift left, shift right, also rotate left, also rotate right operation.

G. Tri register

The tri register is related towards the data bus also can stand information through the data bus also into the same time expedition information by the data bus.

2. COMPOSITION AND TESTING:

The ALU inputs A also B are the two input buses at which the ALU manipulation are featured. Output bus C regress the result by the ALU operation.Input select (sel) patch up which of the arithmetic either logical operation is performed.

Set input	operation
0000	Addition
0001	Substraction
0010	Multipication
0011	Division
0100	Anding
0101	Oring
0110	Xoring
0111	Noring
1000	Xnoring

Table 1.ALU Function Table

The table displays the comparison modes and values. every operations function into two input values also return a single bit output. present bit is applied to command the stream by manipulation inside the processor as long as executing instructions. The comparator lie by a large case statement where all branch to the case statement contains a IF. If state tested is real, a „1" value is fixed; else „0" is fixed. Every statement take place after 1nanosecond to discard delta delay problems.

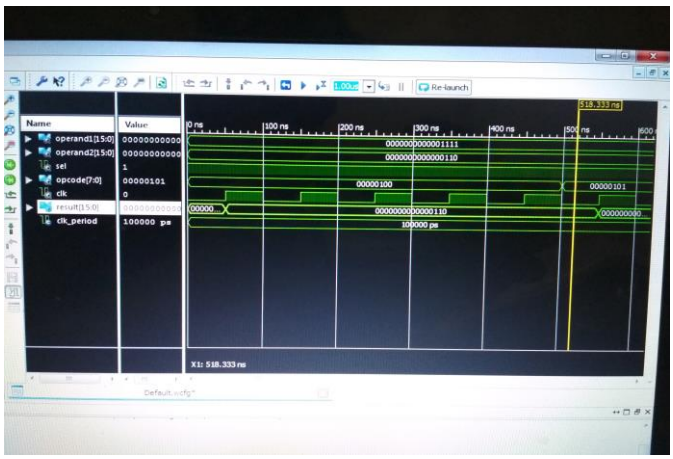


Chart -1: Simulation of logical unit

The suitable work from the processor is validated. The simulation result demonstrate so the processor is eligible by implementing the given modules into the design.through the programming keep done in VHDL, an VHDL simulator is applied to test the functionality by the CPU. The VHDL RTL report by the CPU is spurious by a task VHDL simulator. This way we keep used Model Sim SE 6.5 simulator also xilinx ISE 13.2. An simulator requirement two inputs, the description through the design also the stimulus until drive the design. occasionally formation are self-stimulating also not require any external stimulus, but at most state VHDL designers utilization a VHDL test bench of one kind either another until drive the design entity tested.

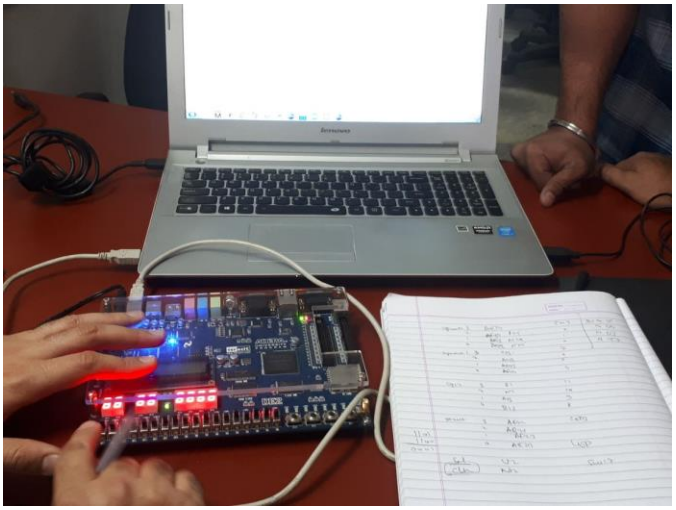


Fig -1: Altera DE2 board

3. CONCLUSIONS

Microprocessors are a mass storage device. They are the advanced form of computers. They are also called as microcomputers. The impact of microprocessor in different lures of fields is significant. The availability of low cost, low power and small weight, computing capability makes it useful in different applications. 16 bit processors have high performance and power than 8 bit processor and low power consumption than 32 bit processors. VHDL is also a very useful hardware description language. It is a very powerful language with numerous language constructs that are capable of describing very complex behavior. In our project we have designed a 16 bit CPU . The CPU is described by a number of lower-level components that are instantiated to form the CPU design. In our work we have done the VHDL coding of the CPU and simulated it successfully. We also have tried to implement it in FPGA Kit but due to the hardware problem we couldn't do it.

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