Investigation of Multicarrier PWM Topologies for Five Level Cascade H-Bridge Multilevel Inverter (CHMLI)

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Abstract - *Multilevel inverter (MLI) can achieve high power efficiency at medium voltage inverters in industrial application. It can generate stepped waveform by reducing harmonic distortion with increase in the number of voltage level; a full bridge is known as H-bridge inverter because it shows alphabet 'H'. In this paper, Multicarrier PWM topologies and there Modulation schemes are discussed. The Modulation index is varied to analyze its effect on Voltage THD. This paper also presents the comparison of Multicarrier PWM topologies controlled Cascade H-Bridge multilevel Inverter in terms of THD. The simulation result shows that vertically shifted PWM topologies has superior performance when compared to other-SPWM. The simulation of circuit is done by using MATLAB/Simulink.*

Key Words: **Multilevel Inverter, Modulation Index, Multicarrier PWM topologies, Total Harmonic Distortion(THD).**

1. Introduction

Grid connected inverter structures are gaining importance due to the increase in demand on renewable energy sources. Typically, the conventional two-level inverter is used for grid-connected operation. Nevertheless, the conventional inverter has a high degree of harmonic distortions, which impact the performance of the electrical equipment. Also, conventional inverters are vulnerable to the effect of electromagnetic noise sources such as wireless equipment. Reducing the distortion demands an additional filtering to meet the IEEE standards for Distribution Generation (DG) interconnection. Moreover, the higher DC voltage link necessitates a larger DC link and auxiliary capacitors which are very bulky at higher voltage, it has also a higher rate of voltage (V) change with respect to time (t) (dV/dt), which leads to a transient overvoltage (TOV) that may damage equipment such as switchgears due to exceeding their rates and saturating the magmatic cores of the transformers and motors connected to the grid. The conventional two-level inverter uses relatively high switching frequency and large series inductance connected to the output circuit of the converter to fulfill the required Total Harmonic Distortion THD.

To cope the raising challenges associated with the conventional two-level inverter, multilevel inverters are introduced as an improved design to power system-tied inverters. The multilevel inverters are combined of multi-cascaded-circuits, and each circuit is designed to handle a portion of the total output wave signal (voltage). The design concept of the multilevel inverter circuitry leads to the use of electronic components with low switching frequency and low voltage rating comparing with the traditional two-level inverter. The multilevel design allows using MOSFET/IGBT switching components with low power loss; hence the inverter system efficiency is improved.

2. Multilevel Inverter

The inverter is a power electronic circuit which converts the DC to AC power. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms[1]. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig.1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions.
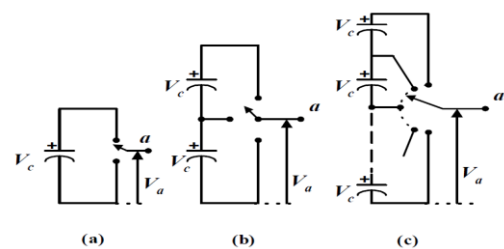

Fig 1: One phase leg of an inverter with (a) two levels, (b) three levels, (c) n levels

A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor, while the three-level inverter generates three voltages, and so on. The term multilevel starts with the three level inverter. By increasing the number of levels in the

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inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped), capacitor-clamped (flying capacitors) and cascaded multi-cell with separate dc sources[3][4][5]. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM).

The most attractive features of multilevel inverters are as follows.

1. They can generate output voltages with extremely low distortion and lower dv/dt.
2. They draw input current with very low distortion.
3. They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
4. They can operate with a lower switching frequency.

The amplitude of the fundamental component of the AC output phase voltages for m-level can be found by the following expression,

$$\hat{V}_{an} = \frac{(m-1)V_{DC}}{2}m_a$$

The amplitude of the fundamental component of the AC output line voltages for m-level can be found by the following expression,

$$\hat{V}_{ab} = \frac{\sqrt{3}}{2}(m-1)V_{DC}m_a$$

3. Cascade H-Bridge Multilevel Inverter

Figure 2 shows the 5 level CHB MLI consist of two H-bridge combine with a series of the power conversion cell. Cascaded H-Bridge Multilevel Inverter is better than the diode clamped inverter and flying capacitors inverter, it requires less number of the component in each switching levels. In Cascade H-Bridge Multilevel Inverter, the grouping of switches and capacitors is called H-bridge consisting of isolated DC Voltage source. The switching states of one leg of

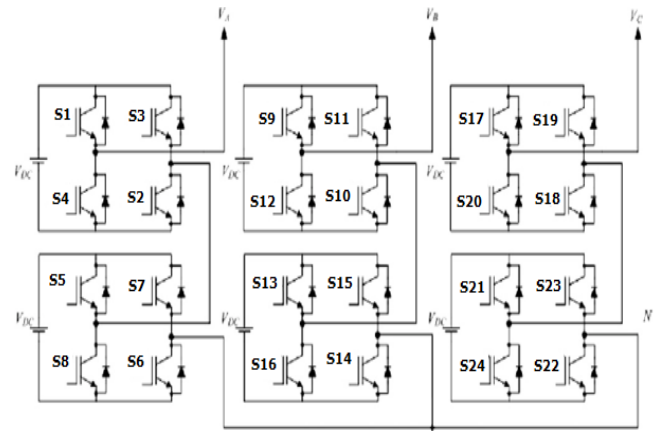three phase 5-level CHBMLI is shown in table 1. Also the 5-level phase voltage is shown in Figure 3

Fig 2: Three-phase Five level Cascaded H-Bridge Inverter

Table -1: Switching states and output voltage for leg-1 of three phase 5-level CHB-MLI

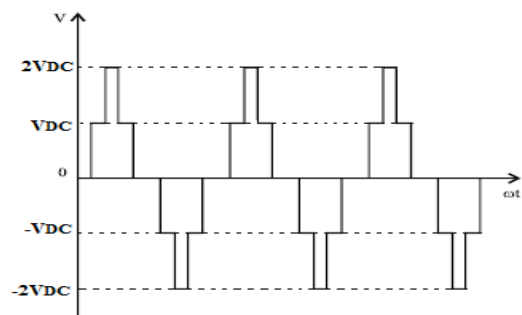| Switching States HB1				Switching States HB2				V_{ao}
S1	S3	S4	S2	S5	S7	S8	S6	
1	0	0	1	1	0	0	1	$2V_{dc}$
1	0	0	1	0	0	1	1	
1	0	0	1	1	1	0	0	
0	0	1	1	1	0	0	1	V_{dc}
1	1	0	0	1	0	0	1	
0	0	1	1	0	0	1	1	
0	0	1	1	1	1	0	0	
1	1	0	0	0	0	1	1	0
1	1	0	0	1	1	0	0	
1	0	0	1	0	1	1	0	
0	1	1	0	1	0	0	1	
0	1	1	0	1	1	0	0	
0	1	1	0	0	0	1	1	$-V_{dc}$
0	0	1	1	0	1	1	0	
1	1	0	0	0	1	1	0	
0	1	1	0	0	1	1	0	$-2V_{dc}$

Fig 3:Output Phase Voltage of Three-phase Five level Cascaded H-Bridge Inverter

4. Sine Pulse Width Modulation

SPWM for Multilevel Inverter is based on classic two level SPWM with triangular carrier and sinusoidal reference waveform. Only difference between two level SPWM and multilevel SPWM is, numbers of carriers are used in multilevel SPWM. For 'm' level inverter 'm-1' carrier are used[9]. Interaction of particular carrier and reference is used to generate gating signal for particular complementary pair of switches in diode clamped or capacitor-clamped inverter, or particular cell in multi-cell inverter. Carriers used in multilevel inverter may be vertically shifted or horizontally shifted as shown in Fig 4(a),(b)[12][13]. Advantage of horizontally shifted carriers scheme is that, each modules are switched on and off with a constant number of times by period, independently of magnitude of generated voltage as shown in Fig 5 at m_f=21. But vertically shifted carrier scheme can be more easily implemented on any digital controller[10].
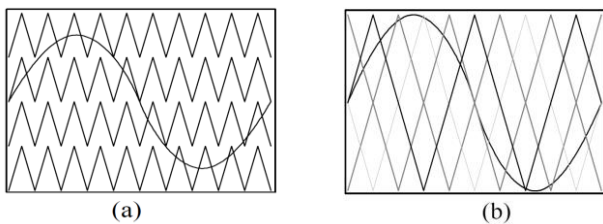

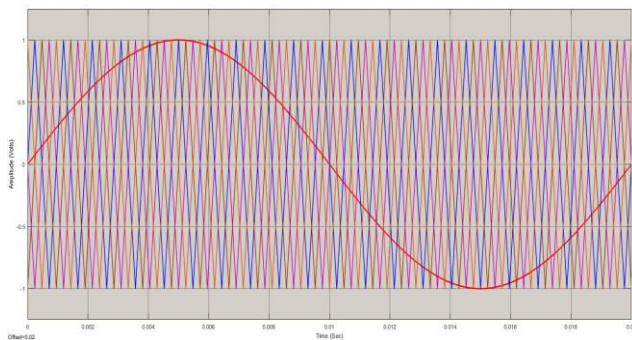Fig 4 (a) Vertically shifted carriers (b) Horizontally shifted carriers

Fig 5 Horizontally 90º Shifted Carriers Waves

Vertically shifted scheme comes with three variant, as shown in Fig 6, 7 , 8 & 9 at m_f=21.

1. All carriers are in phase [Phase Disposition (PD)]
2. All carries above the zero reference are in phase, but in opposition with those below [Phase Opposite Disposition(POD)]
3. All carriers are alternatively in opposition [Alternate Phase Opposite Disposition(APOD)]
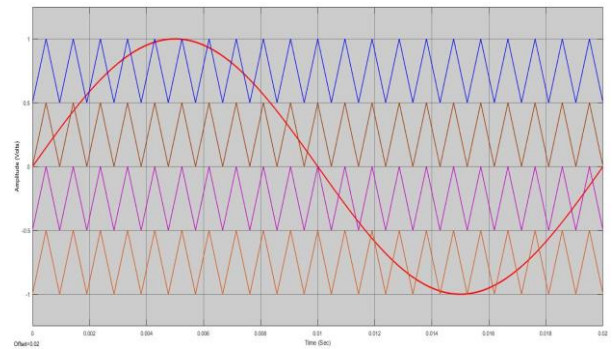4. All carriers are Vertically shifted by 90º
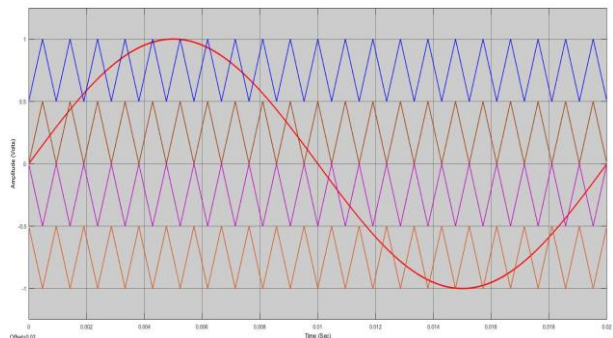

Fig 6 Phase Disposition Carriers Waves

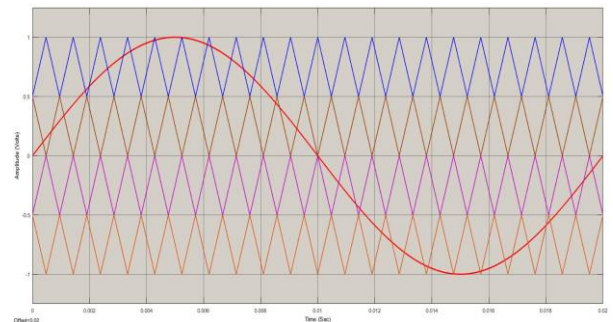Fig 7 Phase Opposite Disposition Carriers Waves

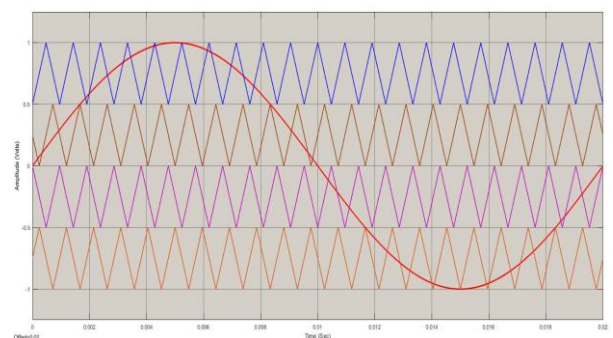Fig 8 Alternate Phase Opposite Disposition Carriers Waves

Fig 9 Vertically 90º Shifted Carriers Waves

5. Total Harmonic Distortion (THD)

Harmonic distortion is caused by nonlinear devices in power system. A nonlinear device is one in which current is not proportional to applied voltage. IEEE Standard 519-1992 recommends the requirements for harmonic control in

electrical power systems. The quality of Output voltage of inverter strongly related to total harmonic distortion.THD is the measure of effective value of harmonic components of a distorted waveform.

$$THD_V = \frac{\sqrt{\sum_{h>1}^{h\,max} V_h^2}}{V_1}$$

Where h is characteristic harmonic order, V_h is harmonic voltage and V_1 is fundamental voltage.

$$THD_I = \frac{\sqrt{\sum_{h>1}^{h\,max} I_h^2}}{I_1}$$

Where h is characteristic harmonic order, I_h is harmonic voltage and I_1 is fundamental voltage. Fast Fourier transform (FFT) is used to do the spectral analysis of phase voltage and current of inverter output and used as useful tool for THD calculations. The algorithm requires a large amount of calculations but with MATLAB simulation software, calculations are done easily.

6. Simulation & Results

All Multicarrier PWM topologies (PD, POD, APOD, 90º Shifted-Horizontally & Vertically) based 5-level Cascade multilevel inverter has been simulated with RL load in MATLAB software as shown in Figure 11. The simulation output of 5-level CHBMLI is presented in this section. The reference sinusoidal wave frequency is taken as 50 Hz and frequency modulation is varied as tabulated in table 2 and the load is taken as 4KVA, 0.86 power factor. The output phase voltage waveforms of all PWM techniques based CHBMLI is shown in Figures 12 to Figure 16.
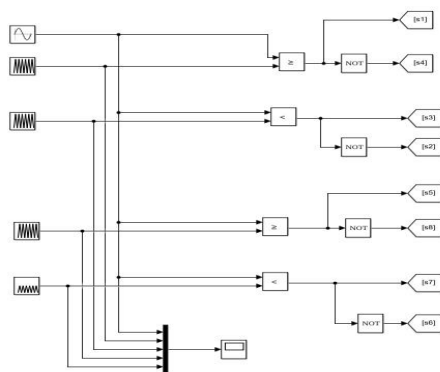

Fig 10: Modulating & Carrier Wave Comparison for one leg of three phase 5-level CHB-MLI
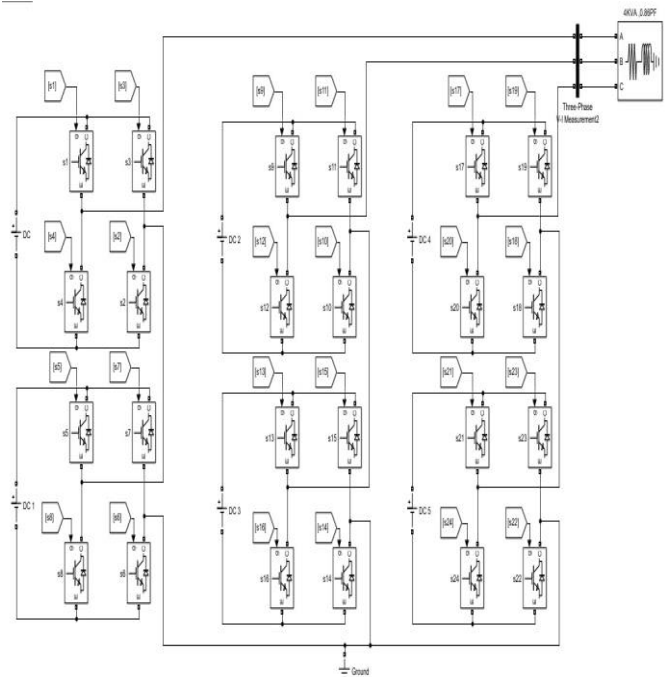

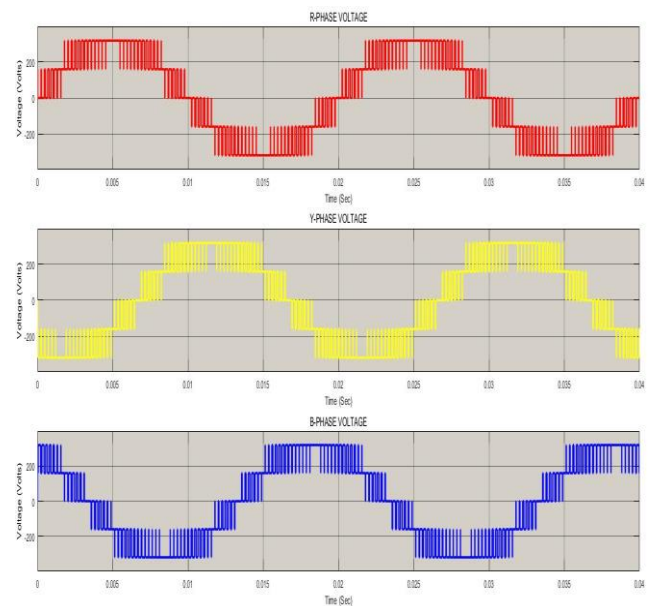Fig 11: Three-phase Five level Cascaded H-Bridge Inverter MATLAB Model

Fig 12 Horizontally 90º Shifted Carriers Waves Output Phase Voltage Waveforms

From table 2 it can be observed that in PD,POD & APOD the THD_v is almost same but at m_f =27, 39 APOD gives better results compared to other Multicarrier PWM topologies whereas when m_f=21, 33 vertically 90º shifted Multicarrier PWM provides lower THD_V .The FFT analysis of best results are shown in Fig 17, 18, 19 & 20.
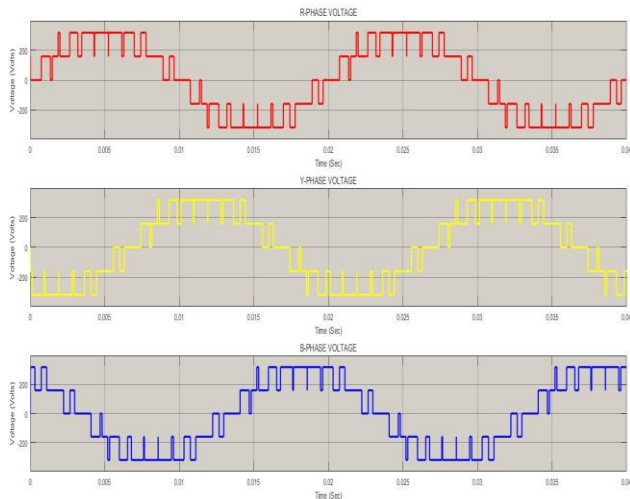
Fig 13 Phase Disposition Carriers Waves
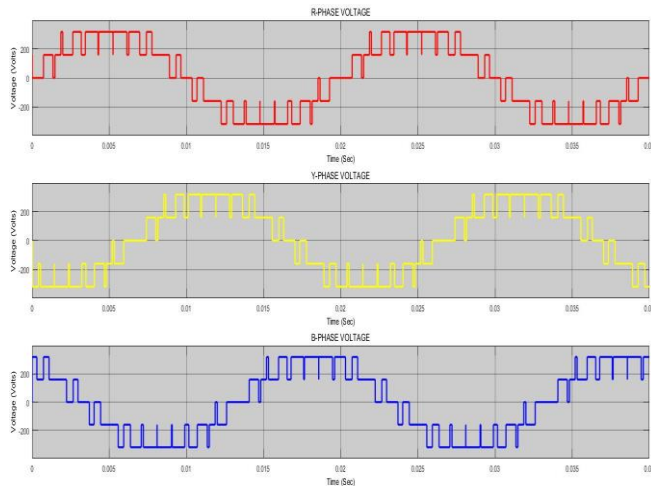Output Phase Voltage Waveforms

Fig 14 Phase Opposite Disposition Carriers Waves
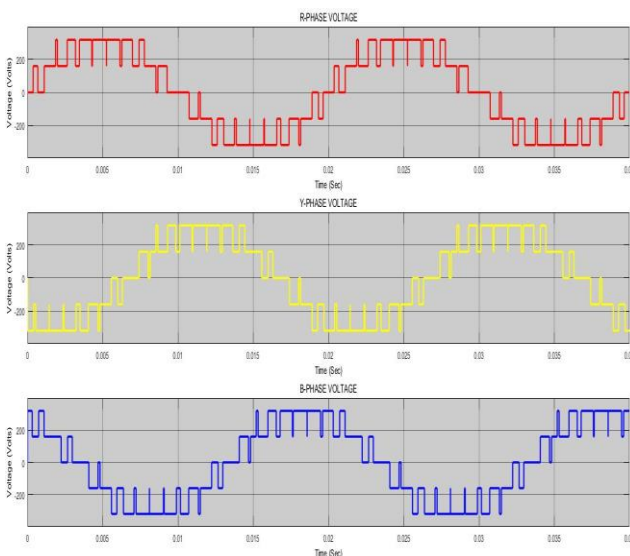Output Phase Voltage Waveforms

Fig 15 Alternate Phase Opposite Disposition Carriers
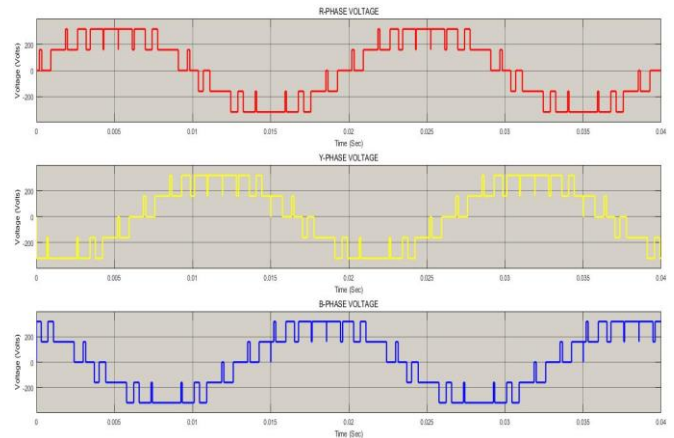Waves Output Phase Voltage Waveforms

Fig 16 Vertically 90º Shifted Carriers Waves
Output Phase Voltage Waveforms

Table -2: Switching states and output voltage for leg-1 of
three phase 5-level CHB-MLI

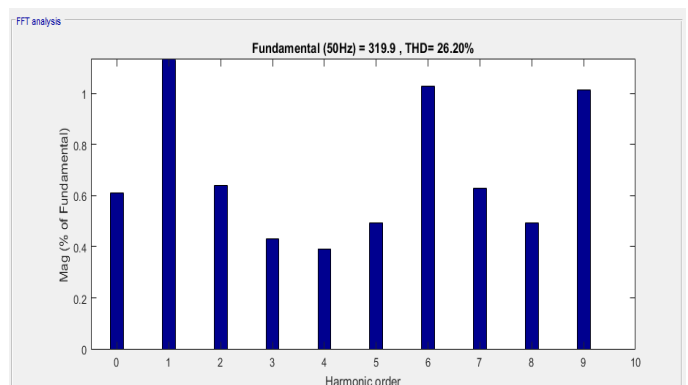| Frequency Modulation m_f	Multicarrier PWM Topologies	PD THD$_V$ (%)	POD THD$_V$ (%)	APOD THD$_V$ (%)	Vertically 90º Shifted THD$_V$ (%)	Horizontally 90º Shifted THD$_V$ (%)
21		26.78	26.78	26.78	26.20	26.87
27		26.92	26.92	26.91	27.25	27.03
33		27.04	27.04	27.03	26.66	26.97
39		26.93	26.93	26.92	26.97	26.94

Fig 17 FFT Analysis of Vertically 90º Shifted THD$_V$ (%)
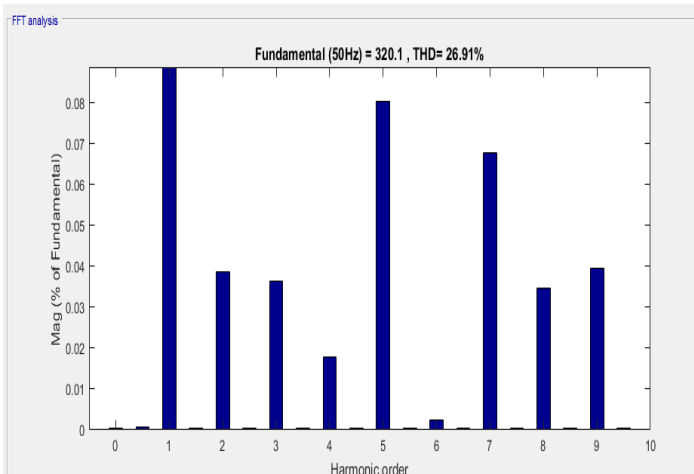(m_f=21)

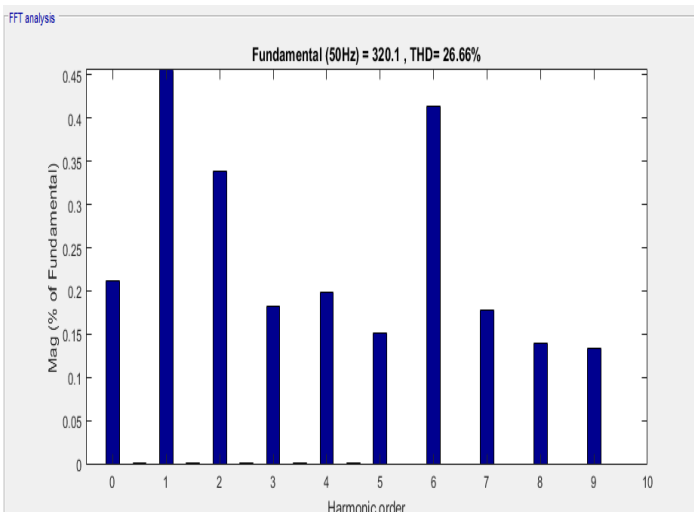Fig 18 FFT Analysis of APOD THD_V (%)
(m_f=27)

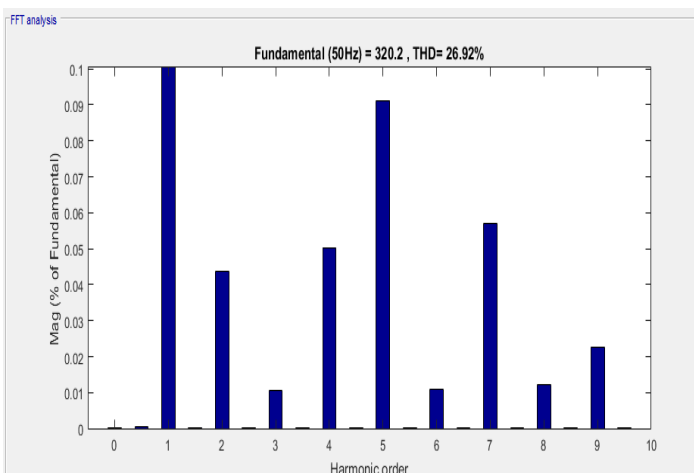Fig 19 FFT Analysis of Vertically $90°$ Shifted THD_V (%)
(m_f=33)

Fig 20 FFT Analysis of APOD THD_V (%)
(m_f=39)

7. CONCLUSION

For controlling multilevel inverter different modulation scheme are used. Of these different modulation schemes SPWM method has gained more interest in industrial application. In this paper different Multicarrier PWM topologies has been studied and there results are tabulated in table 2. From the table 2 it can be evident that vertical carrier modulation topologies (PD, POD, APOD & $90°$ Shifted) has best results in terms of output phase voltage total harmonic distortion(THD).

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BIOGRAPHIES

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