GENERATION OF HIGH VOLTAGE USING COCKCROFT -WALTON VOLTAGE MULTIPLIER CIRCUIT

Amit Kumar Sinha¹, Rajeev Kumar²

¹Asst.Professor, Dept.of Electrical Engineering, Axis Institute of Technology & Management, Kanpur.
² B.Tech, Student, Electrical Engineering, Axis Institute of Technology & Management, Kanpur.

Abstract - The objective of the project is to design a voltage multiplier which should be able to multiply voltage from an input as low as 12 Volts to a maximum output of approximately 200 Volts. As High Voltage DC (HVDC) transmission is becoming more popular in the present scenario of bulk power transmission over long distance transmission, it is required to study the testing of various insulation materials at laboratory level in under graduate and post graduate course curricam. Since, generation and handling of high voltage is very dangerous and required skilled personnel in the laboratory. In addition, it is very much costly. Cockcroft-Walton multiplier provides suitable high DC voltage source from a low input voltage i.e. 230 V AC supplies which is rectified by using half wave rectifier circuit. Designing of the circuit is based on Cockcroft Walton Principle that consists of ladder network of Capacitor and Diodes. Other specifications considered carefully while designing multiplier and components must be used based on size consideration for expected load current and expected output voltage. Finally, the results are compiled from the simulations done on MATLAB. A prototype was designed and experimental result was tested and demonstrate was purpose.

Key Words: HIGH VOLTAGE, DC, VOLTAGE MULTIPLIER CIRCUIT, COCKCROFT-WALTON MULTIPLIER

1. INTRODUCTION

In many application, the used of high voltage with low power supply devices are needed in communication, biomedical equipment, high voltage testing and any other field are in high demand. Depending on the application the converted power ranges from some Watts to values above 100kW while output voltages above 1kV up to a few 100kV are needed. The aims of this paper is to design a high voltage low power supply device that can produce high voltage up to 10 kV with lowest current and power values. On top of that, the powers supply device is small in size, simple and low cost. Generation of high DC voltages is mainly required in research work in the areas of pure and applied physics. Sometimes, high direct voltages are needed in insulation tests on cables and capacitors. Impulse generator charging units also required high DC voltages of about 100 to 200 kV. Normally, for the generation of high voltages DC around100 kV, the output currents are about 10 mA.
Fig 1: Cockcroft-Walton multiplier

Where, $C_1, C_2, C_3, ..., C_n$ = Capacitor and $D_1, D_2, D_3, ..., D_n$ = Diode. And $I_{D_1}, I_{D_2}, I_{D_3}, ..., I_{D_1}$ = Diode Current. The advantages of Cockcroft-Walton Multiplier circuit are low in cost, small in size and can be easy to insulate the circuit. Another advantage of voltage of multiplier circuit is its peak to peak voltage at each stage will be double.

Consider operation of two stages Cockcroft-Walton multiplier is shown in figure 1.

1) When $T_s$ is negative, then Capacitor $C_1$ charges through Diode $D_1$ to $V_{max}$.
2) When $T_s$ is positive, then $V_{max}$ add arithmetically existing potential $C_3$ thus $C_2$ charges to $2V_{max}$ through Diode $D_2$.
3) Again $T_s$ is negative, $C_3$ charge $2V_{max}$ through Diode $D_3$.
4) Again $T_s$ is positive, Capacitor $C_4$ charge Diode $D_4$ to $4V_{max}$.

Therefore output of multiplier = $V_{max} \times N$

Where,

$N$ = Number of stages.

Designing of Multiplier circuit most commonly half wave circuits are used. And because of the multiplier circuit, high voltage develops at the output side of the Cockcroft-Walton multiplier circuit.

Design of Cockcroft voltage multiplier is simple Careful consideration of all component parameters is the only way to insure both reliable and predictable circuit performance.

3. Design of Cockcroft-Walton Multiplier Circuit

This circuit is consisting of series parallel combination of diode to achieve the blocking voltage as required. Also, the rating of capacitor is matched to withstand the voltage level in a each stage. Cockcroft-Walton multiplier has different construction. In this paper half wave "Cockcroft-Walton" multiplier is shown.

$$2\delta V = q \sum_{n=2}^{2n} \frac{1}{C_n} \quad (1)$$

$$q = IT \quad (2)$$

$$q = \frac{1}{f} \quad (3)$$

$\delta V$ is amount of ripple generated by the system, since it passes through $C_2, C_4, C_6, ...$ only because these capacitor columns is known as smoothing column as voltages through these circuit remain constant. Whilst the voltage through $C_1, C_3, C_5, ...$ oscillates in same manner as supply varies that is the reason it is known as oscillating column. 

$q$ is amount of charge injected to smoothing circuit.

For n stage total ripple is given by:

$$2\delta V = q \left( \frac{1}{C_{2n}} + \frac{2}{C_{2n-2}} + \frac{3}{C_{2n-4}} + \frac{4}{C_{2n-6}} + ... + \frac{n}{C_2} \right) \quad (4)$$

From above it is clear that the voltage ripple generally depend on the lowest capacitor hence size of capacitor at lowest end can be kept smaller. However, due to loading effect and other un-avoidable condition this may create a severe damage to the system hence it is advisable to keep this value identical.

$$C_{2n} = C_{2n-2} = C_{2n-4} = C_{2n-6} = ... = C_2 = C$$

As putting the above identical values equation (4) can be written as

$$\delta V = \frac{1}{2fC} \left( \frac{n(n+1)}{2} \right) = \frac{1}{fC} \left( \frac{n(n+1)}{4} \right) \quad (5)$$

It is very much obvious from the equation (5) that the voltage ripple is constant and depends on the number of stage. As number of stages increases the ripple content is increases proportional to $n(n+1)$ . Variation of ripple with number of stage is given in figure 4. As it is clear that the variation is non-linear after $n=10$ and $n=11$ stages, still it is comparable that till lower stages and ripple can be linearised.

Fig 2. Variation of Ripple Voltage with number of stages in Cockcroft Walton.

In addition, ripple is function of number of stages and number switching frequency for a fixed capacitor design. Hence, varying frequency ripple can be reduced and can be treated as high frequency switching. In the present work, diode drop is neglected for the sake of simplicity and to reduce the complexity of the circuit equations. Also, parasitic effect of diode and capacitor is neglected as its contribution is very small. There are two modes of
operation of CWVM viz. no load operation, and operation under loaded condition. When load is applied there will be some drop due to internal behavior and load applied. That drop is considerably high and reduces the output voltage in a great manner.

Total drop $\Delta V$ is given by:

$$\Delta V = \Delta V_n + \Delta V_{n-1} + \Delta V_{n-2} + \ldots + \Delta V_1$$

![Fig. 3 Variation of Drop Voltage for a fixed frequency](image)

As to get a fixed stage of output voltage with constant frequency and capacitor value, optimal number of stage can be calculated. Again, this equation number is considered when number of stages is assumed.

![Table 1. Parameter Value for Simulation](image)

### Table 1. Parameter Value for Simulation.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Numerical Value [unit SI]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage to Primary of X’mer $V_2$</td>
<td>230 [V]</td>
</tr>
<tr>
<td>Secondary Voltage</td>
<td>10000 [V]</td>
</tr>
<tr>
<td>Supply Frequency, f</td>
<td>50 [Hz]</td>
</tr>
<tr>
<td>Capacitor, C</td>
<td>100 [nF]</td>
</tr>
<tr>
<td>Number of Stages, n</td>
<td>7</td>
</tr>
</tbody>
</table>

4. SIMULATION AND RESULTS

With values given in table I, one can simulate this model with a fixed rating of all elements. Voltage drop through diode is neglected.

![Fig. 4 Circuit Arrangements in Simulation](image)

Fig. 6 shows the simulation arrangement in this figure scopes are the virtual oscilloscope where the visualization of voltages are taken. It can be used as recording purpose also.

![Fig. 5 Voltages of Source and Stage-1, 2](image)

Simulation shown in Fig 4 is simulated in MATLAB environment for various numbers of runs and with 20 seconds run till the stable output is not achieved. After proper stable condition Fig. 7 is plotted for the stage output of stages 5, 6, & 7.
REFERENCES


BIOGRAPHIES

Amit Kumar Sinha was born in Jamshedpur (Jharkhand), India, in 1991. Currently, He is working as Asst.Professor in Axis Institute of Technology and Management, Kanpur. He received B.E (Electrical and Electronics) and M.E (Power Electronics and Drives) from Anna University, Chennai. His area of intrest includes Control System, Power Electronics, Electrical Machines and Power Quality.

Rajeev Kumar was born in Madhubani (Bihar), India, in 1996. He is doing B.tech (Electrical Engineering) from Axis Institute of Technology and Management, Kanpur. His area of intrest includes Power Electronics, Electrical Machines and Power System. He is a student member of Institute of Electrical and Electronics Engineers (IEEE).