

IMPLEMENTATION OF CARRY SKIP ADDER USING PTL

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Abstract - In majority of electronics applications, performance of devices are taken into consideration. Adder is considered as one of the important operations in these devices. So the performances such as area, power and delay should be enhanced. This paper presents the design and implementation of Carry Skip Adder which uses pass transistor logic to enhance the performance parameters.. Here comparison is done between conventional CSKA and Proposed CSKA in-terms of power, delay, area and number of transistors used in the design. Schematic and implementation of complete project is done in Cadence Virtuoso 6.1.4 software at 90nm technology.

Key Words: VLSI, CSKA, PTL, ALU, RCA, FA, HA

1. INTRODUCTION TO ADDERS

The demand for electronics devices is increasing day by day which requires the use of power efficient VLSI circuits. Thus these circuit computation speed needs to be increased by enhancing the performance parameters such as area, power and delay. Number of transistors is the primary concern in the complex devices as it affects the area, power and delay.

Adders are one of the essential blocks of most of the digital applications. In many of the arithmetic applications and other applications, adders are used in Arithmetic logic unit and most of the processors. Addition is utmost vital operations and it will result in sum bit and carry bit. There are two forms of adder, they are binary adder and multi-bit adder. Binary adders are full adder (FA) and half adder (HA). Multi-bit adder or complex adder architectures are constructed from the binary adders. Binary adder is the basic building block of any adder design. In this paper, CSKA implementation using pass transistor logic is done. Pass transistor logic has the advantage that it uses less gates compared to CMOS logic.

2. CONVENTIONAL CSKA

Conventional carry skip adder is constructed by placing full adders in parallel to form a Ripple carry adder and for carry propagation it uses 2:1 mux and propagate block. In the conventional carry skip adder, carry is skipped to i^{th} bit position without waiting for the rippling. This is done by using the skip logic, which is nothing but the 2:1 multiplexer.

The working principle of CSKA is that it operates in 2 stage, they are generating sum bits from the Ripple Carry Adder block and the carry propagation block. Propagation block uses EXOR gates to generate the propagate bits and the generated bits are fed to the AND gates. The result of propagation block is given to the selection line of multiplexer, which selects the carry.

In order to construct a 16 bit conventional Carry skip adder, it requires a total of 920 transistors. This can be divided as 608 transistors for RCA, 232 transistors for propagate block and 80 transistors for 2:1 multiplexer. The conventional 16-bit Carry Skip Adder is shown as below,

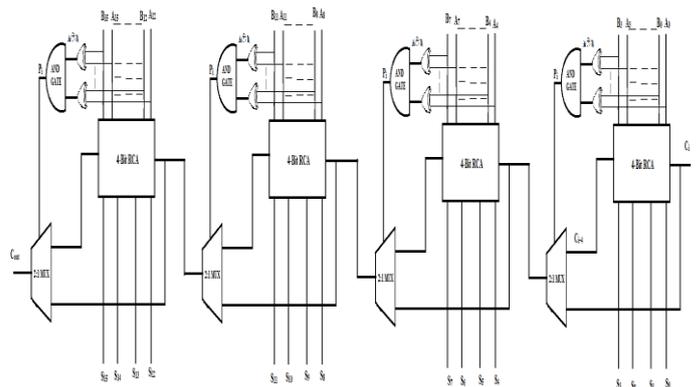


Fig -1: Conventional 16-bit CSKA

3. PASS TRANSISTOR LOGIC

Pass transistor logic forms one of the essential logic families in integrated circuit design. Pass transistor acts as a switch to pass the signals from input to the output. Pass transistors are used in most of the application as it reduces the transistor count in the circuit design, also they are faster and consumes less power compared to the CMOS logic.

There are two types of PTL they are PMOS type and NMOS type. PMOS type transmits strong 1's and weak 0's. NMOS type transmits strong 0's and weak 1's. In this paper, NMOS type is used for the design. The output voltage is given by $V_G - V_{TH}$. Pass transistor is shown as shown in figure below,

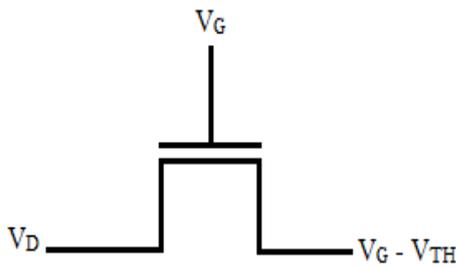


Fig -2: General Pass Tansistor

4. PROPOSED CSKA

The proposed carry skip adder architecture is constructed using pass transistors. Here only the full adder and multiplexer are constructed using PTL and propagate block is similar to that of the conventional CSKA. The proposed CSKA requires 472 transistors to construct and the working principal is exactly similar to the conventional CSKA, only difference is the internal structures, which can be shown in figures 3 and 4.

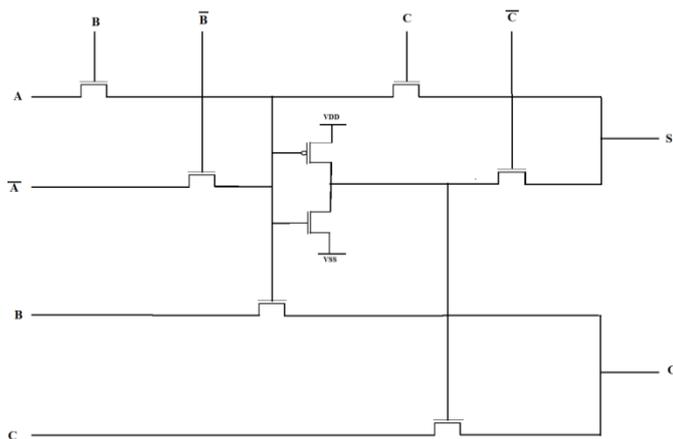


Fig -3: Internal Structure of FA using PTL [9]

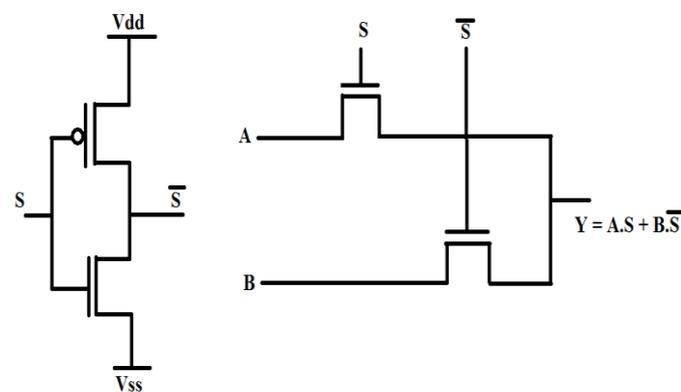


Fig - 4: Internal structure of 2:1 MUX using PTL

5. SIMULATION AND COMPARISON

Simulation of both proposed and conventional carry skip adder is carried out in Cadence Virtuoso 6.1.4 software in 90nm technology and the results are compared. Results and comparison is shown below,

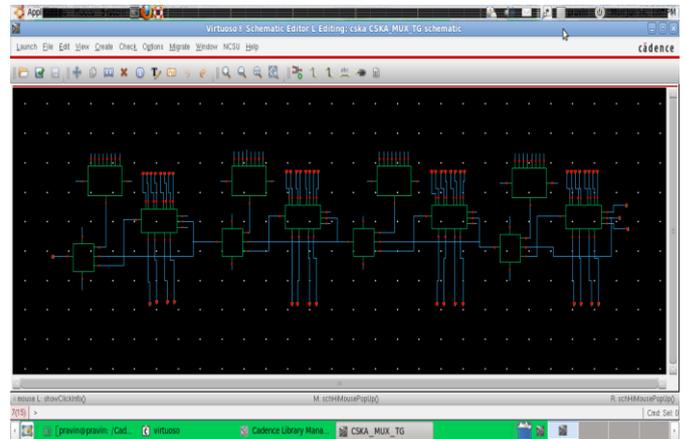


Fig -5: Schematic of proposed CSKA

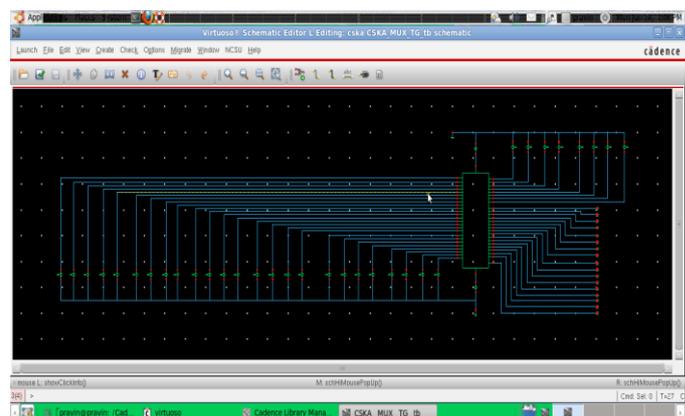


Fig -6: Test Bench of proposed CSKA

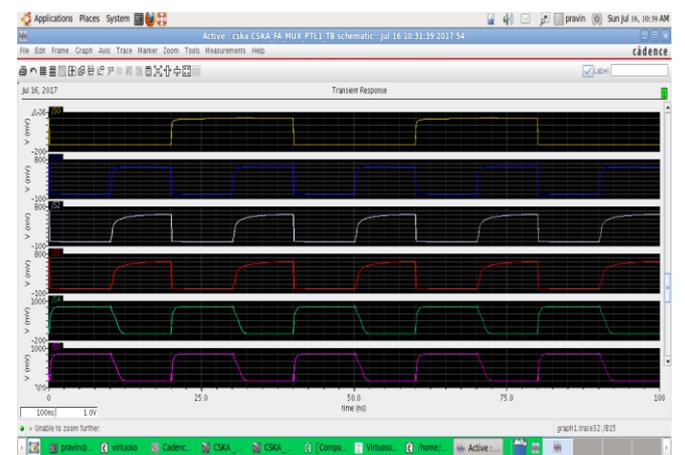


Fig -7: Output showing from S₀ to S₅ of proposed CSKA

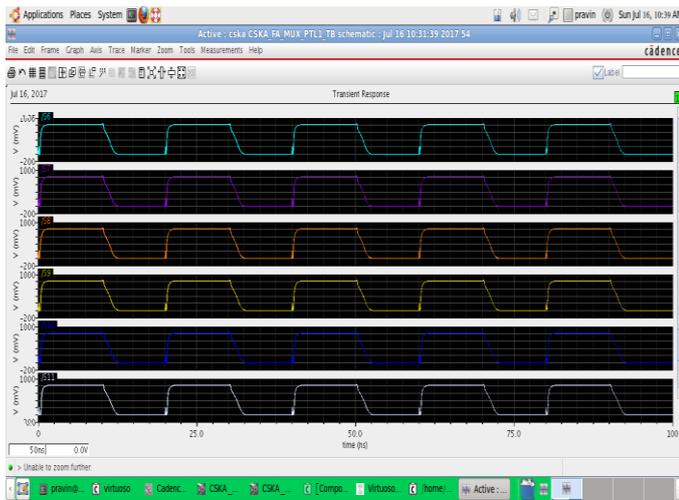


Fig -8: Output showing from S_6 to S_{11} of proposed CSKA

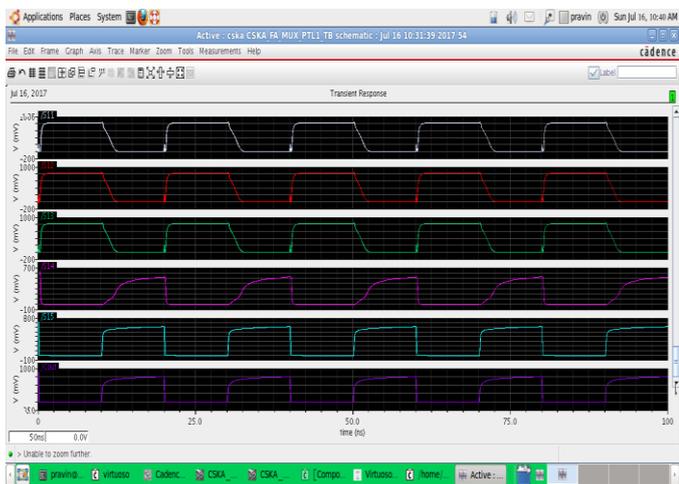


Fig -9: Output showing from S_{12} to S_{15} and C_{out} of proposed CSKA

Table -1: Comparison of Conventional CSKA and Proposed CSKA

Factors	Conventional CSKA	Proposed CSKA
Number of Transistors	920	472
Area	782 μm^2	272 μm^2
Delay	136.8 ps	38.61 ps
Average Power	494.1 mW	351.2 mW

6. CONCLUSION AND FUTURE SCOPE

The proposed CSKA using pass transistor logic has achieved major enhancement compared to that of the conventional CSKA. From the Table 1 we can see that transistor count, area, delay and average power, are nearly

halved compared to the conventional CSKA. Thus the proposed CSKA is a good competitor for low power and high speed electronic applications. In future, the proposed CSKA can be enhanced as there is voltage drop since PTL cannot output the same voltage level of the input voltage.

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