

Solid State Fault Current Limiter for Improvement of Smart Grid Performance

Karthigha.D¹,Sathiya.K²,Nirmala.S³

Department of Electrical and Electronics Engineering,
Prince Shri Venkateswara Padmavathy College of Engineering, Chennai-128

Abstract - One of the most important topic regarding the application of Solid State Fault Current Limiter (SSFCL) for upcoming smart grid is related to its possible effect on the reduction of abnormal faults current. Due to the grid connection of the micro grid with the current power grid, excessive fault current is a series problem to be solved for successful implementation of smart grids. In this paper SSFCL is implemented by integrating the simulink and simpower system blocks in MATLAB. The designed SSFCL model is easily utilized to reduce the fault current for various kinds of smart grid system. Typical smart grid model including generation, transmission, and distribution with dispersed energy resource is modeled to find the performance of the SSFCL. As a dispersed energy resource, 10MVA wind farm is considered for simulation. Three phase fault have been simulated in smart grid and effect of SSFCL has been evaluated.

Key Words: SSFCL, FCL, SFCL, GTO, SSCB.

1. INTRODUCTION

In today circumstances, due to the rapid development of smart grid network the occurrence of fault become high. The levels of fault current in many places have often exceeded the withstand capacity of existing power system equipment. As a result security, stability and reliability of power system will be negatively affected. Thus, limiting the fault current of the power system to a safe level can greatly reduce the risk of failure to the power system equipment due to high fault current flowing through the system. Because of that, there is no surprise to fault current limiting technology has become a hotspot of fault protection research since this technology can limit the fault current to a low level. In power system design view, limiting the fault current to a low level can reduce the design capacity of some electrical equipment in the power system. This will lead to the reduction to the investment cost for high capacity circuit breakers and construction of new transmission line. Consequently, from both technical and economical points of view, fault current limiting technology for reducing short circuit current is needed.

2. FAULT CURRENT LIMITING TECHNIQUES

Fault Current Limiter (FCL) is a variable-impedance device connected in series with a circuit to limit the current under fault conditions. The FCL should have very low impedance during normal condition and high impedance

under fault condition. On the basis of the above characteristic, various types of FCL have been developed. Some of these FCL are based on superconductor, power electronic switches and tuned circuit impedance. The fault current limiting technology has become hotspot in power system protection research. However, the research are concentrated on the superconducting and power electronic switches types of FCL. FCL is a device that has potential to reduce fault level on the electricity power networks and may ultimately lead to lower rated components being used or to increased capacity on existing systems. Electricity industry is very attracted in such devices, providing that FCL offer them satisfaction in economics aspect as well as technical constraints. Fault current limitation is a vital part in power system protection.

2.1 Fast Interrupting Devices:

Fast interrupting devices can be separated into two types, fault current limiting fuses and solid-state circuit breaker (SSCB). Fault current limiting fuses consist of a thin wire that simply melts when the current is too high. While fuses are very reliable, they have practical drawbacks. First, it takes a certain minimum amount of time before the wire heats up enough to melt. Once installed, it is not possible to change the sensitivity of a fuse, or how much current it will take to melt it. Then, once the wire melted, it has to be physically replaced before the connection can be re-established. This usually means a time delay for restoring the connection. Fuses are used for radial feeders in distribution systems, the desired sensitivity of fuse is fixed and the time delay for restoring service is considered acceptable because only a small number of consumers are affected. This circuit breaker employs a high speed switch and a surge arrester. There are various combinations of solid state switches but generally, all share the same concept. During normal operation, the semiconductor switch is continuously on. However, during fault occurrence, the switch is turn off.

2.2 Fault Current Limiting Devices:

Fault current limiting devices can be segregated into three types: the tuned circuit impedance current limiter, the superconducting fault current limiter and the solid state fault current limiter. The tuned circuit impedance current limiters normally exploit tuned circuit or non-linear elements that produce an increase of impedance at the

sensing of fault current. The net impedance of the resonance circuit can rapidly increase when the switch is triggered. The nuisance of this FCLs is that it is bulky, expensive tuning is very critical. Superconducting FCL can be classified into two types; resistive and inductive. Resistive SFCL is simplest the type of SFCL to visualize its concepts. A superconducting section of the power lined switches from zero resistance to a significant resistance when either the critical current, I_c , or the critical magnetic field, H_c , is exceeded within the material.

2.3 Fault Current Limiting And Interrupting Devices:

Fault current limiting and interrupting devices (FCLID) can limit the fault current and is capable of fully interrupting it at any desired delay-time after fault interception. This device consists of GTO thyristor contribute to the current limiting action. The basic structure of the FCLID is very simple and similar to the SSFCL. However, its operation differs to one another. During normal operation, the varistor is short circuited by the GTO thyristors which are in the on-state. On detection of fault, GTO thyristors switched off at pre-set value and the fault current is diverted to the varistor. When the transient over-voltage suppressed and varistor current decrease, the GTO switch is turned on again and so on. This operation will be repeated for some period of time. If the over current still occur more than this specified period of time, the GTO thyristors are permanently turned off.

3. SOLID STATE FAULT CURRENT LIMITER MODELING

This paper will be based on simulation of SSFCL in smart grid system. In order to congregate data to be analyzed, simulation model of SSFCL need to be modeled. SSFCL modeling is the vital part throughout this paper and need to be model appropriately. SSFCL used in this paper consist of two parallel connected circuit branches with one branches connected to the solid state switches comprising of only two thyristors connected in inversely parallel manner and the other branches, two thyristor connected in inversely parallel but with current limiting impedance (reactor) connected in series with it. The first branch (with thyristors switch only) acts as the main circuit breaker used to clear the fault when it occurs. The first branch is normally closed and conducts current during normal operation. Nevertheless, when the magnitude of the current exceeded a pre-set level, the switches will open the circuit instantly interrupting the current flow. The switches from the other branch (with thyristors and current limiting reactor in series) are normally open and have no continuously current rating during normal condition. Its function is to conduct fault current to facilitate operation of the conventional protective device on the load side of the SSFCL. A proper design of fault current limiting device including its control strategy will ensure the fault current in the system is kept as low as

possible in order to limit the surge current of the thyristors and also to minimize stresses on the distribution system.

4. SIMULATION MODEL

Figure 1 shows the basic configuration of the SSFCL consisting of two parallel connected solid state switches. The first branch (Thyristor Branch 1) consists of thyristors switches and the other branch (Thyristor Branch 2) consists of thyristor and current limiting reactor. Switches are connected in inversely parallel manner for both branches. Surge arrester used to protect the system from voltage surge during switching.

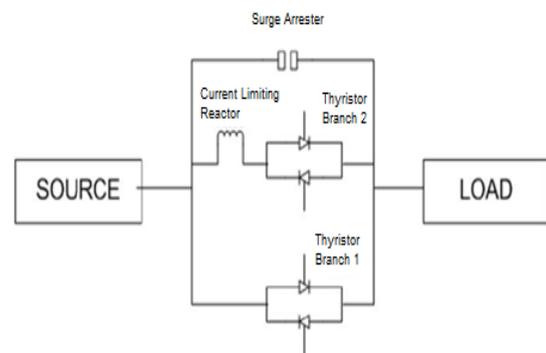


Fig -1: Solid state fault current limiter modeling

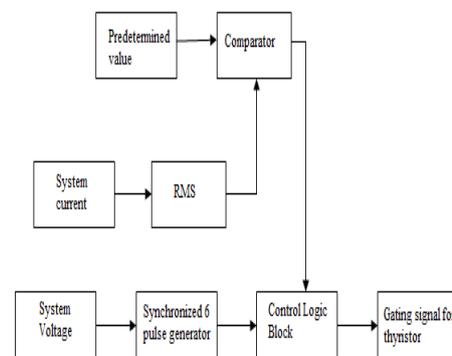


Fig -2: Block diagram for SSFCL Control system

The control system of the SSFCL is shown in term of block diagram in Figure 2. In the operation of SSFCL, fault current need to be detected promptly before it becomes harmful to other equipment. The fault current detection is done by comparing RMS current level with a predetermined reference value. The output from the comparator used to generate switching signals for the thyristors.

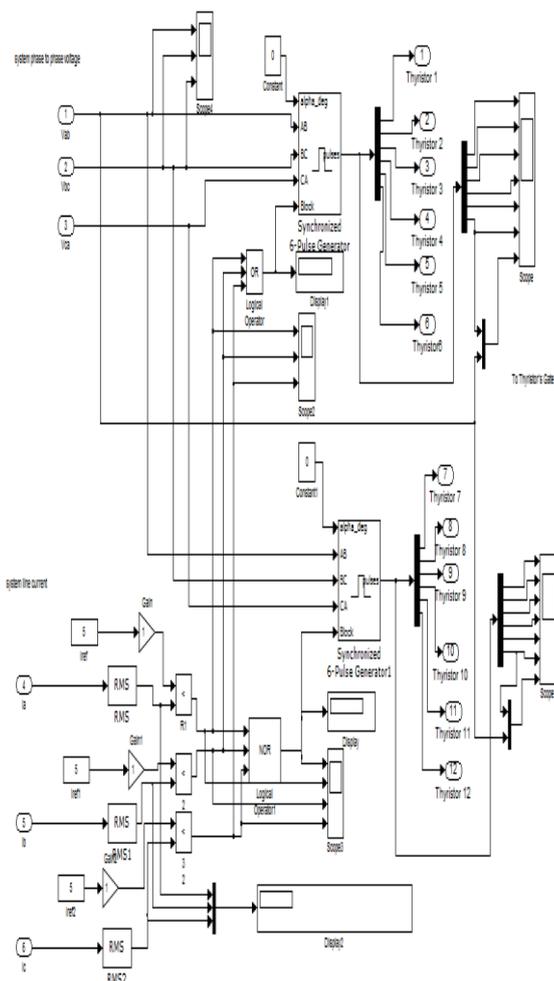


Fig-3: SSFCL control system

Figure 3 shows the simulation model of SSFCL control system used in this work. During PRE-FAULT period, comparator will produce output “0” to allow the operation of Synchronized 6-Pulse Generator 1 and output “1” to block the operation of Synchronized 6-Pulse Generator 1. During FAULT period, comparator sensed line current is exceeded pre-set value and produce output “1” to block operation of Synchronized 6-Pulse Generator and output “0” to allow the operation of Synchronized 6-Pulse Generator 1. Note that, thyristors 1, 2, 3, 4, 5 and 6 were control by Synchronized 6-Pulse Generator and the rest were control by Synchronized 6-Pulse Generator 1. Simulation model of SSFCL shown in Figure-4 is developed using simulation tools in MATLAB, SIMULINK. The SSFCL consist of two parallel connected solid state switches in each phase, one is formed by thyristors and the other one is formed by thyristor with current limiting reactor in series. Each switch connected in inversely parallel.

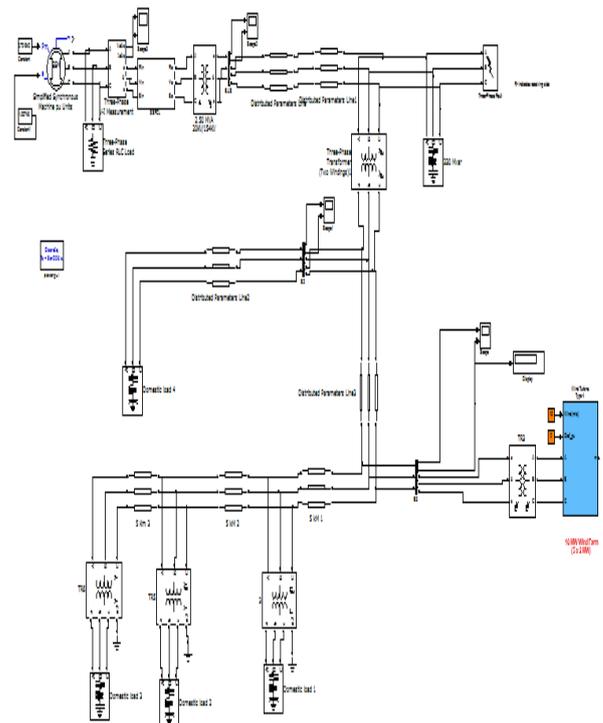


Fig-4: smart grid model

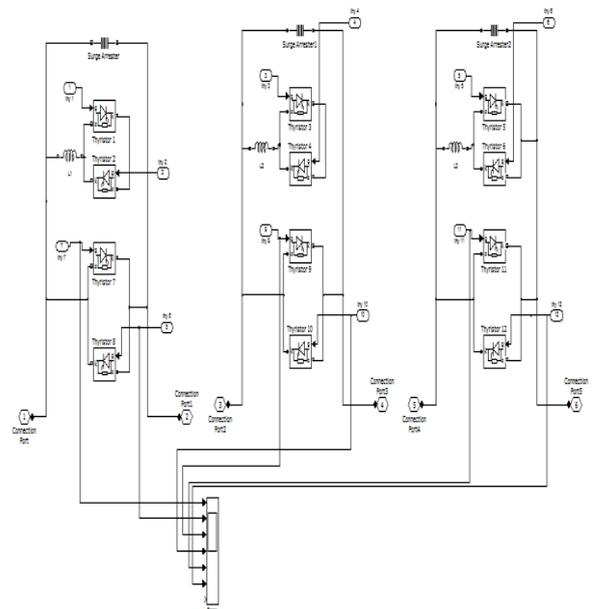


Fig-5: SSFCL Circuit

An arrester is connected in parallel to protect the system from overvoltage during switching operation. In figure 4, the power system is composed of 100 MVA conventional power plant, composed 3 phase synchronous machine, connected with 200km long 154 KV distributed parameter transmission line through a step up transformer TR1. At the substation (TR2), the voltage is stepped down to 22.9KV from 154KV. High power industrial load (6MW) and low power domestic load (1MW each) are being supplied by

separate distribution branch networks. The wind farm is directly connected with the branch network B1 through transformer TR3 and is providing power to the domestic loads. The 10MVA wind farm is composed of five fixed – speed induction type each having the rating of 2MVA. At the time of fault, the domestic load is being provided with 3MVA out of which 2.7 is being provided by the wind farm. Figure 5 shows that the simulation model of SSFCL circuit.

5. RESULT AND DISCUSSION

To analyze the performance of smart grid during insertion of SSFCL, simulations were carried out using the MATLAB Simulation Tool: SIMULINK. Simulations were performed by considering a test system. To simulate a fault condition, three phase fault were applied on the system.

5.1 Three Phase Fault

Three phase fault or balance fault is the most severe fault that could occur in the power system.

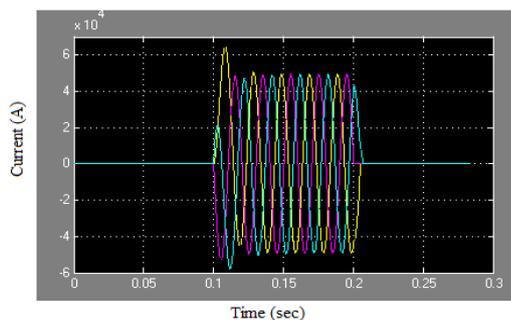


Fig-6: System Without SSFCL For ThreePhase Fault

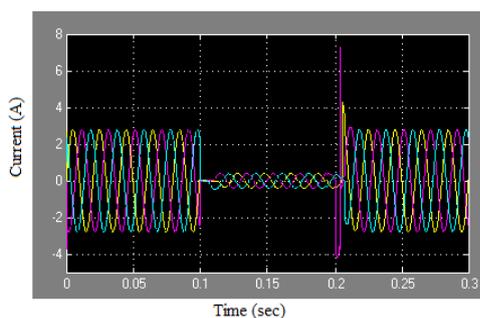


Fig-7: System with SSFCL For ThreePhase Fault

Figure -6 envisage the current waveforms of the distribution radial system without SSFCL when three phase fault occurred in the system. It can be seen for three phase fault, all three phases experiencing high current flowing through the lines. Figure -7 shows the similar system and condition of fault with inclusion of SSFCL in the system. Within the quarter-cycle after fault detection, the limiter starts limiting the fault current. After the first transient

current, the SSFCL is able to reduce 45 kA fault current to 0.4 A.

6. CONCLUSION

This paper presents the impact of SSFCL in smart grid. SSFCL has been used here as a circuit breaking element and as a fault current limiter. SSFCL not only limits the fault current, but also improves the smart grid performance. A simulation model of SSFCL and its control system for the power system is developed and verified. The simulation model of smart grid system is used to test its performance while inserting SSFCL during three phase fault. Comparison of current has been made between the smart grid system without SSFCL and the system with SSFCL for various types of faults. Simulation results proved that SSFCL effectively limit the current during fault incident.

REFERENCES

- [1] Umer A.Khan, J.K.Seong, S.H.Lee, S.H.Lim and B.W.Lee “Feasibility Analysis of the positioning of Superconducting Fault Current Limiter for the Smart Grid Applications using Simulink and simpower systems”, IEEE Transactions on Applied Superconductivity, vol 21, 2011.
- [2] Yagami.M. and Tamura J “Enhancement of Transient Stability Using Fault Current Limiter and Thyristor Controlled Braking Resistor”, Power tech, 2007, IEEE Lausanne 2007.pp.238-243.
- [3] Yan Pan et.al, “Impact of waveform distorting fault current limiters on previously installed overcurrent relays”, Power Delivery IEEE Transactions on July 2008, Volume 23, pages: 1310-131.
- [4] V.K.Stood and S.Shahabur Alam, “3-phase Fault Current Limiter for distribution systems”. IEEE International conference on Power Electronics, Drives 2006.
- [5] Lee Seungje, Lee Chanjoo, Tae Kuk Ko and Hyun Okbae, “Stability Analysis of a power system with Superconducting Fault Current Limiter installed” IEEE Transactions on applied superconductivity, 2001, Vol.11, pp 2098-2101.
- [6] Kalkner B. “Short Circuit current limiter for coupled high power systems”, CIGRE 1966, paper 301.
- [7] Hannan M.A. and Mohamed A. “Performance evaluation of solid state fault current limiter s in electric distribution systems”, Research and development, Aug 2003.pages 245-250.