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Characterization of 6T CMOS SRAM in 65nm and 120nm Technology using Low power Techniques

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Abstract - *As the channel length of MOSFETs is scaling down, the Power dissipation of the SRAM cells become the major concern for future technology. In this paper, stable SRAM cell's power dissipation reduction in 6T static random access memory (SRAM), is described by using dynamic self- controllable voltage level (SVL) switch. Total power dissipation is reduced by 74/% and 84% at 1.2 volt and die area is increased by 36% and 69% from 120nm to 65nm technology respectively. The schematic and layout are drawn on 120nm and 65nm technology file on a Dsch tool and their analysis is done on a Microwind 3.1 tool and BSIM simulator.*

***Key Words*: Static Random Access Memory (SRAM), 6T memory cell, area, power dissipation, 120nm-65nm. SRAM , Stand-by power.**

1. INTRODUCTION

Design techniques for low-power circuits, for example, for use in battery-driven mobile phones, are not only storage circuits (such as flip-flops, register files, and memories) but also needed for logic circuits (such as very fast adders and multipliers). An integrated static random access memory (SRAM) is proposed to reduce leakage power at circuit and architectural level [1]. There are several techniques for reducing standby power. One of the method is multi threshold-voltage CMOS (MTCMOS). This technique reduces the power supply through the use of nMOSFET switches with higher threshold Vthn voltage and pMOSFET switches with higher threshold voltage Vthp. However, it has serious drawbacks such as the need for additional fabrication processes for higher Vthp and higher Vthn and the fact that storage circuits based on this technique cannot retain data. To solve this drawback, a self-contollable voltage level switch, which can decrease stand-by power, while maintain the high speed performance [2]. There is a significant increase in the subthreshold leakage due to its exponential relation to the threshold voltage, and gate leakage due to the reducing gate-oxide thickness [3]. The subthreshold leakage current is exponentially dependent on the gate-to-source voltage of a MOSFET [4]. When the SRAM circuit are in active mode, the SVL switch generated maximum supply voltage (e.g. Vd = 0.7V) and the minimum ground level voltage (Vs = 0V) to them through switches that are turned on. So the SRAM circuit can operate quickly. On the other hand when the SRAM circuit are in stand-by mode, it generates slightly lower supply voltage and relatively higher ground level voltage. The present work describes such an analysis and shows that use of SVL switch for reducing supply voltage yields the maximum reduction in leakage currents especially when the pre charge. Transistors are put in cut-off state during the stand-by mode. An SVL switch can be used either to reduce the supply voltage to the SRAM cell or increase the potential of ground level and the two approaches can be combined as well. Although a technique similar to use of SVL for raising the ground potential has already been reported to yield significant reduction in gate leakage currents [5],

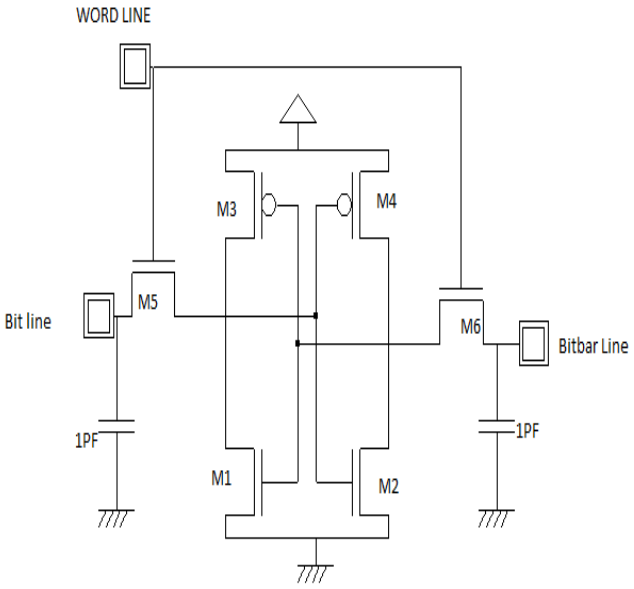

Figure1: schematic of 6T SRAM

An analysis of leakage currents in 6T SRAM cell has been carried out and techniques for suppressing it are compared. A number of techniques have been proposed in literature for reducing the impact of leakage power dissipation such as gate-Vdd scheme [6], Dual-Vt SRAM [7] etc. As a result, even though supply voltage has also been reduced with new generations of technology, the magnitude of leakage current has increased gradually and is likely to become comparable in future CMOS devices [8]. In this 6T SRAM cell comparison with 65 nm technology and 120 nm technology, The 6T SRAM cell consists of six transistors, in which two inverters (M1, M3 and M2 and M4)are connected in cross coupled manner, transistors M5 and M6 are write access transistor as shown in figure 1.

2. Leakage Control in 6T SRAM Bit Cell

It was described earlier that self- controllable switch can be used either at the upper end of the cell to reduce supply voltage (USVL technique) or at the lower end of the cell to raise the voltage of the ground node (LSVL technique). The switching energy, the short-circuit energy, and the power dissipation are assumed to remain constant under the same power supply [9]. The impact of these techniques on power dissipation is described in the next sections.

2.1 Leakage Control Using USVL

An SRAM cell consisting USVL techniques is shown in Fig. 2. In this technique, a full supply voltage is applied to SRAM cell in active mode, while the supply voltage level to SRAM is reduced to voltage level 'Vd' in stand- by mode. Since transistor M3 is in on state, voltage at the drains of M1 [10] and M3 is also reduced to 'Vd'. As before let us consider first the impact on gate leakage currents. As a result of a decrease in gate voltage of transistor M2, gate leakage current through it is sharply reduced. A decrease in drain voltage of transistor M1 results in lower gate-drain voltage across it and thus gate leakage current through it is also reduced. A decrease in source voltage of M6 results in a decrease in one component of EDT (Edge direct tunneling) leakage across it while leaving the other unchanged Gate leakage across transistor M5 remains unchanged. Transistor PU1 being a PMOS transistor does not result in any significant added leakage current as a result of transistors used in USVL circuit. LSVL technique has a better effect on power dissipation reduction. However, this technique is inferior with respect to subthreshold leakage current. While, sub threshold leakage through transistors M1 and M4 is reduced, further, a new sub threshold leakage current appears in transistor M6 as a result of reduction in its source voltage. To summarize, the USVL technique, while more successful in reducing power dissipation, still leaves two gate leakage current component in access transistor is unchanged.

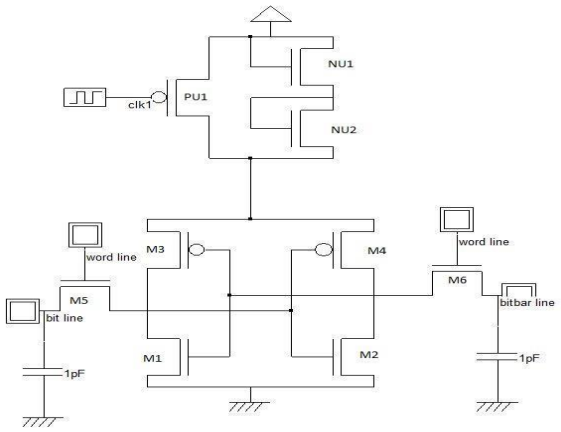

Fig. 2 Schematic of 6T SRAM cell after applying USVL technique

2.2 Leakage Control Using LSVL

Figure 3 shows a schematic of 6T SRAM cell in which LSVL technique is applied. The switch provides '0' Volt at the ground node during the active mode and an increased ground voltage (virtual ground) during the stand-by mode. This technique is similar to the diode footed cache design scheme proposed to control gate and sub-threshold leakages in SRAM cell, in which a diode designed with high Vt MOS transistors, was used to increase the ground voltage of SRAM [11],[12]in the stand-by mode. Let us consider the effect of this technique on power dissipation. An increase in the virtual ground voltage (Vs) therefore decrease of gate- source and gate-drain voltages of transistor M1 and gate-drain voltage of transistor M2 and results in sharp reduction in gate leakage currents of these two transistors. An SVL can be used either to reduce the supply voltage to the SRAM cell or increase the potential of ground node and the two approaches can be combined as well. However, there is no improvement in gate leakage currents for transistors M5 and M6. In fact, as a result of increase in drain voltage of M2. Incorporation of SVL results in another new gate leakage current through NMOS transistor NL1 in the SVL switch

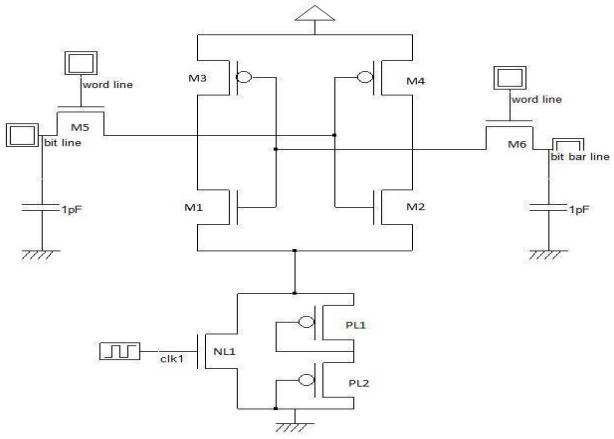

Fig. 3 Schematic of 6T SRAM cell after applying LSVL technique

As far as sub threshold leakage currents are concerned, LSVL approach is successful in reducing currents through M1, M4 and M5 as well. To summarize, one note that while all power dissipation are reduced using LSVL approach, it is only partially successful.

2.3 Leakage Control Using Combined Technique (USVL& LSVL)

Figure 4 shows the schematic of mixed technique (e.g. LSVL plus USVL). In this technique LSVL and USVL both are connected to the conventional seven transistors SRAM. By using this technique supply voltage is reduced [13].

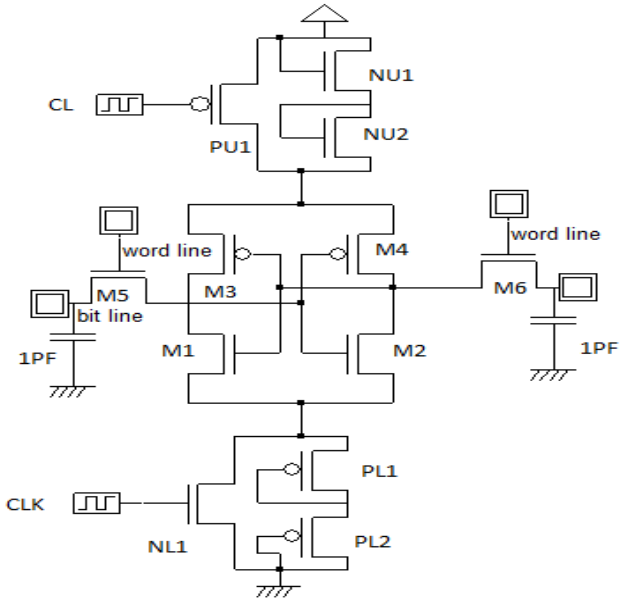

Fig.4 Schematic of 6T SRAM cell after applying USVL&LSVL technique

2.4 Advantage of SVL Techniques

There are very important advantages of the SVL circuit. When the SRAM circuit are in active mode, the SVL circuit supplies maximum drain-source voltage Vds to the on MOS through on Switch, thus the SRAM circuit can operate quickly. On the other hand, when the SRAM circuit are in stand-by mode, it supplies slightly lower Vd and slightly higher Vs to MOS transistor through "weakly on switch", thus the SVL circuit not only retains data but also produces high noise immunity with minimal overheads in terms of silicon area. Furthermore the Vth increase and consequently sub threshold current (Isub) of the "off MOS" transistor decrease,

4. Simulation Results and discussion

The power dissipation in the conventional and the schemes suggested in this section. Simulation results are simulated on. The 65nm and 120nm Micro wind tool with a nominal supply voltage 1.2 volt. The power dissipation being the only dominant mechanism at room temperature, SVL scheme suppresses the total power dissipation of 6T SRAM.

4.1 Layout of the 6T SRAM cell with USVL and LSVL of 120 nm

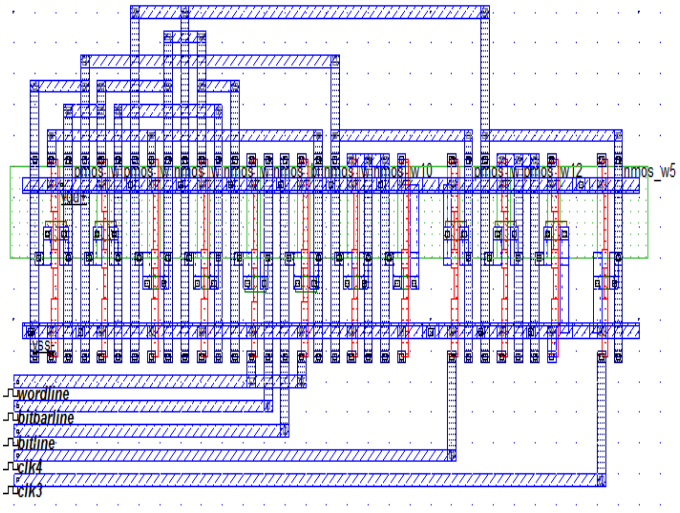

Fig 5. Layout of the basic 6T SRAM 120nm technology

4.2 Layout of the 6T SRAM cell with USVL and LSVL of 65nm

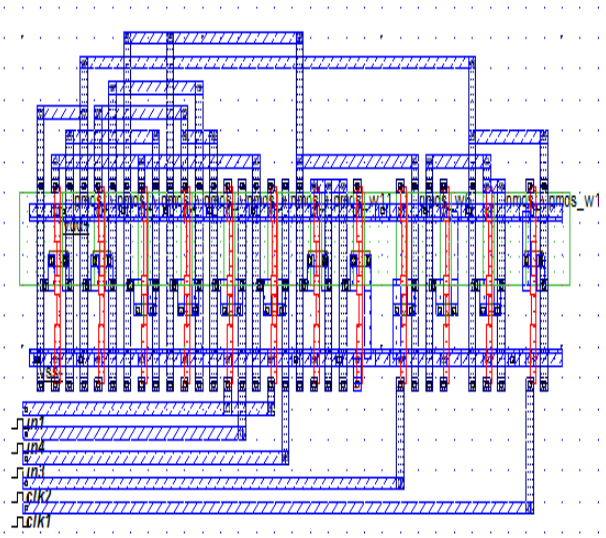

Fig 6. Layout of the basic 6T SRAM 65 nm technology

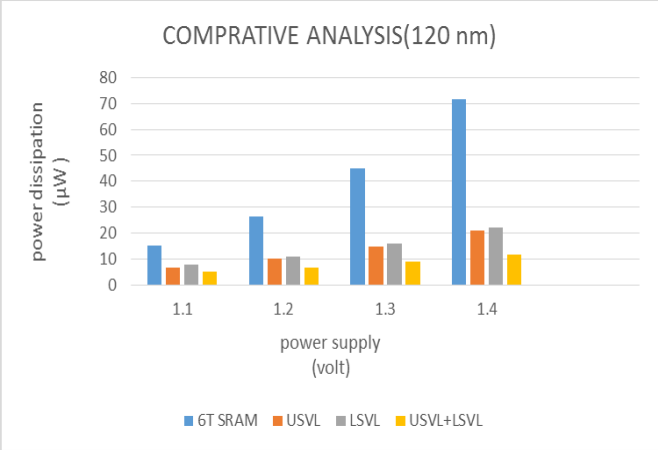

Fig 7: power dissipation versus power supply

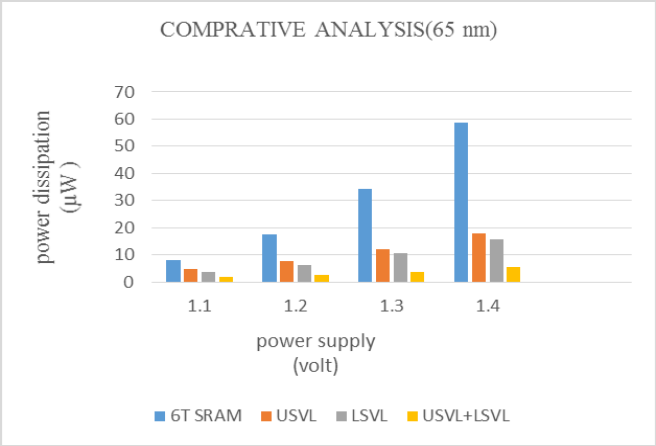

Fig 8: power dissipation versus power supply

Technique	Die Area(μm^2)	
	65nm	120nm
6T SRAM	48.4	72.3
USVL	74.9	117.4
LSVL	79.1	124.7
USVL&LSVL	124.3	171.8

Fig 9: Comparison chart of die area between 120nm and 65nm

5.0 Conclusion

An analysis of gate leakage currents in 6T SRAM cells for a 120nm and 65nm technology shows that power dissipation reduces from one technology to other technology and overall power dissipation in stand-by mode is also reduced. Reduction in supply voltage and increase in ground voltage using self-controllable voltage level switches for reducing leakage currents in 6T SRAM is examined in detail. It is found that while the LSVL approach is better in terms of reduction in power dissipation, the. However, both these techniques are found to be inadequate for power dissipation through access transistors. A modified USVL & LSVL approach in which access transistors are put in off state during the stand-by mode is found to be very effective in reducing all significant components of power dissipation.

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