International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 04 Issue: 06 | June-2017 www.irjet.net p-ISSN: 2395-0072

Design of a PID Controller using VHDL

Amana Yadav

[1] *Assistant Professor, Electronics and Communication Engineering, Manav Rachna International University, Haryana, India*

Abstract - *The intelligent control system's design is now the major area of research interest. The designing of an idea to implement these control systems need synthesis of artificial intelligence approach. In the industries the Proportional-Integral-Derivative (PID) controller is widely used controller now a day as it requires very few numbers of parameters are to be tuned and has simple structure. The PID is widely used in the application of robotics, power electronics, to control the temperature and to control the servo motor. Hence this paper, presents an implementation of PID controller using Xilinx ISE 10.1 software. For programming VHDL is used in this paper.*

Key Words: *Digital PID (Proportional-Integral-Derivative) Controller, Xilinx, FPGA, VHDL.*

1. INTRODUCTION

PID control is a control strategy and broadly used, as it is effective, robust, simple and applicable in wide variety of designs. PID controllers are widely used in larger than 95% of the process of industries now a day [1]. The PID is widely used in the application of robotics, power electronics, to control the temperature and to control the servo motor. Earlier it was implemented in solid state analog electronics, after that it was implemented using Microcontrollers, Microprocessor, Digital Signal Processors (DSPs) but it was not more flexible and performance was also poor. Sequential execution requires longer processing time to perform the task than DSP and Microcontrollers [2]. Now to realize digital control systems FPGA are used, which provides low power consumption, high computational speed, power efficiency, complicated functionality, accuracy and the capability to process real time function [3, 4].

In the industrial control systems, a common feedback loop is provided by PID controller component [5]. The process and other apparatus provide the calculated value to the controller. This value is compared with a value of reference point [6]. Then this variation is used as a signal to set the input to bring it at its desired set value. The PID can modify the output of process depending on the previous signal as well as on the rate of change of the fault signal, which provides very authentic and balanced control [7].

The paper is organized accordingly:

An overview of the PID Controller is presented in the section II. The methodology of the proposed approach and architecture of PID controller using FPGA is explained in section III. Simulation results attained using Xilinx 12.3 in terms of a RTL schematic with its timing diagram are shown in section IV. Section V concludes the theory.

2. METHODOLOGY

PID controller consists of the sum of its three correcting calculations:
1. Proportional: Immediate error can be handled by multiplying the error by a constant P and then finally add to the quantity under control. P is valid when controller's output is proportional to the system's error.

2. Integral: Here to take the previous value, the error is added up (Integrated) over a particular cycle of time, and multiply it with a constant I and then finally add with the controlled quantity.

3. Derivative: The error slope over time is measured for future handling and then multiplies it with another constant D, finally add with the controlled quantity [8].

2.1 The PID Actions

An architecture of a PID controller is shown in Fig.1 From the architecture it can be observed that the proportional, derivative and integrals are generated using error signal *e(t)* then the output signals are weighted and finally add all three signals which forms *u(t)* is added with Disturbance d(t) is introduced with the *u(t)* signal and applied to plant model. The equation of the PID controller is

$$u(t) = K_p[e(t) + \frac{1}{T_i}\int_0^t e(\tau)d\tau + T_d\frac{de(t)}{dt}]$$

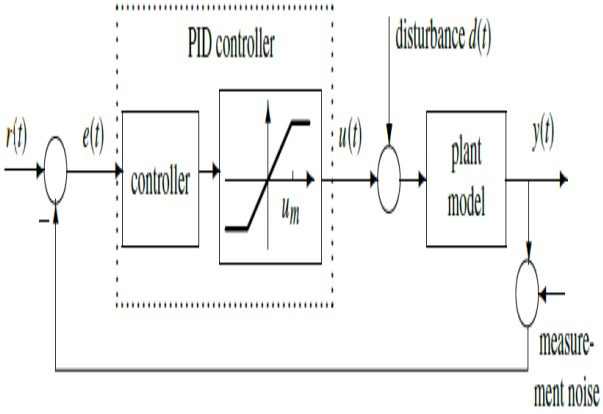

Fig -1. A Typical PID Control Structure

Transfer function form of PID is

$$K(s) = K_p + \frac{K_i}{s} + K_d s$$

Where

K_P= Proportional gain

K_i= Integral gain

K_d = Derivative gain.

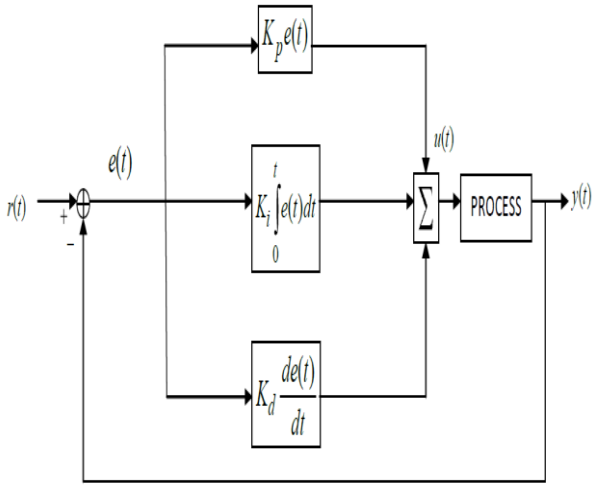

Fig -2. PID Control Logic

2.2 Digital PID Architecture

The three control actions proportional, integral, and derivative are added to form a PID controller. Complexity of design can be increases as per the requirement of additional additions or subtractions and multiplications or divisions blocks [9]. Hence to implement digital PID controller the given architecture is used which increases the efficiency of hardware. The proposed architecture includes three adders, three combinational logic multiplier, one subtractor and three registers to increase the speed and reduce the cost as well as provide the better performance [10]. The fig of the proposed method is

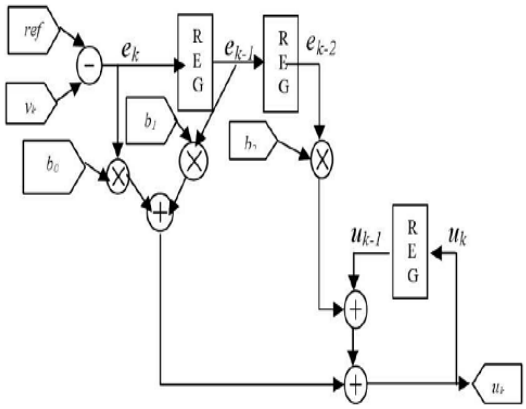

Fig - 3. PID Architecture

3. RESULTS

Before creating hardware of a system, simulation provides effective approach to verify the design on a computer. Designer can verify the signal values inside the design. To verify the function, Xilinx simulator tool is used to simulate the whole system. A VHDL code has been written to generate simulated results.

After performing synthesis step, the RTL diagram has been generated using Xilinx ISE software and shown in Fig4.

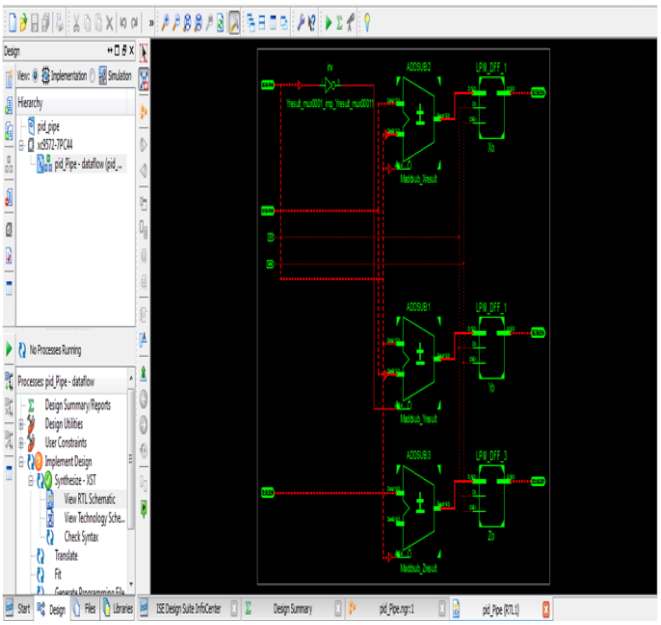

Fig - 4. RTL schematic design of PID system

As it is a hierarchical system, internal signals of sub sections are also shown in the waveform of simulator. The output waveform of PID controller is shown in the figure 6.

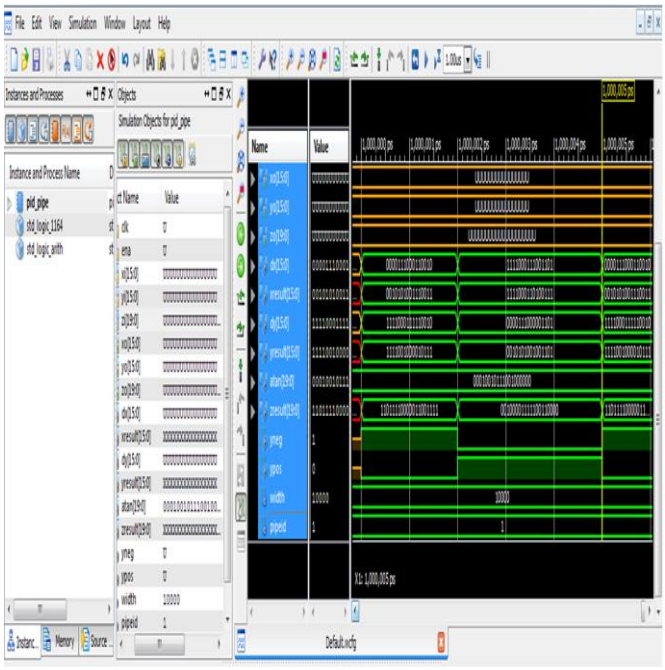

Fig -5. Simulation of PID control system by the ISE simulator

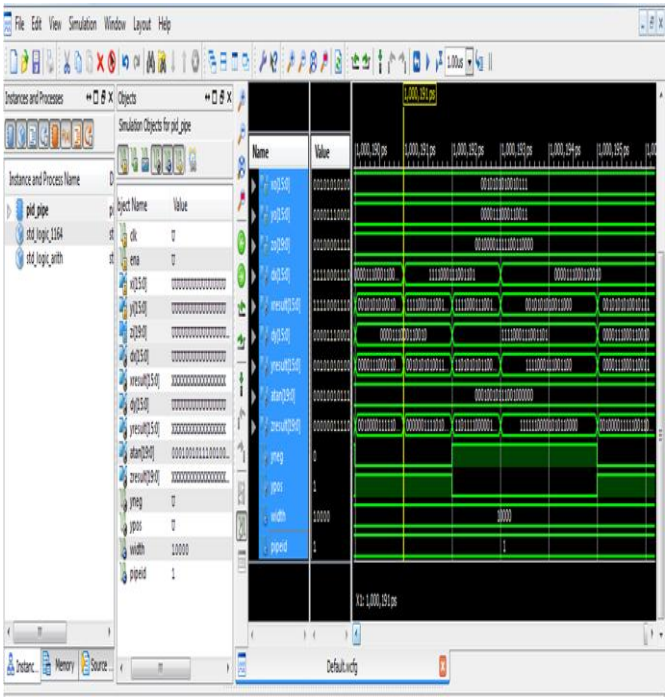

Fig -6. Simulation of PID control system by the ISE simulator

4. CONCLUSION AND FUTURE SCOPE

The given PID controller is successfully designed with the help of the Xilinx in FPGA technology. For other applications it can work as a general purpose controller. Using logic synthesiser the architecture of the PID controllers has been created. The estimated results achieved from Xilinx ISE have been presented. The PID controller designed here in FPGA technology is convictable controller in terms of resolution, latency, and parallelism. The designing of this controller has minimizes the complexity of the hardware and their cost.

As designing of PID controllers using FPGAs provides low power consumption, high computational speed, power efficiency, complicated functionality and accuracy, hence this PID controller can be designed for MEMS technology also in future.

REFERENCES

[1] K.J. Astrom and T. H. Hagglund, "New Tuning Methods for PID Controllers," Proc. of 3rd European Conference, pp. 2456-2462, 1995.

[2] Rajesh Nema, Rajeev Thakur, Ruchi Gupta "Design & Implementation of FPGA Based On PID Controller". International Journal of Inventive Engineering and Sciences (IJIES) ISSN: 2319–9598, Volume-1, Issue-2, January 2013.

[3] Shouling He and Xuping Xu, "Hardware/Software Co design Approach for an ADALINE Based Adaptive Control System," Journal of Computers, vol. 3, no. 2, pp. 29-36, Academy publisher, February 2008.

[4] Craig Hackney, "PGA Motor Control Reference Design," Application Note: Spartan and Virtex FPGA Families, Xilinx XAPP808 vol. 1.0, September 16, 2005.

[5] Manoj Gogoi, "Proportional-integral-derivative (pid) controller design for robust stability of arbitrary order plants with time-delay and additive uncertainty". Bachelor of Technology, B.P.U.T., India, 2007.

[6] Prof. Vikas Gupta Dr Kavita Khare, Dr R. P. Singh, "Efficient FPGA Design and Implementation of Digital PID Controllers in Simulink". International Journal of Recent Trends in Engineering, Vol 2, No. 6, November 2009.

[7] Abdesselem Trimeche, Anis Sakly, Abdelatif Mtibaa and Mohamed Benrejeb, "PID Controller Using FPGA Technology".

[8] Prashant Kumar, Ravi Mishra International Journal of Engineering Research and Applications (IJERA)

[9] Danlel E. Rlvera, Manfred Morarl,' and Slgurd Skogestad "PID Controller Design". Chemlcal Engineering, 206-4 1, California Instltute of Technology, Pasadena, California 91 125.

[10] M. Lelic, A Reference Guide to PID Controllers in the Nineties, In Proceedings of IFAC Workshop: Past, Present and Future of PID Control. 2000.

BIOGRAPHY

Amana Yadav was born on 15.10.83. She is currently working as an Assistant Professor in ECE Department of FET-MRIU, Faridabad. She is pursuing her Ph.D from Manav Rachna International university. She did M. Tech in VLSI Design from Mody Institute of Technology and Science, Lakshmangarh in the year 2008 and B.E. (Honors) in ECE from Sri Balaji College of Engineering and Technology, Rajasthan University in the year 2006. She did her thesis during M.Tech. under the guidance of Dr. S. C. Bose Scientist E2, CEERI, Pilani. Her Research interests include VLSI Designing.