

4-Bit Full Adder Using 1-Bit Hybrid 13T Adder

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Abstract - The focus of researchers throughout the years is a quest of designing low power and high speed adder. Addition is one of the fundamental arithmetic operations and is used extensively in many signal processing system and the heart of arithmetic logic unit (ALU). Several logic styles have been used in the past to design a full adder (FA) with the least power consumption and delay, and each design has its own advantages and disadvantages. Most of the new FA circuits were proposed using less number of transistors with less delay and low power requirement but different logic tend to prefer certain performance aspect. The usual 1-bit 28 transistors FA of standard courtesy style-based has the advantages of strength against voltage scaling and has regular layout but it requires high input capacitance. Therefore, the trend now is using hybrid logic approach which mixed various logic styles in improving the overall performance of the full adder. A 1-bit full adder is designed using 20 transistors through the hybrid approach. This full adder has a good characteristic in term of speed and power; but the weakness of this design is it depends on the modified semi XOR-XNOR gates which are not able to generate a full swing waveform for all its output. Even though this design offers significant improvement in terms of power and speed, the drawback is it consumes larger area than some other designs. The low power and high speed aim is achievable by this design by removing an inverter and balancing its delay. However, the adder circuit also produced incomplete voltage swing. Hence this project is proposing a 1-bit hybrid full adder (HFA) circuit using 13 transistors (13T) that will able to achieve the desired target. The proposed 4-bit adder is implemented using Tanner EDA tool.

Key Words: Arithmetic Logic Unit (ALU), Full Adder (FA), 13 Transistors (13T), Hybrid Full Adder (HFA), Tanner EDA tool

1. INTRODUCTION

The focus of researchers during the years is a quest of deceitful low power and high speed adder [1]. Addition is one of the fundamental arithmetic operations and is used extensively in many signal processing system and the heart of arithmetic logic unit (ALU). Several logic styles have been used in the past to design a full adder (FA) with the least power feeding and delay, and each design has its own advantages and drawbacks. Most of the new FA circuits were proposed using less number of transistors with less delay and low power requirement but different logic tend to prefer

certain performance aspect. Therefore, the trend now is using hybrid logic approach which mixed many logic styles in improving the total act of the full adder. In [5] a 1-bit full adder is designed using 20 transistors over the hybrid approach. This full adder has a good characteristic in term of speed and power; but the disadvantage of this design is it depends on the modified semi XOR-XNOR gates which are not able to generate a full swing waveform for all its output. Uniform though this design offers significant improvement in terms of power and speed, the drawback is it consumes larger area than some other designs. The low power and high speed aim is doable by this design by eliminating an inverter and matching its delay. However, the adder circuit also produced incomplete voltage swing. Hence this paper is proposing a novel 1-bit hybrid full adder (HFA) circuit using 13 transistors (13T) that will able to achieve the desired target.

1.13T XOR Module

Module I am a XOR gate ended up of only three transistors (3T). The design is based on an altered version of CMOS inverter and a PMOS pass transistor [4].

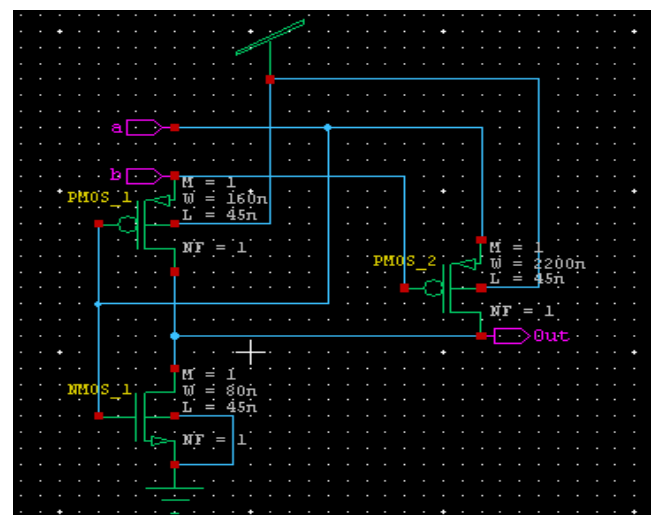


Fig. 1: Module I 3T XOR Circuit

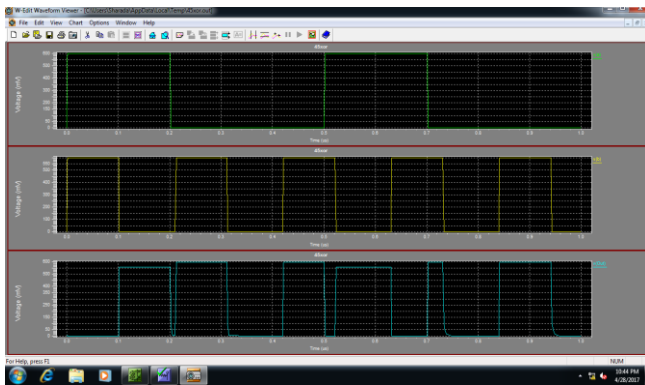


Fig. 2: Output of 3T XOR Circuit

1.2 XNOR Gate

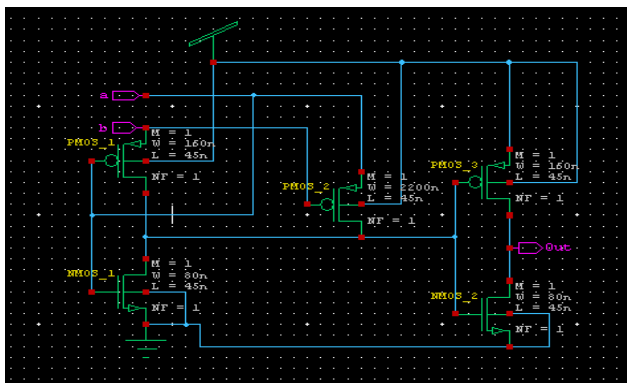


Fig. 3: XNOR Circuit

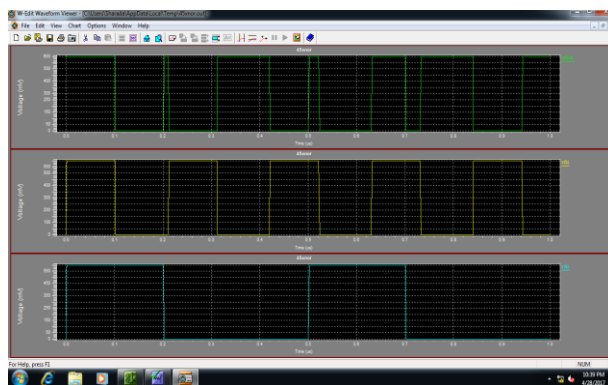


Fig. 4: Output of XNOR Circuit

2. New SUM Module

Module II is a new circuit being planned called sole sum circuit to yield output SUM for the HFA. Only four transistors are used as shown in Figure 3 as compared to the circuit which castoff six transistors [5]. The input to this new sum circuit is coming from the carryin bit (Cin) along with the output of module I (XOR) and its inverted form (XNOR). Both XOR and XNOR are used to control the gate of the upper

transmission gate in Figure, while the lower transmission gate is controlled by the carry-in (Cin). The output (OUT) of this module depends on the output value of XOR and XNOR gates.

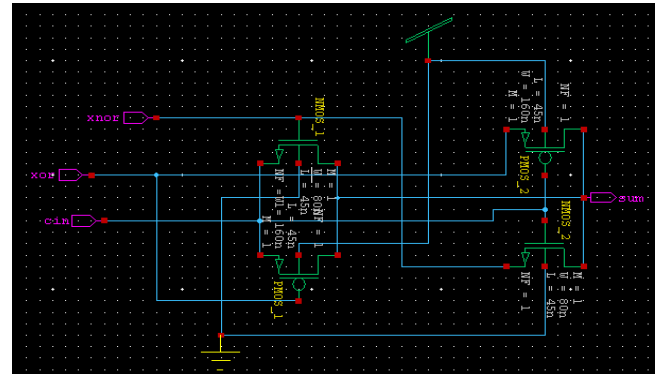


Fig. 5: Sum Circuit

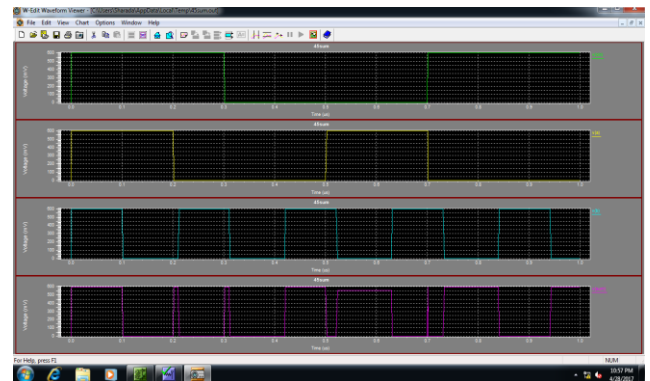


Fig. 6: Output of Sum Circuit

3. Cout Circuit

Module III has two sets of transmission gate which are controlled by XNOR and XOR as shown in Figure. The input signals (Cin or B) will spread through either one of these transmission gates. This circuit can curtail the overall carry propagation path and the propagation delay can be reduced further by the unhurried use of strong transmission gate.

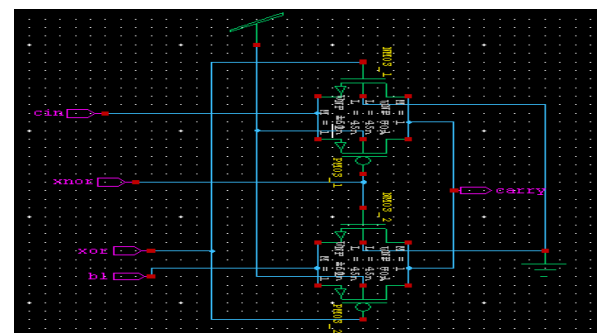


Fig. 7: C out Circuit

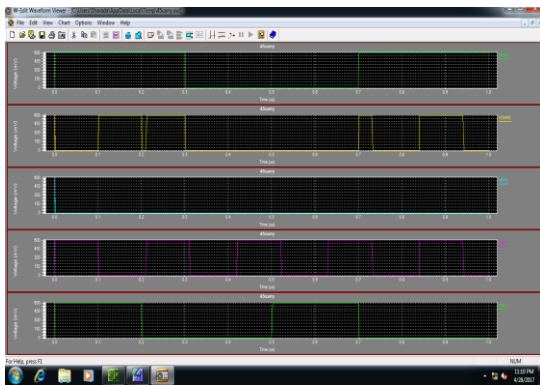


Fig. 8: Output of Cout Circuit

3. 13T Full Adder Circuit

The complete 1-bit HFA utilizes only 13 transistors so the design is called 1-bit 13T HFA. The design was simulated using General Purpose Design Kit (GPDKit) of Tanner EDA using 45 nm CMOS technology process. The schematic of the proposed 13T HFA was drawn using S-edit and shown in Figure, whereas the tested output waveforms are shown in Figure.

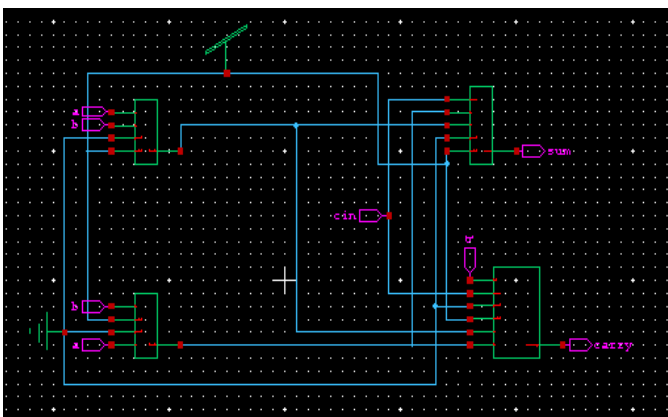


Fig. 9: 13T Full Adder Circuit

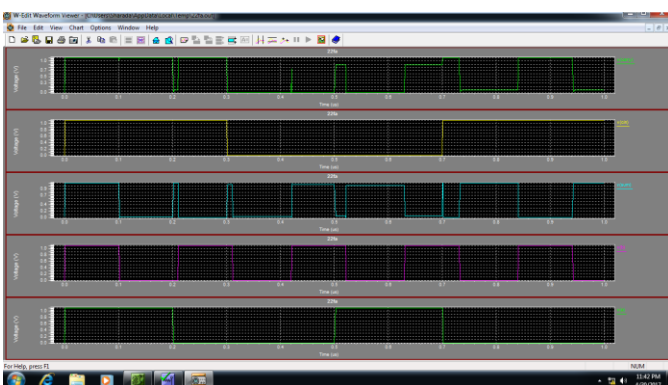


Fig. 10: Output of 13T Full Adder Circuit

4. 4-Bit Full Adder Circuit

Then four 1-bit HFAs are cascaded to form a full 4-bit ripple carry adder as depicted in Figure. The carry from the first HFA will propagate to the second HFA block and carry propagation takes place all the way to the last HFA block as it functions as a non-carry look ahead adder. Instance symbol had been created for the 4-bit full adder as shown in Figure (11).

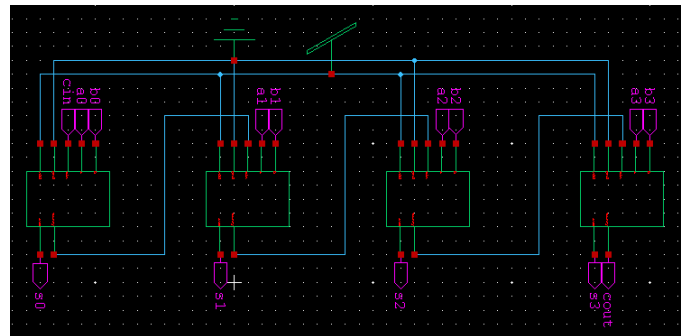


Fig. 11: 4-Bit Full Adder Circuit

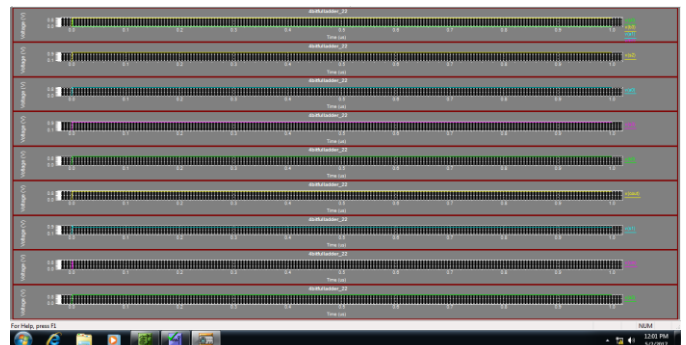


Fig. 12: Output of 4-Bit Full Adder Circuit

Table -1: Results on 22nm,32nm & 45nm Technology

Technology	13 Transistors	20 Transistors	28 Transistors
Power(uw) at 45nm	2.86	7.32	8.45
Power(uw) at 32nm	2.36	3.36	6.23
Power(uw) at 22nm	1.63	2.63	3.58

5. CONCLUSIONS

In this paper, a low-power 1 bit hybrid full adder using 13 transistors (1-bit 13T HFA) is proposed and observe the 1-bit 13T HFA is performing well in terms of power consumption as compared to 28 transistors and 20 transistors reported works on 1-bit full adder. And Power

are compared on 22nm,32nm & 45nm technology's in Tanner EDA Tool 13.

6. REFERENCES

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BIOGRAPHIES



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