

# Implementation of NoC Router and its Architecture

Arshi Nazish<sup>1</sup>, Waseem Khanooni<sup>2</sup>

<sup>1</sup>M.Tech Student , Department of Electronics

<sup>2</sup>Assistant Professor, Department of Electronics

S.B.Jain Institute of Technology,Management and Research,Maharashtra,India.

**Abstract** - An Network-on-Chip is a new paradigm of communication network into System-on-Chip (SoC). It overcomes the problems of traditional bus-based SoC and meet the communication requirement of next SoC.. It provides efficient communication and the data is routed through the networks in terms of packets. The routing of data is mainly done by routers. A router is one of the most important communication back bone in NoC. The design is implemented in VHDL and simulated in Xilinx ISE Design Suite 13.

**Key Words:** Network-on-chip(NoC), System on chip(SoC), Field Programmable Gate Array(FPGA), Router,Architecture.

## 1. INTRODUCTION

NoC is a method to design the communication subsystem between intellectual property cores in a SoC. System on chip uses dedicated buses for communicating with the resources. Using buses as communication strategy does not give any flexibility for the needs of communication. Secondly using shared buses does not scale very well as the number of resources increases in number. These drawbacks have been overcome in Network-on-chip by implementing a communication network of routers and resources and by using a packet-based communication network. Implementation medium has highly affected the configurations of SoCs and their interconnect mechanisms in term of cost and performance. NoC is becoming popular as it reduces the feature sizes and increasing use of parallel architectures. Field Programmable Gate Array (FPGA) has gain popularity over Application Specific Integrated Circuits (ASICs) in several contemporary applications because of its advantages such as low development cost and the short time required to market, Secondly, FPGA is ease to upgrade and have suitability for research purposes, given that they provide fast design cycle and immediate results.

## 2. NoC ARCHITECTURE

Various interconnection schemes such as crossbar, buses and NoCs are currently in use. Crossbar and buses have poor scalability because of more number of processing elements. As the number of elements increases, the performance of the system degrades dramatically. Due to these disadvantages, now a days, Network -on chip is generally being used which consists of processing

elements (PEs), network interfaces (NIs), routers(R) and channels. The PE and Nis comprise the architecture. The NI packetizes data before traversing through the NoC. Each PE is attached to NI that connects the PE to local router. The data packet transmission takes place between sources PE to destination PE. During transmission the packet is forwarded hop by hop on the network depending on the decision made by the router. The router further contains switches and buffer. The buffer is also an important parameter which consumes around 64% of total node leakage power. A node comprises of a router and the link associated with it. In router, the packet is first received and stored at input buffer. The control logic of router makes the routing decision and channel arbitration and finally the selected packets traverse to next router through a crossbar. This process is repeated until the packet reaches its destination. Several Processing Elements (PEs) together comprise a generic NoC implementation. The Processing Elements (PEs) can be various processors, memory elements and dedicated hardware like audio cores, video cores, wireless transceivers etc. Each PE is linked to a local router through a Network Interface (NI). The NI can be used to packetize or de-packetize the data into or from the underlying interconnection network. Router transmits the data from source to its destination, using special purposed routing algorithms and control flow mechanisms.

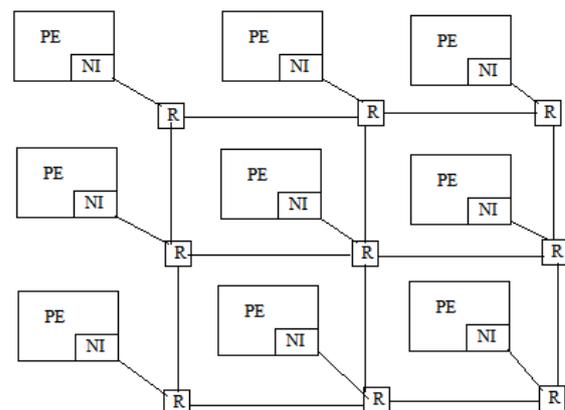


Fig 1.Generic NoC Architecture

## 3. ROUTING ALGORITHM

The routing algorithm defines the path to be followed by a packet to travel from source router to destination router.

Our goal is to make this routing scheme as simple and efficient possible in order to have high speed performance ,low area and low power consumption. Network ties such as deadlock, livelock and starvation should be avoided as much as possible. While designing NoC router it has to be taken care that there is possibility of offering recovery mechanisms and congestion control .For NoCs ,the most popular routing algorithm used is XY routing algorithm that is usually implemented using a distributed routing .The data packet is first directed towards X axis until it reaches towards Y axis of the destination node. Then, it is moved in Y axis to reach the destination. The routing decision time is one of the important that affects the latency of the network. The routing algorithm and its implementation methodology highly affect the latency.

#### 4. FPGA IMPLEMENTATION

The most popular FPGA families of devices used in NoC research are Xilinx [19] Virtex-II and Virtex-4, and Altera Stratix and Stratix II. Before making the decision to choose the appropriate family and device that will be used for accommodating the application design, Their structures and characteristics should be well studied in order to meet the following requirements:

Application requirements such as area, speed, and power.

It should be able to make a comparison between the design on hand and previous work fairly.

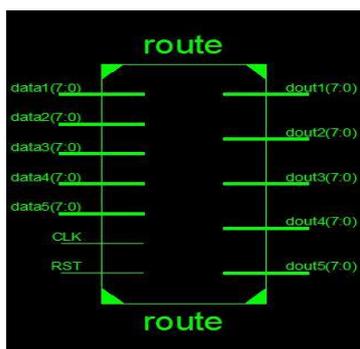


Fig 2. FPGA Implementation of NoC Router

#### 6. IMPLEMENTATION

The router architecture has five input ports, five output ports and each input port has four virtual channels with each VC having four flit buffers. The data coming to each input port is stored in virtual channels temporarily. Each input port sends a request to the arbiter to grant access to

the crossbar. So, based on the priority level of each input port, arbiter grants access to the crossbar. Then the data traverse through the crossbar and reached to the destination port

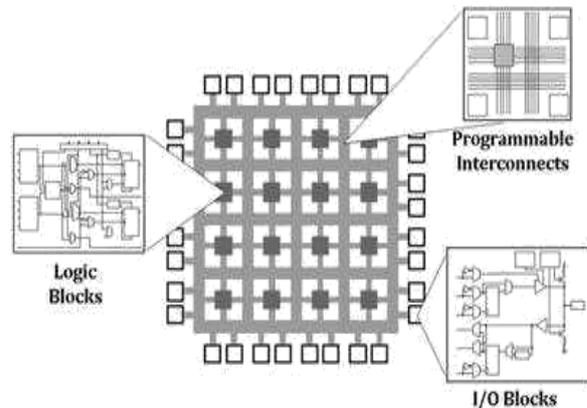


Fig 3.RTL view of NoC Router

#### 7. CONCLUSION

In this paper, a five port NoC router is proposed using fixed priority arbiter. Xilinx ISE design suite 13.1 tool is used for the synthesis and simulation of the router. As fixed priority arbiter can be used for few requesters and there is no limit to how long a lower priority request should wait until it receives a grant so this can affect the network performance. This router can be modified by using a strong fairness arbiter such as round robin arbiter.

#### 8. REFERENCES

R. V. Kshirsagar , “ Design of NoC Router Architecture using VHDL,“in International Journal of Computer Application(0975-8887) vol.115-No. 4, April 2015.

Pankaj Agrawal and Bharati B. Sayankar, “Minimization of Latency and Power for Network on chip” in International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169 Volume: 3 Issue: 2, February 2015

Asha R, <sup>2</sup>Divya Prabha, <sup>3</sup>Dr.M Z kurian, “Adaptive Router Design for Networks-On-Chip on FPGA using Buffer Resize Technique” in International Journal of Engineering Trends and Technology (IJETT) - Volume4 Issue7- July 2013.

Concatto, C., Matos, D., Carro, L., Kastensmidt, F., Susin, A., and Kreutz, M., “NoC Power Optimization Using a Reconfigurable Router”. In the IEEE Symposium on VLSI, 2009.